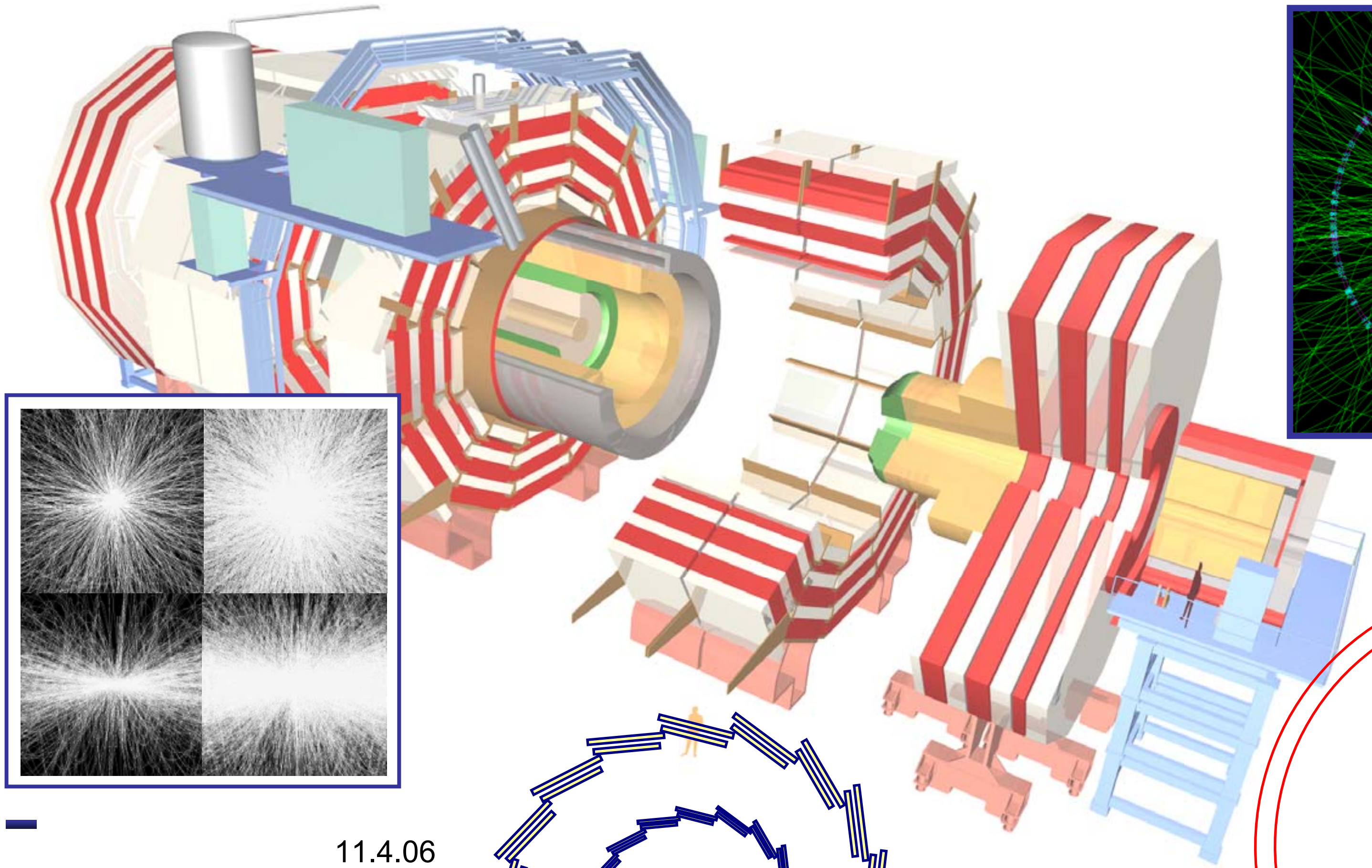
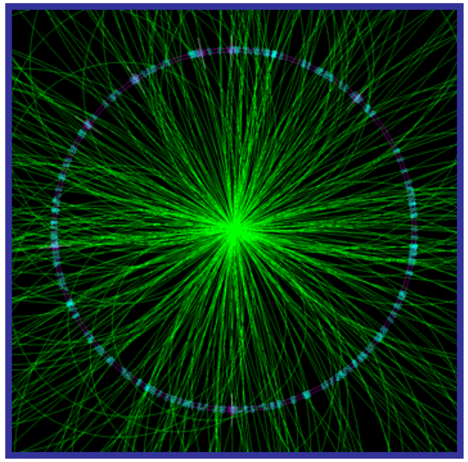
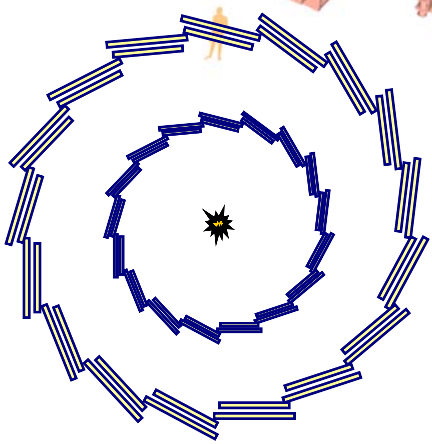
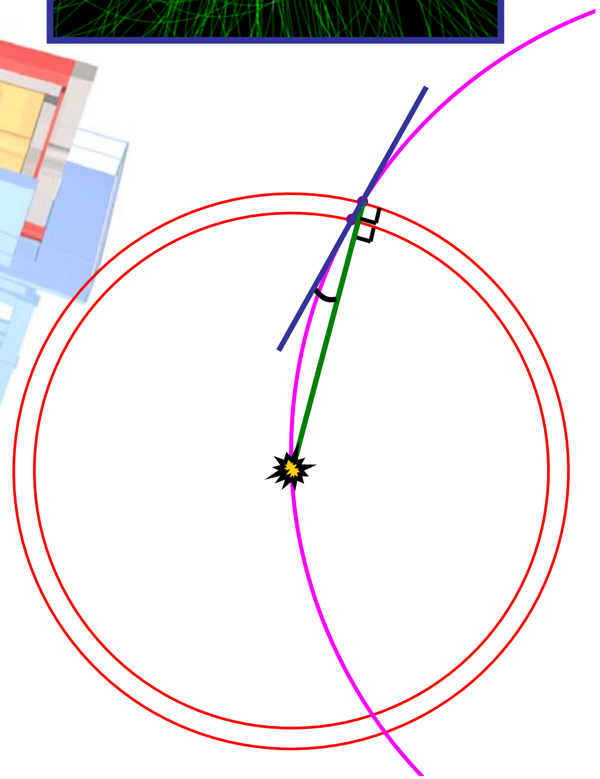
A Level-1 Tracking Trigger in Super-LHC









11.4.06

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CMS and The Super LHC

- Current CMS trigger is designed for 'clean' (relatively unambiguous) signatures
  - Higgs → **Muons, di-photons**, (jets, 4 leptons)
  - SUSY → **Missing E_T, leptons**, (topological jet triggers)

- 1st level of triggering in CMS has to perform fast, complex calculations in ~1.5μs

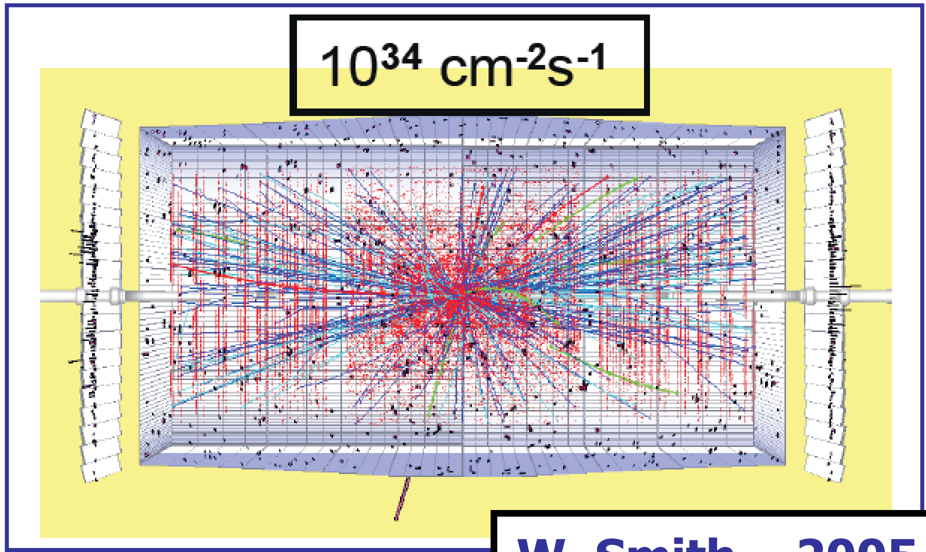
- Design of trigger was driven by many constraints
  - **Money, power, cabling, radiation tolerance, hardware capability, speed, availability**

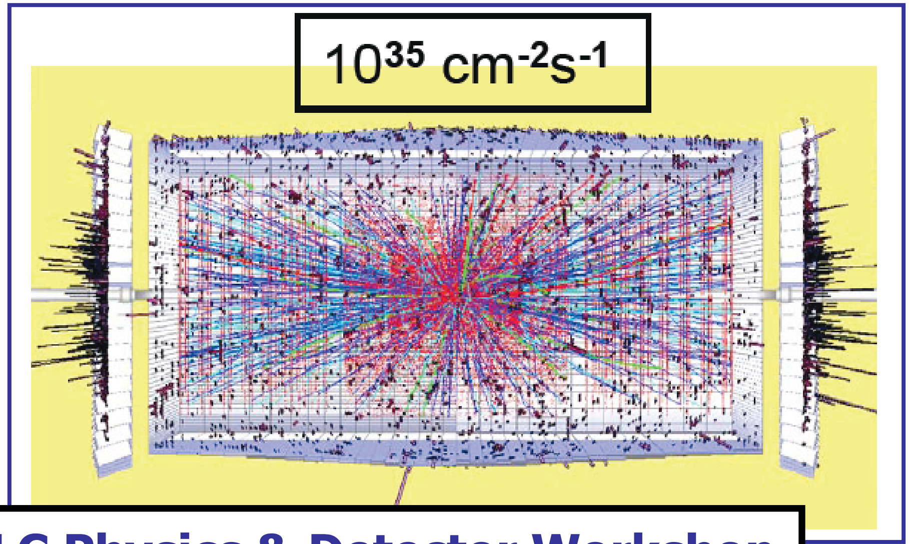
- **It has been proposed that LHC be upgraded x10 nominal luminosity in 2015**

  $10^{35}cm^{2}s^{-1}$

- Requires an improvement in detector performance to allow efficient triggering
- It is widely believed that CMS requires tracking information in L1 trigger in the future
- Tracker is not currently used for many reasons
  - Data rate is too great, even for nominal LHC environment
  - In upgrade, rate at r=10cm is **~10Gbit/cm^2/s** when zero-suppressed

What Does It Looks Like? (Why It's A Problem)





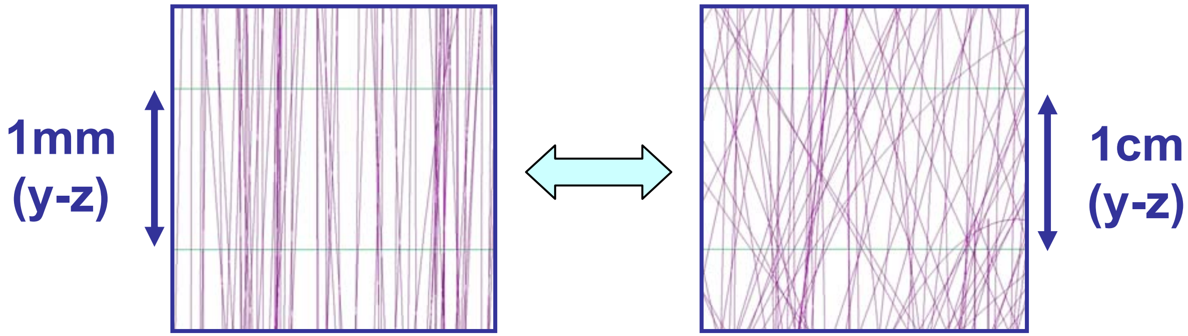
W. Smith – 2005 ILC Physics & Detector Workshop

- Leptons, photons and pions look like jets (lack of isolation)
  - Incorrect energy, no isolation, miss-identification
- Jets look like clusters of jets (lack of isolation)
  - Incorrect count, incorrect energy, incorrect missing E_T
- Muon chambers lose ability to threshold rate of trigger based on p_T of track
  - Inability to control single-muon trigger rate (although not certain we use this in SLHC)

- Bandwidth of DAQ system increases x10 if trigger rate same as current LHC
  - <u>If we allow trigger rate to increase, requirement grows x100 – **UNACCEPTABLE**</u>

What Do We Want To Do?

- We want tracker information in the L1 trigger in SLHC (at least a '**stub**')
- Purity of reconstructed tracks isn't important…
  - …provided reconstruction efficiency for 'interesting' tracks must be very high



- Propose to use two **closely-spaced** electrically coupled pixel detectors in a **stack**
  - Reduces **combinatorials** to manageable levels (J. Jones, A. Rose, C. Foudas)
  - Design can be introduced into current CMS tracker with minimal disturbance
- **Reduce the data-rate** **on-detector** with a **geometrical p_T-cut**

  \+ Lower power consumption (than reading everything out)

  \+ ~100Mbit/cm^2/s optical links (reduced cabling requirements)

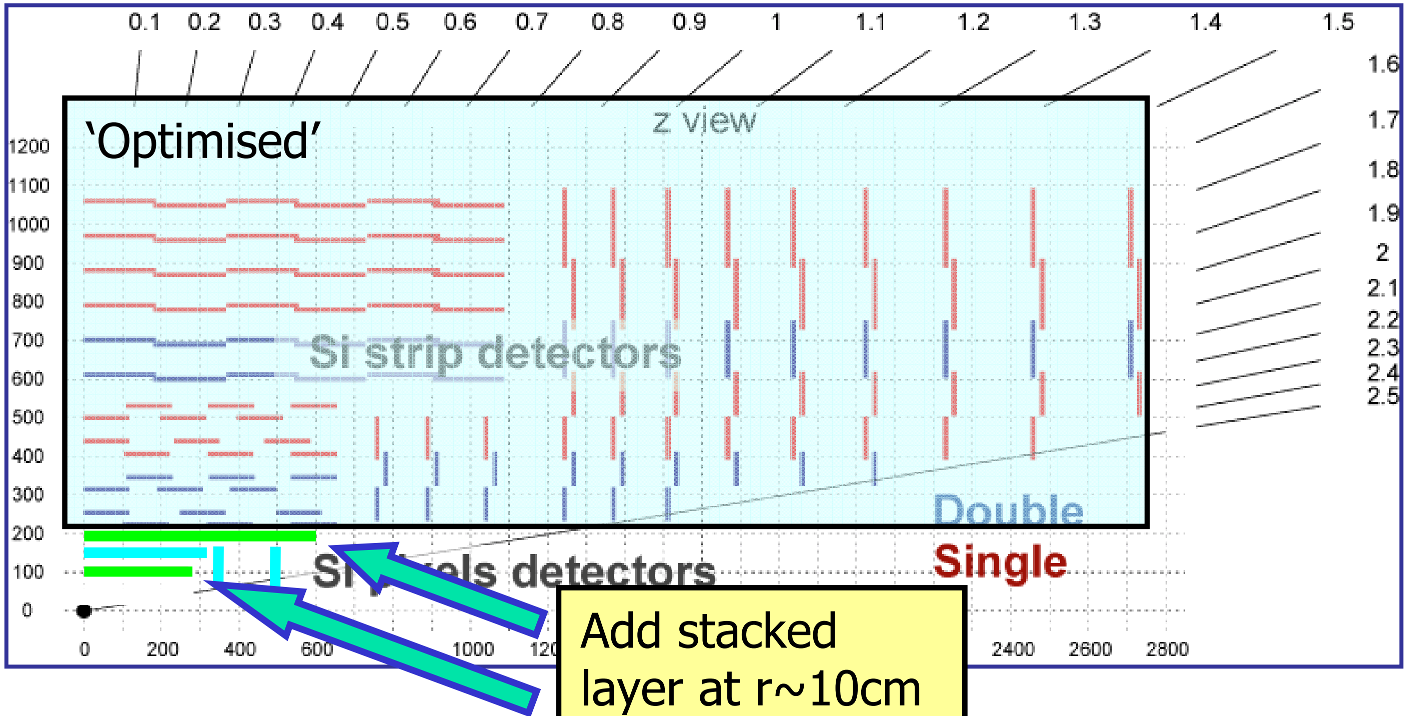
  \+ Close electrical coupling - avoids the need for detector-wide communication

  \- Cannot be used to infer p_T using only one stack

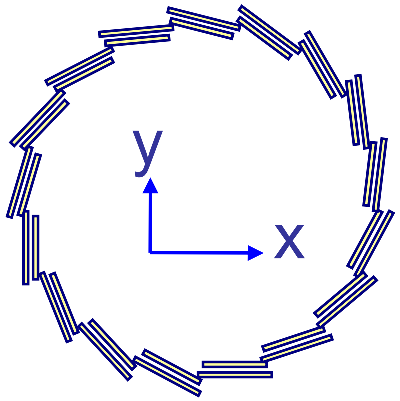
  \- Places strict demands on mechanical aspect of design

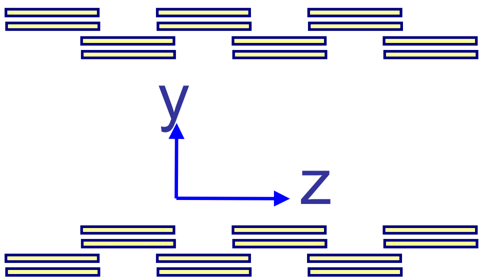
  \- Material budget of detector must not increase significantly

Possible Detector Layout



Add stacked layer at r~10cm & r~20cm





Detector Dimensions:
Tiled, each tile ~2cmx2cm
Total size 120cm(z)x20cm(r) & 60cm(z)x10cm(r)

Pixel Pitch: 10μm(r)x200μm(z)x20μm(φ)

Tangent-Point Reconstruction

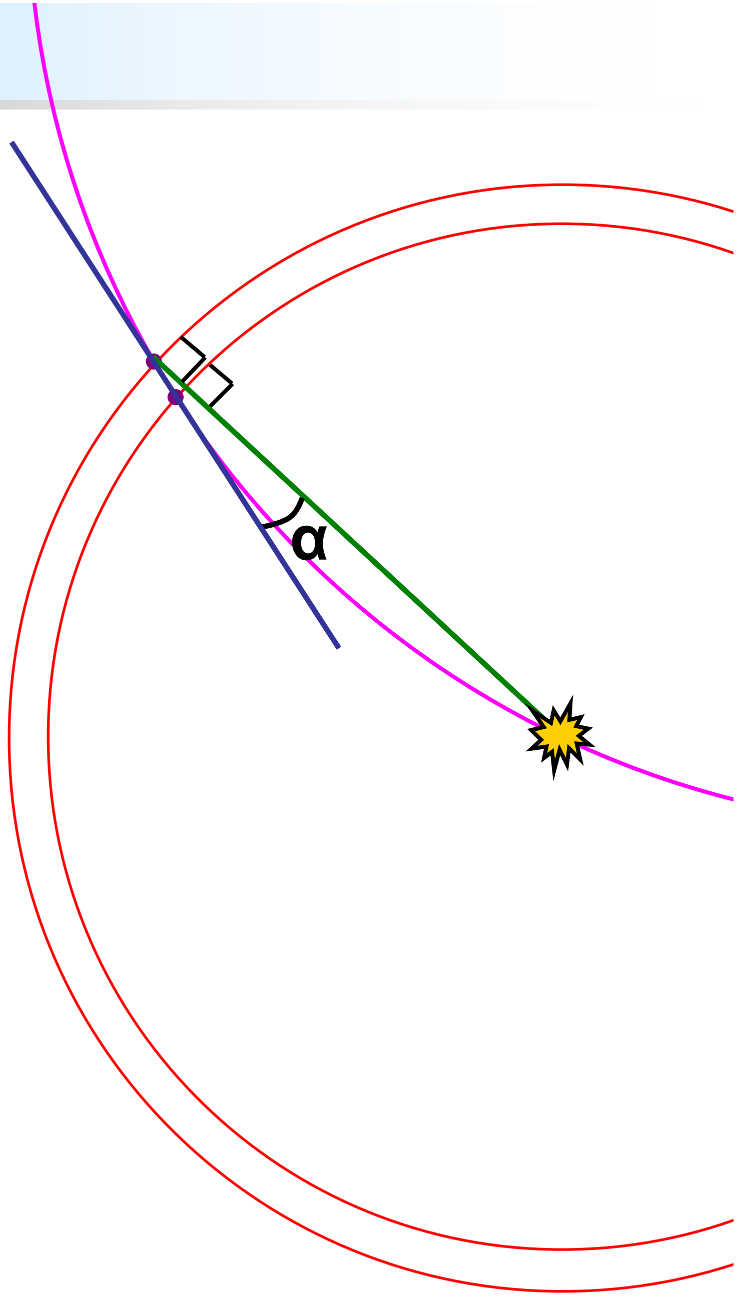
- Assume IP r=0
- Angle **α** determines p_T of track

Smaller α = greater p_T

- Can find high-p_T tracks by looking for small angular separation of hits in the two layers
- Correlation is fairly 'pure' provided separation is small and pixel pitch is small

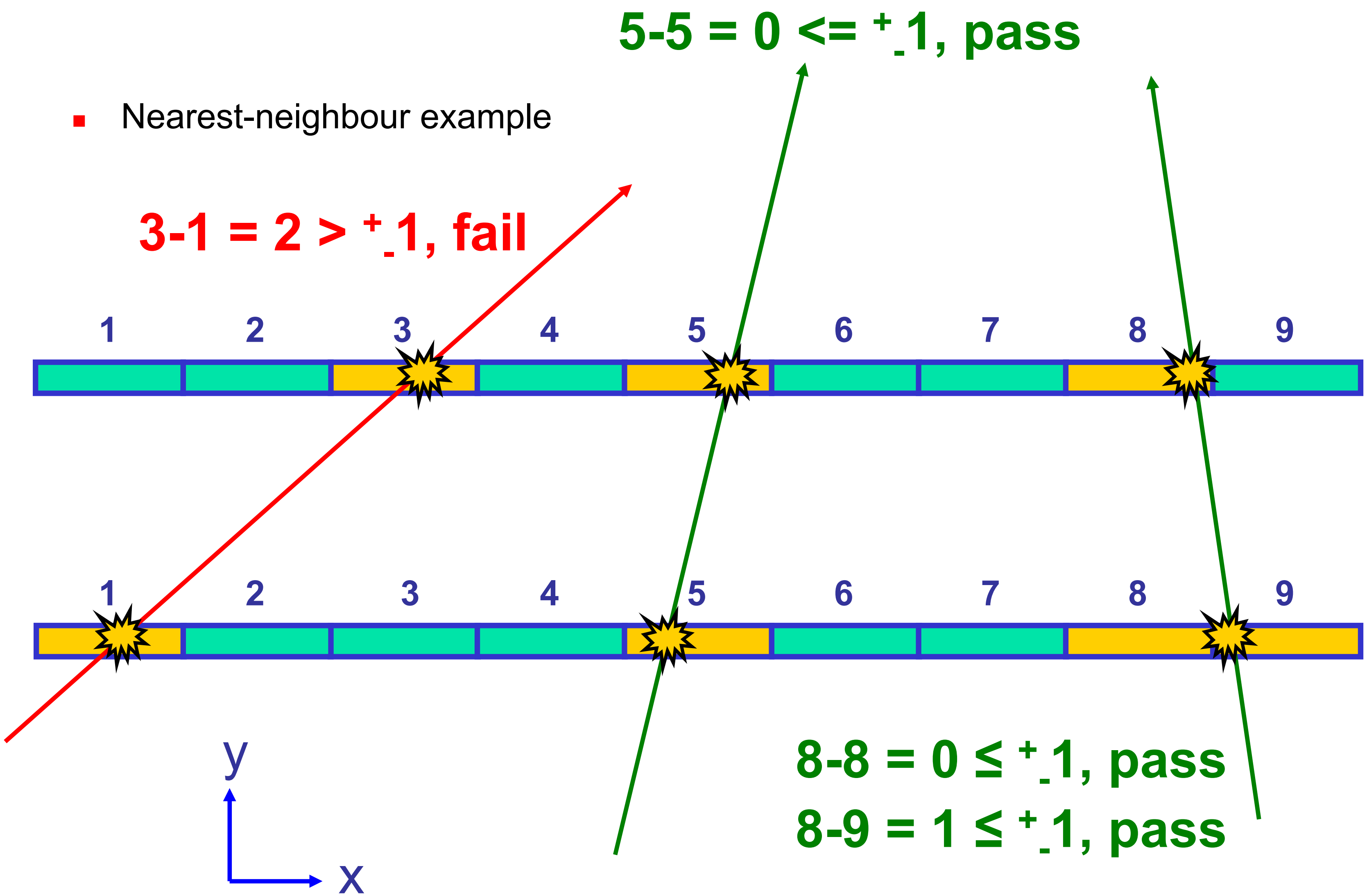
Matching hits tend to be from the same track

- If sensors are precisely aligned, column number for hit pixels in each layer can be compared
- Finding high-p_T tracks becomes a relatively simple **difference analysis**



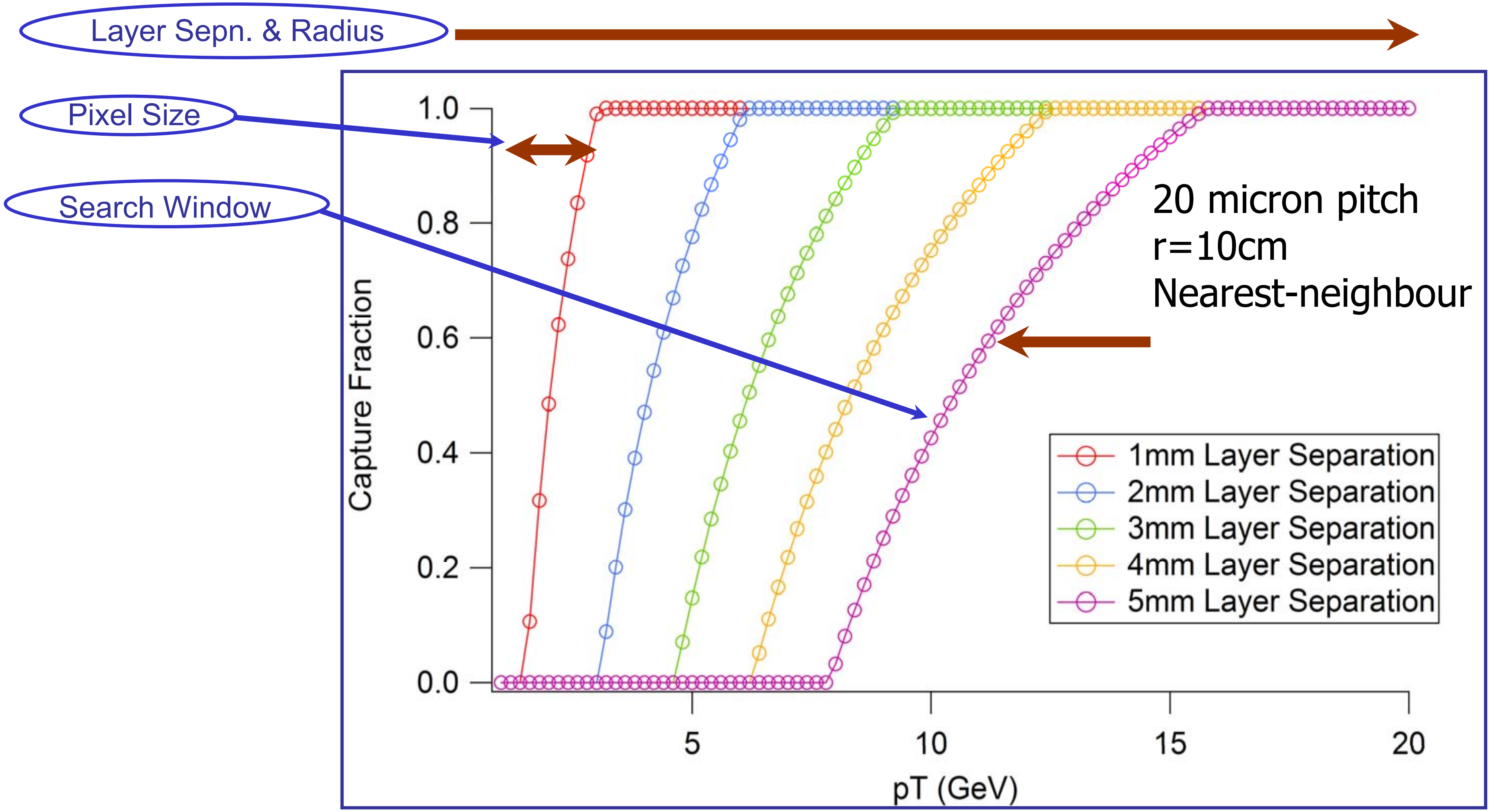
Difference Analysis in Practice

- Nearest-neighbour example



p_T Cuts in a Stacked Tracker – p_T Cut Probabilities

- Depends on:



There is an additional 'blurring' that is caused by charge sharing…

Monte Carlo Results – Purity / Data Rate (Minimum Bias)

- Just showing 200 events / BX as an example (10^{35}@40MHz)

These should be lower – subtle effect

Layer Sepn	Threshold	Window Size (PIX)	Purity % R=10cm	Purity % R=20cm	Data Rate % R=10cm	Data Rate % R=20cm
1mm	Low	2	81.2	76.7	12.2	3.19
1mm	High	2	78.2	72.0	9.82	2.45
1mm	Low	1	88.4	90.7	6.80	1.66
1mm	High	1	82.9	81.5	4.83	1.13
2mm	Low	2	21.7	9.15	5.77	1.68
2mm	High	2	17.2	7.56	4.79	1.40
2mm	Low	1	43.9	31.6	3.54	1.06
2mm	High	1	27.1	13.6	2.69	0.84

- Is better at 100 events / BX (10^{35}@80MHz) – lower occupancy…
- I also simulated 500 events / BX ($5x10^{35}$@80MHz!)
  - Still appears to work

Key Differences w.r.t The Current Tracker

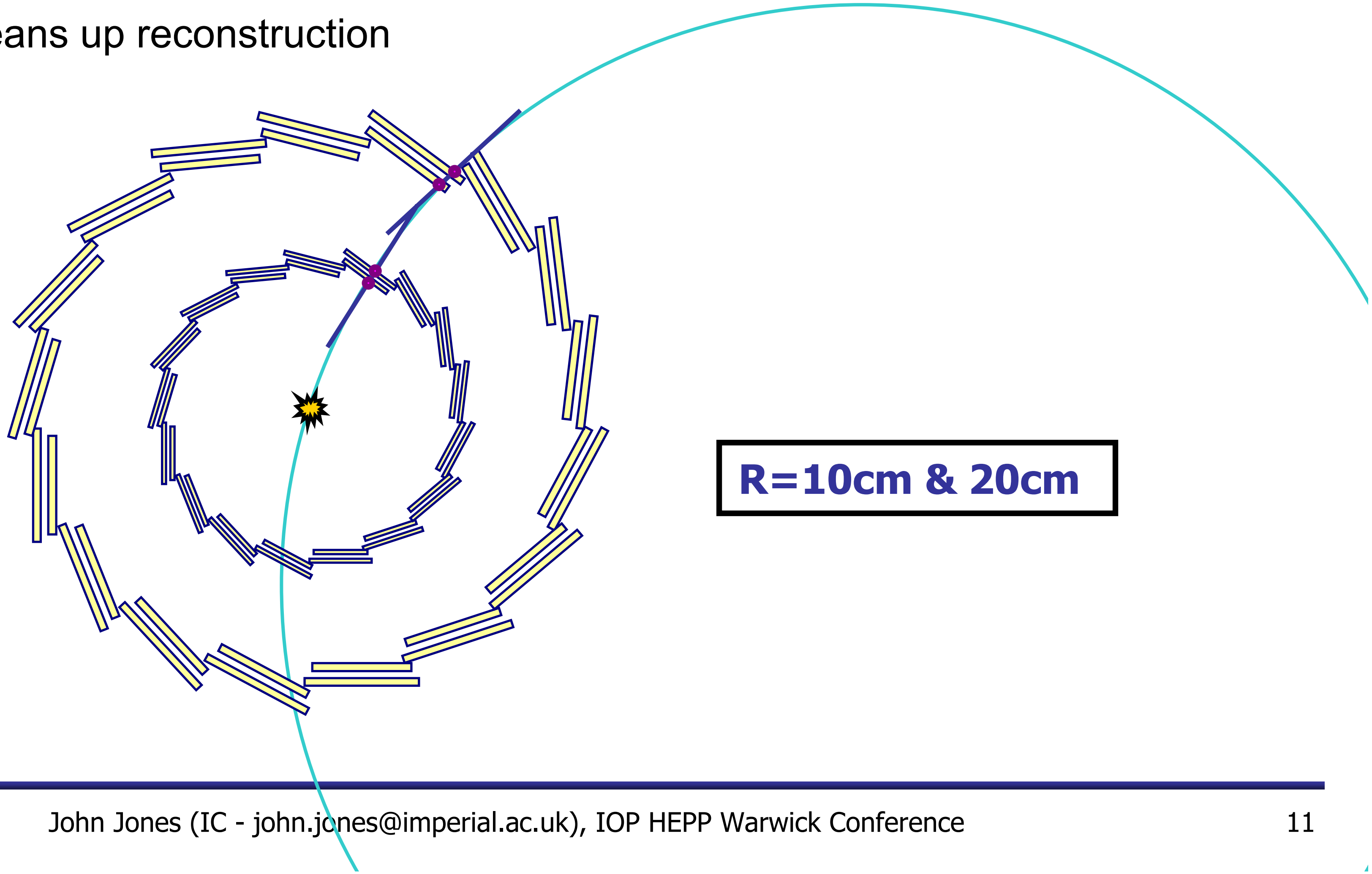
- Pixels are **stacked**
  - Electrically coupled
  - No long-range (>mm) inter-layer communication
  - Reduces combinatorials
  - Speeds up reconstruction
  - Allows p_T cut in hardware placed on-detector to reduce data volume
    - ~x10-x100 depending on tradeoffs
    - Results in **asynchronous processing** (variable data rate)

- Shape of pixel is **significantly elongated**
  - 20μm (phi) x 200μm (z) x 10μm (sensitive thickness – could be bigger)
  - Phi pitch and thickness are critical
  - Hit needs to be localised in (r-phi) as otherwise thickness of region has a serious impact on sensor resolution / p_T cutting
  - Also need to minimise charge spread to reduce data rate
  - z resolution (pitch) can (has to be) be optimised for power / ECAL resolution

- You **can't compute p_T** with just one stacked layer
  - Unless matched with muon tracks or calorimeter hits…
  - …or double stack

The Double-Stack Method

- Close space minimises combinatorials in each layer and allows p_T cut to be applied ‘easily’ **on-detector, but in each stack separately**
- Separation between two stacks allows **calculation of p_T (albeit crudely)**
- Can also do **z-vertexing**
- Also cleans up reconstruction



R=10cm & 20cm

Summary

- Designing a pixel sensor for SLHC presents a lot of challenges
  - But stacked approach limits readout rate leaving detector
    - Manageable data rates leaving detector
    - Reduces combinatorials
    - Allows fast reconstruction
    - Demonstrated by toy Monte Carlo (full study planned)
- Reconstruction algorithm demonstrated in Imperial College (B. Constance, K. Zhu)
  - **Very, very fast** (~3BX = 75ns)
  - Implemented for IDAQ
    - FPGA-based generic DAQ board derived from CMS APV25 emulator
      - G. Iles, J. Jones
  - Algorithm currently being optimised
- Plans to build a prototype correlation → link → reconstruction system
  - Based on IDAQ & GCT Source Card (J. Jones, A. Rose)
  - Possible large-scale prototype based on GCT Leaf Card (M. Stettler)
- Many promising sensor technologies under investigation (MAPS, TFA, Hybrids)

Additional Slides

A Toy Monte Carlo…

In the interest of speed (a

Convert ntuples via H2RO

Solve tracks for barrel reg

- Includes z vertex blu
- Includes primitive ch
- Doesn't include had
- …but still useful for
- Could extend up to

Simulates threshold trigg

100 & 200 events/bx

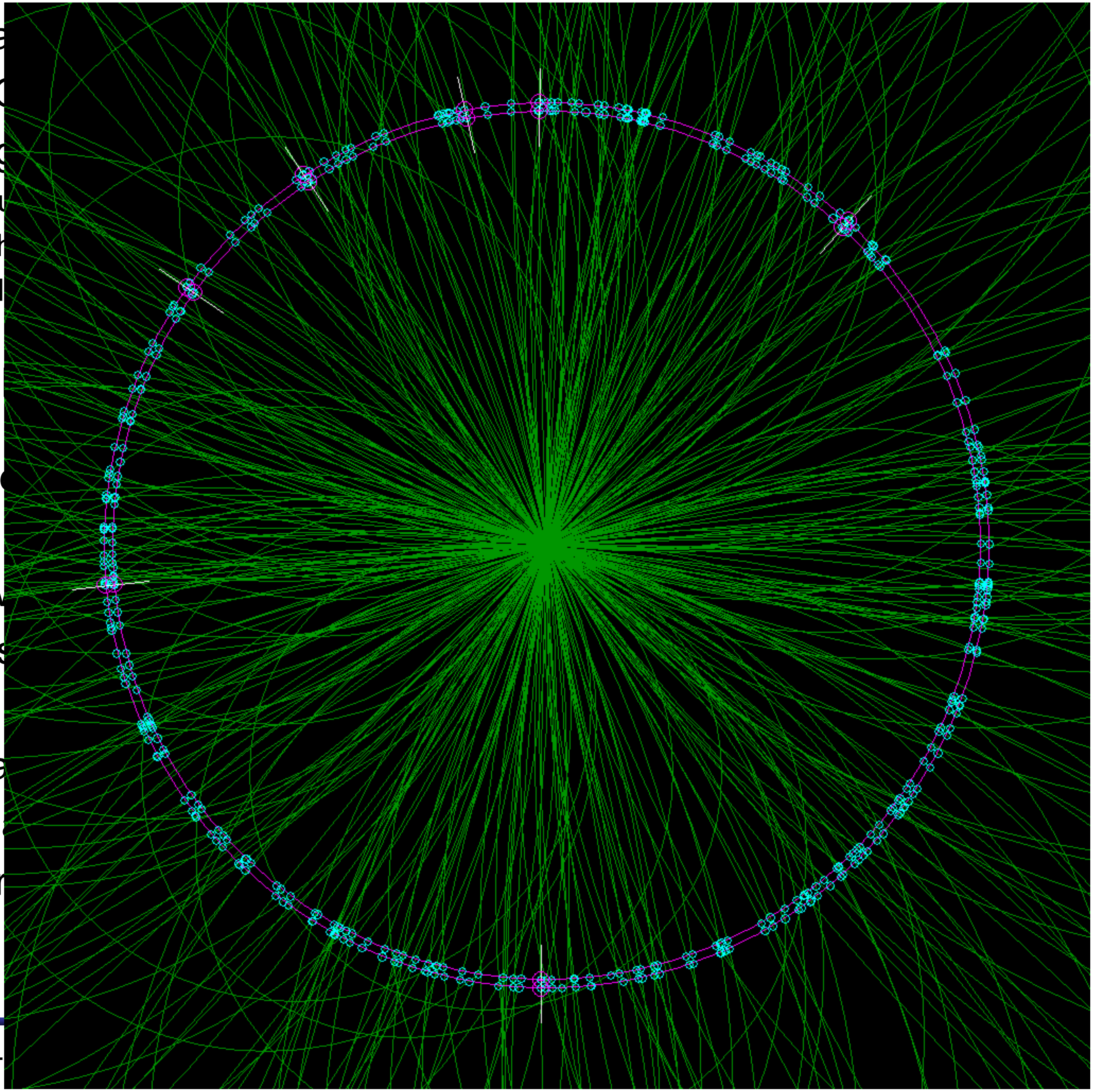
1 & 2-pixel search windov

Low and high comp. thres

Simulates detector overla

get an (over-)estim

Simulates online reconstr



How Big A Sensor Do We Need?

Length requirement comes from lack of information about z co-ordinate for IP

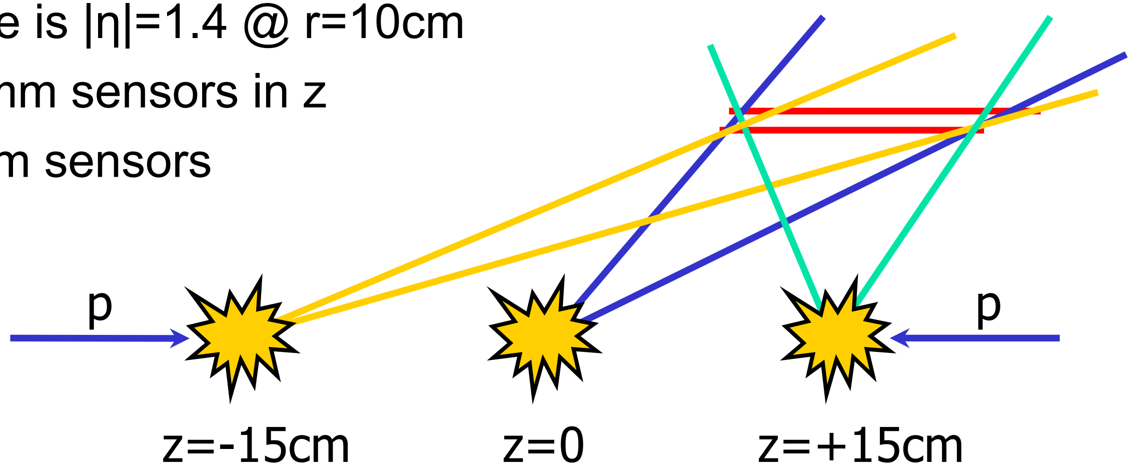
Determines required detector overlap (only when using correlation ASIC)

Effect is strongest in the forward region

Assume maximum coverage is $|\eta|=1.4$ @ r=10cm

For +-15cm, we need >7.2mm sensors in z

For +-8cm, we need >3.6mm sensors

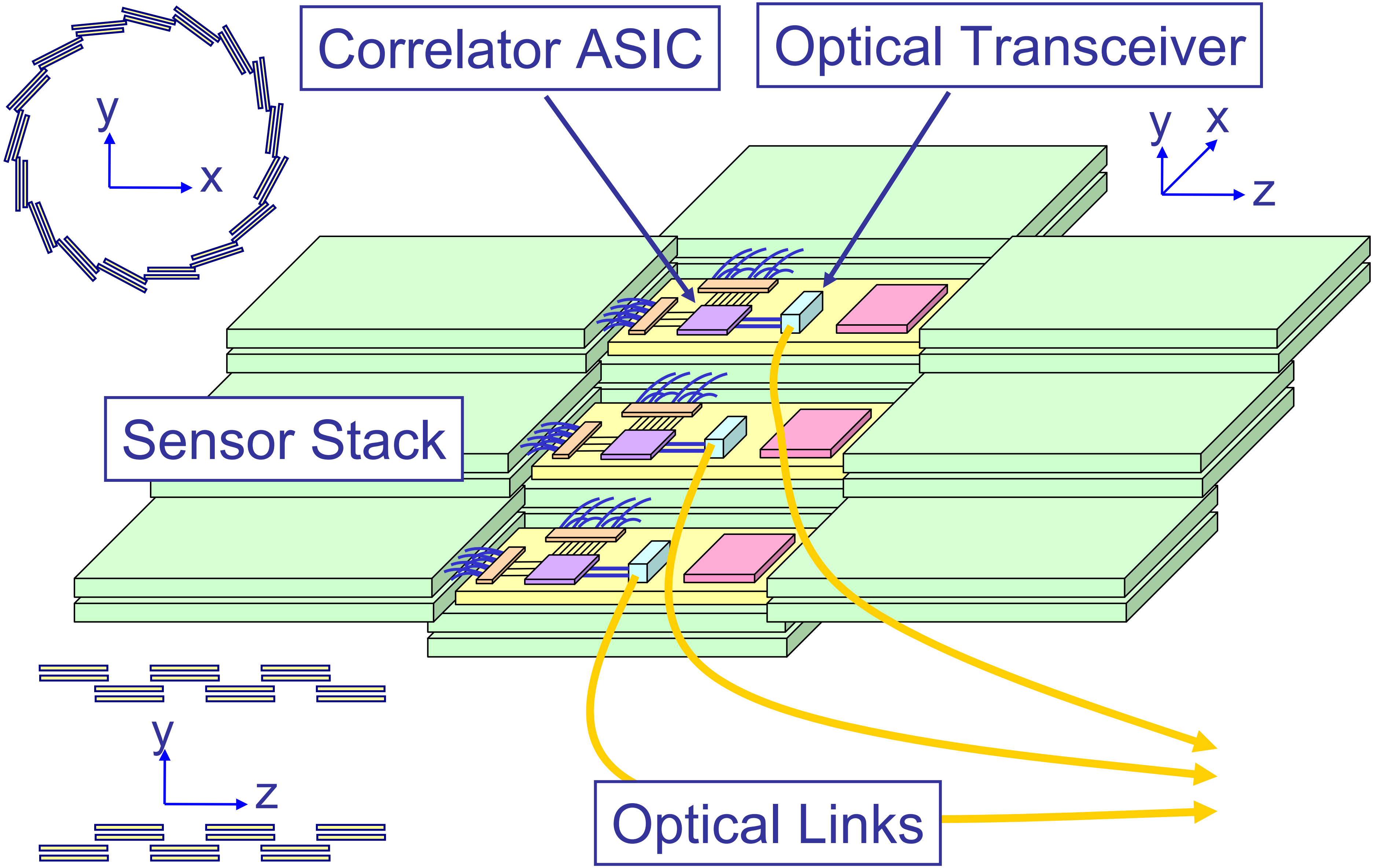


The larger the sensor, the longer the propagation delay

This is the real killer when designing a designing a Level 1 Triggering pixel system for SLHC (or LHC even)

How do we find the hits in 12.5ns and reset the pixels with minimal deadtime?

Conceptual Design



Getting A Handle On Trigger Rate…

- Not only do we want to reduce trigger rate at L1 due to hardware constraints…
- **…we also want to be able to trigger selectively**
- It is likely that we will use more complex (topological) triggers later in the physics programme
- Well we've used the ECAL (not to be replaced), HCAL (not to be replaced) and muon systems (possible upgrade), so what's left?

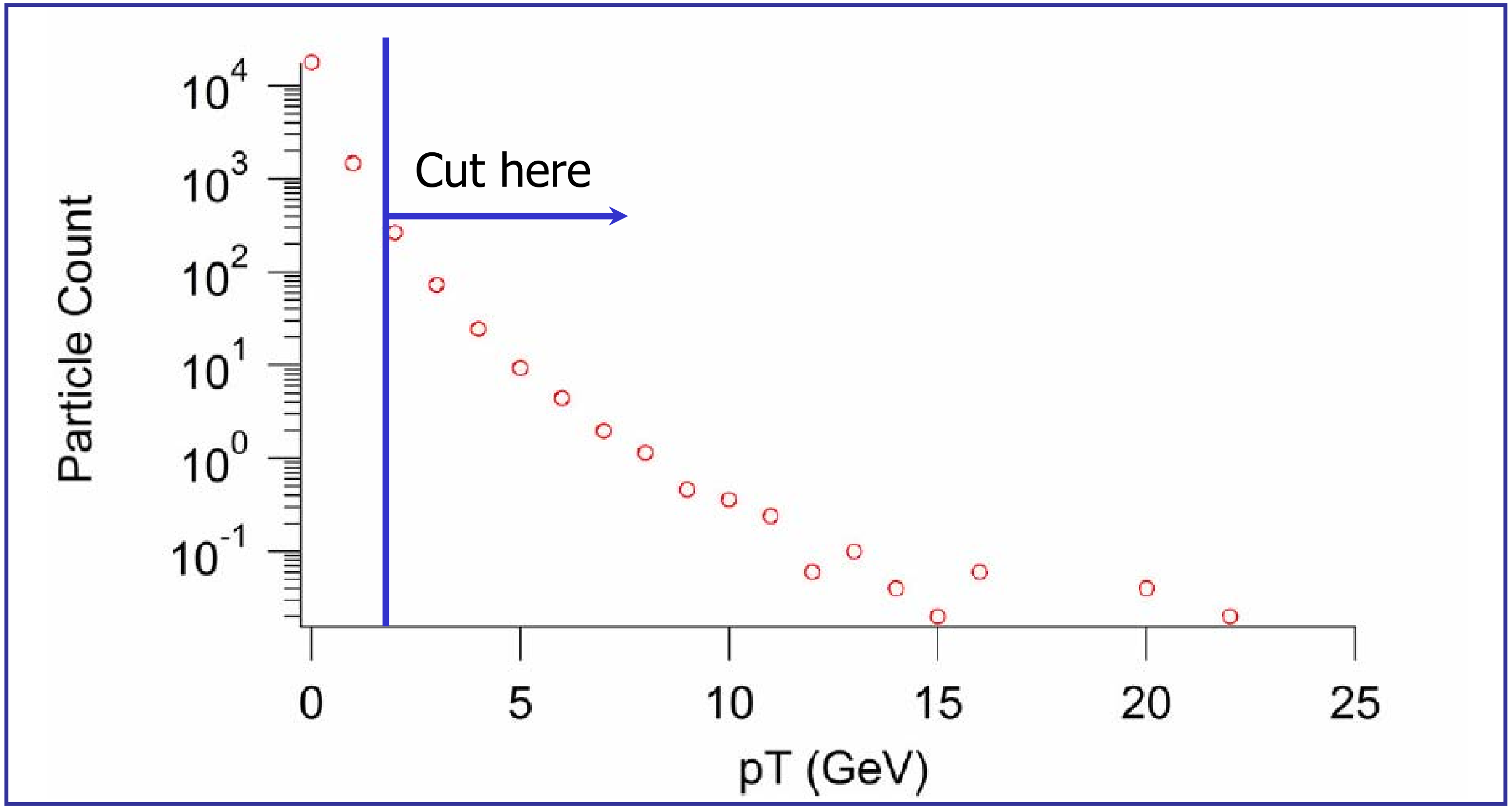
Tracker (Why Not? It won't survive anyway…)

  - **But why not before?**
  - CMS tracker is 12-barrel-layer analogue & all-Silicon
- Some physical limitations are:
  - Power – **30kW**
  - Cabling - **?? (and shared signal/power)**
  - Mass budget - **~1.4X_0 at worst**
  - Electronics performance - **Can we just build it first please??!!**
  - Radiation damage – **up to 30MRad, 10^{15}p/cm^2**
- Some triggering limitations are:
  - **SLOW**… - Kalman filter too slow, GSF even worse (and both are iterative)
  - Analogue readout makes high-speed processing impossible
  - Too much data to get out of detector (needs to be zero-suppressed)

- **So, we change the design…**

Tracker Data Rate & Charged Particles vs. p_T

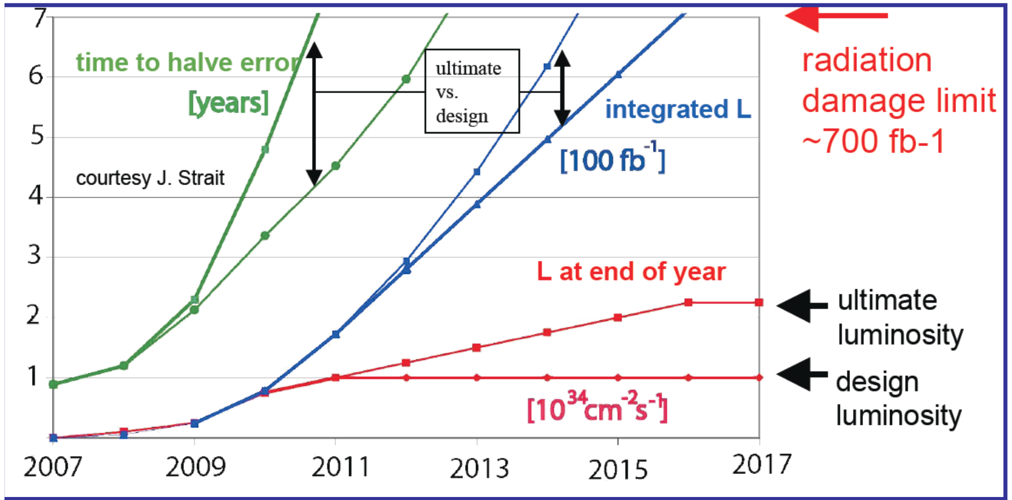
- Mean distribution of transverse momenta for charged particles at SLHC
  - Pythia 6.2772; 10,000 min. bias events via CMKIN 4.2, standard datacard
- By the time we cut at ~GeV, we've removed a lot of the background
  - Having said that, minbias doesn't include high-p_T leptons (and neither do **I**)
  - Leading order QCD is misleading, but close enough to demonstrate principle?
- Data rate in pixel layer (r=10cm) is **~5-20Gbit/s/cm² (!!!!!)**

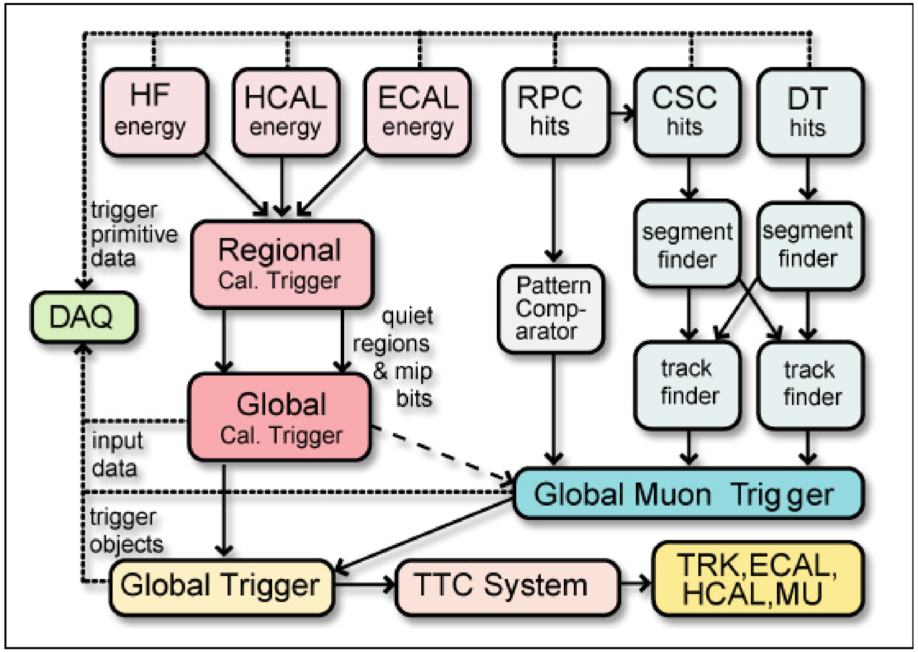


The CMS L1 Trigger

- Separate muon & calorimeter trigger systems feed a global trigger
- Expected final trigger rate ~**100kHz** at high luminosity LHC running (**$10^{34}cm^{2}s^{-1}$**)
- Current trigger primitives are:
  - Muons in chambers (with crude p_T)
  - Isolated photons in ECAL (or electrons – they look the same as there isn't a tracker)
  - Jets (with tau veto) – depends on number, isolation & clustered energy in calorimeter
- It is expected that this design will be able to 'handle' the current trigger rate **efficiently**

- It has been proposed that the LHC machine be upgraded to **$10^{35}cm^{2}s^{-1}$** after five years of running at high luminosity (~2015)





- **<u>What does this mean for our trigger?</u>**

Sensor Implementation Problems

- **Radiation Tolerance**
  - 100MRad & 2x10^{15} worst-case?
- **Speed**
  - All hits need to be identifiable within 25ns (preferrably 12.5ns)
  - Better if hits can reach periphery of chip within this time frame otherwise need in-pixel time-stamping and complicates readout pipeline
  - Alternatively each pixel needs a small buffer & overflow handling
  - Design should probably be **asynchronous**
    - **Not as mad as it sounds**
    - **A large part of the current CMS pixel detector is already asynchronous and running at > 3GHz**
- **Power**
  - Would be nice to aim for similar power budget to current pixel ROC
    - << **40μW/pixel**
- **Complexity**
  - In pixel electronics is limited by space & fill factor in some cases (MAPS)

Power Consumption (ESTIMATE)

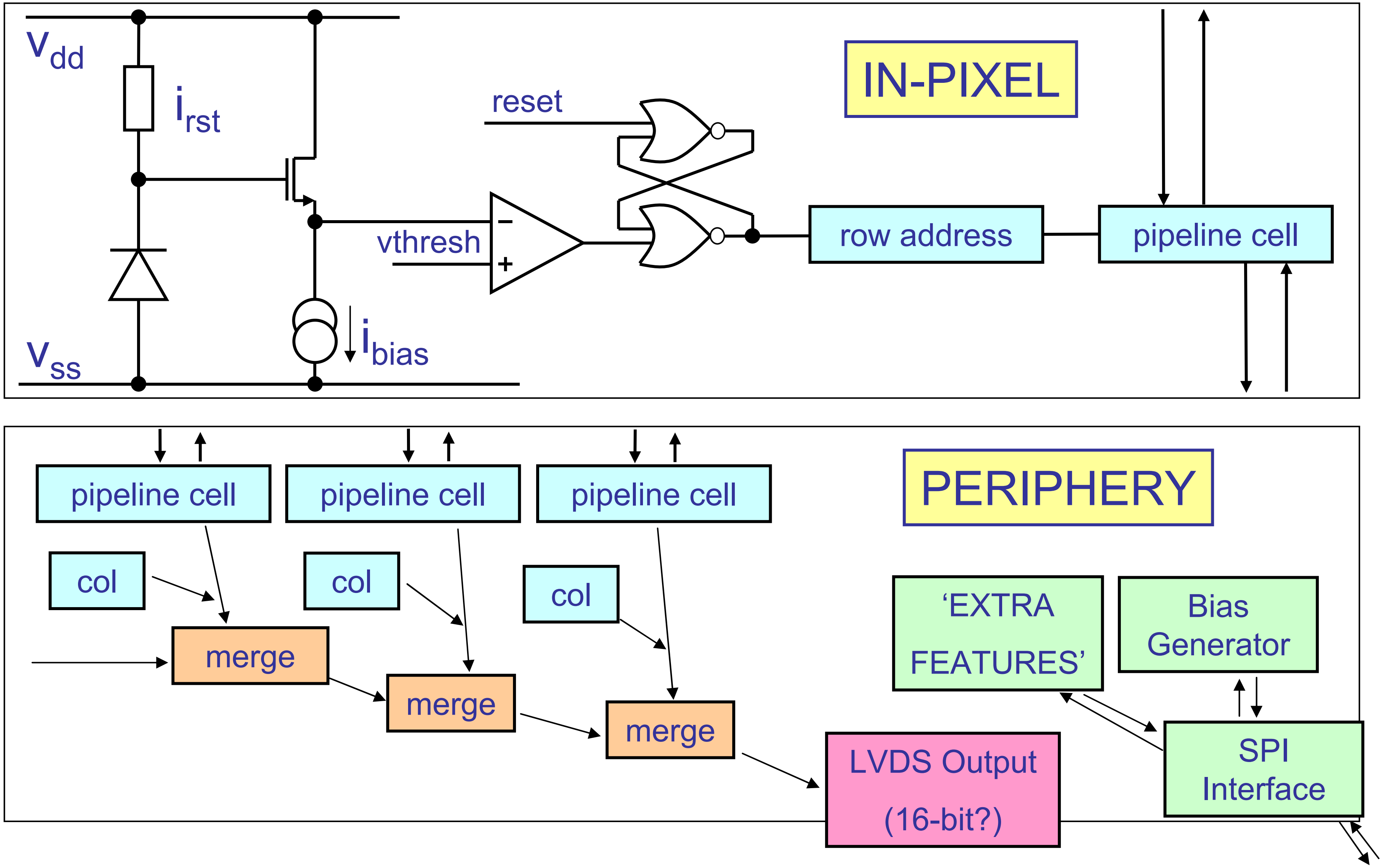
Module	Single Layer (No Correlation)	Stack (Correlation)
Optical Driver	1W(10G)*4562cm^2=4.5kW	4.5kW/50=90W
Pixels (20x50)	10μW/pixel*4562cm^2=4.5kW	11.4kW
Pixels (20x200)	10μW/pixel*4562cm^2=1.13kW	1.13kW
Pixels (40x150)	10μW/pixel*4562cm^2=0.75kW	0.75kW
Correlator	N/A	<< Pixel sensor (but I don't know)
TOTAL	**~12kW (2 layers)**	**~4kW? (2-layer stack)**

Power consumption of pixel sensor is largely dependent on in-pixel comparator?

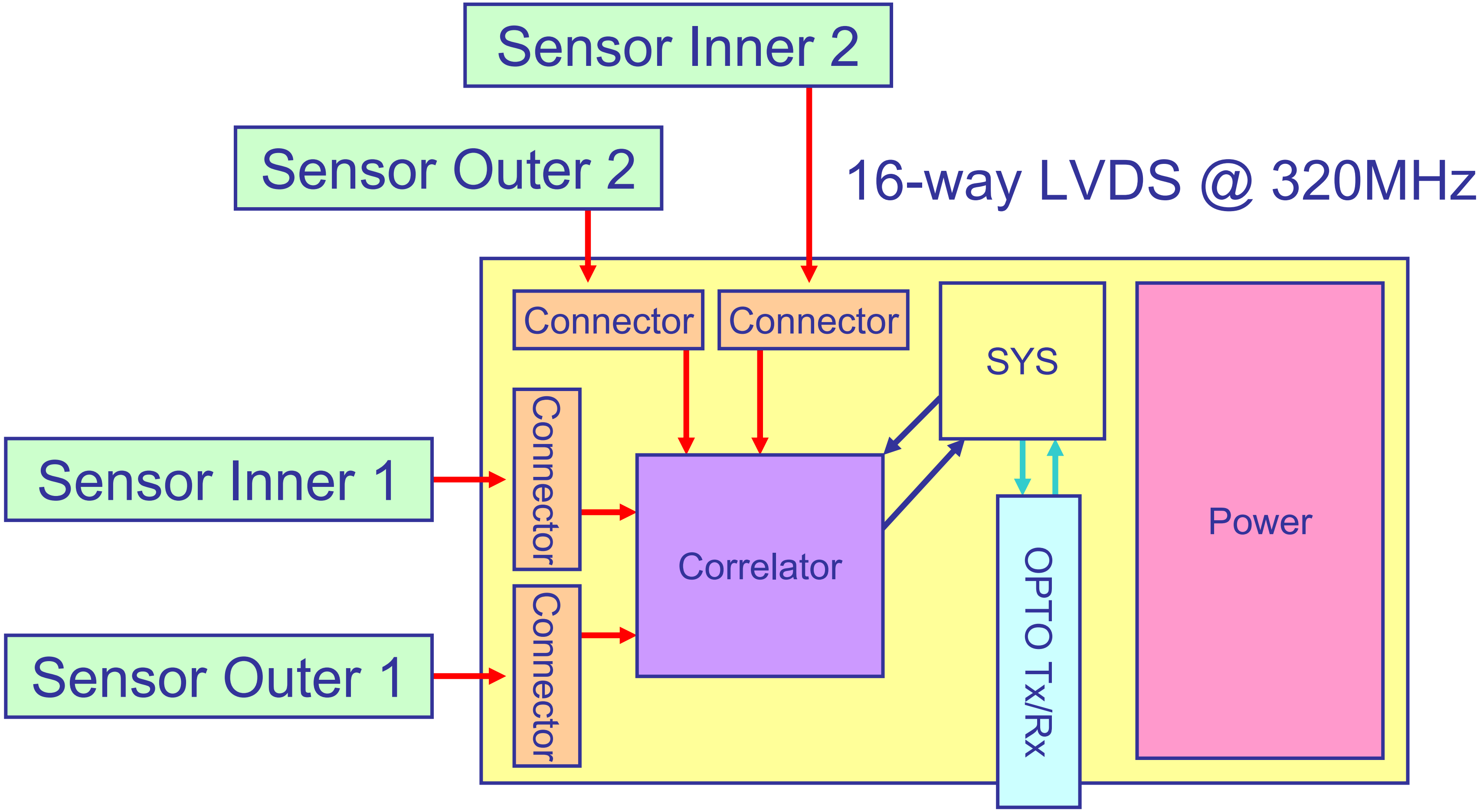
High-speed laser diodes consume a lot of power?

Correlator shouldn't consume a lot of power
I assume ~220mW / cm^2 here

A 'Straw Man' Module (II) – Pixel Sensor (CRUDE!)

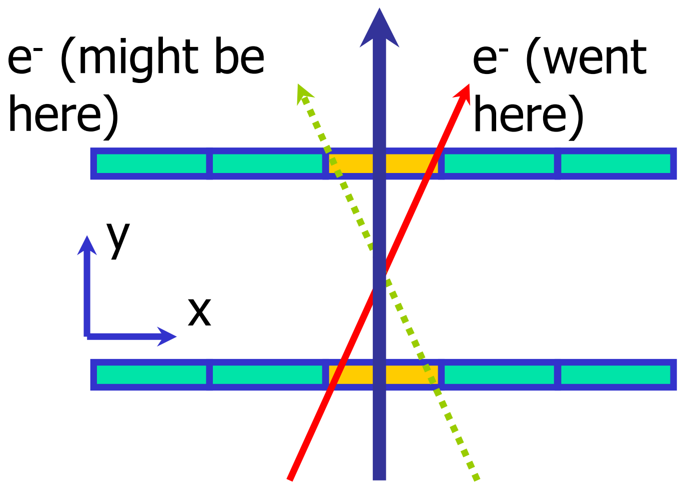


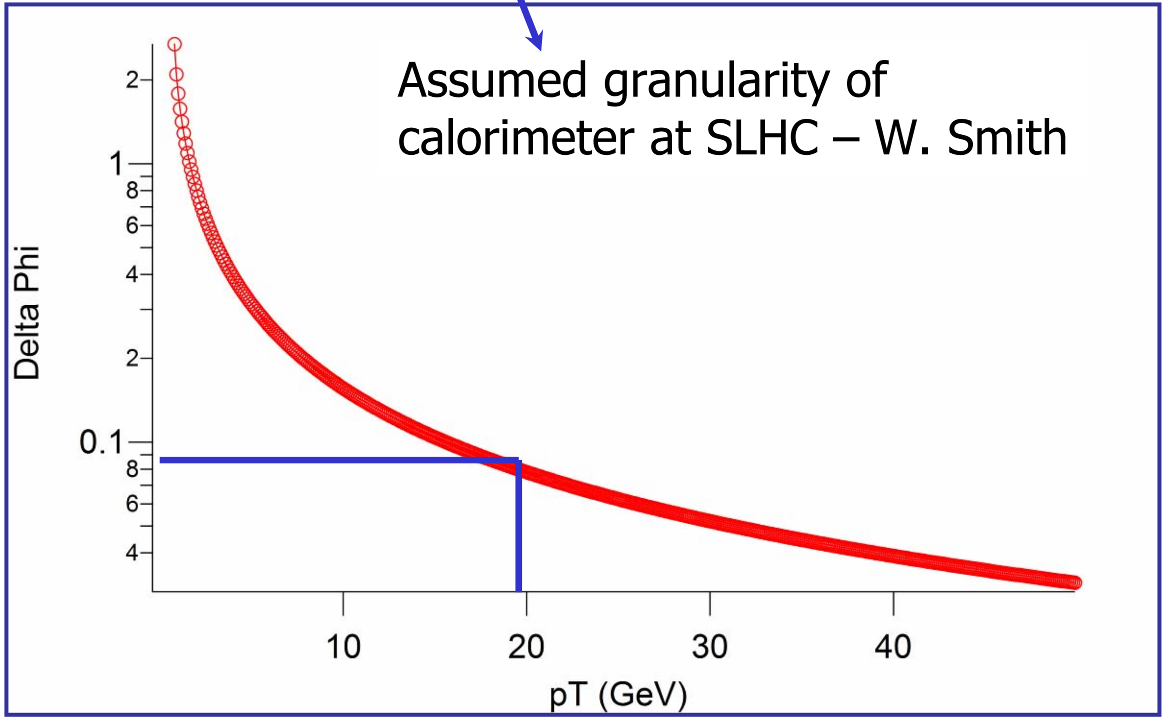
A ‘Straw Man’ Module (III) – Support Board



Worst-Case Resolution in φ

- Ignoring track curvature (for a moment), worst case resolution is as follows
- Layer sepn. ~1mm, pitch 20 microns, r=10cm
- Distance to ECAL ~1.3m
- Worst-case error is ~20 microns * 1.3 / 0.001 = 2.6cm
- Or $\Delta\varphi$ ~ atan(0.00002 / 0.001) = 0.02 rad (good enough)
- BUT – lack of p_T information is more important – **only <0.087 for p_T > 18GeV**





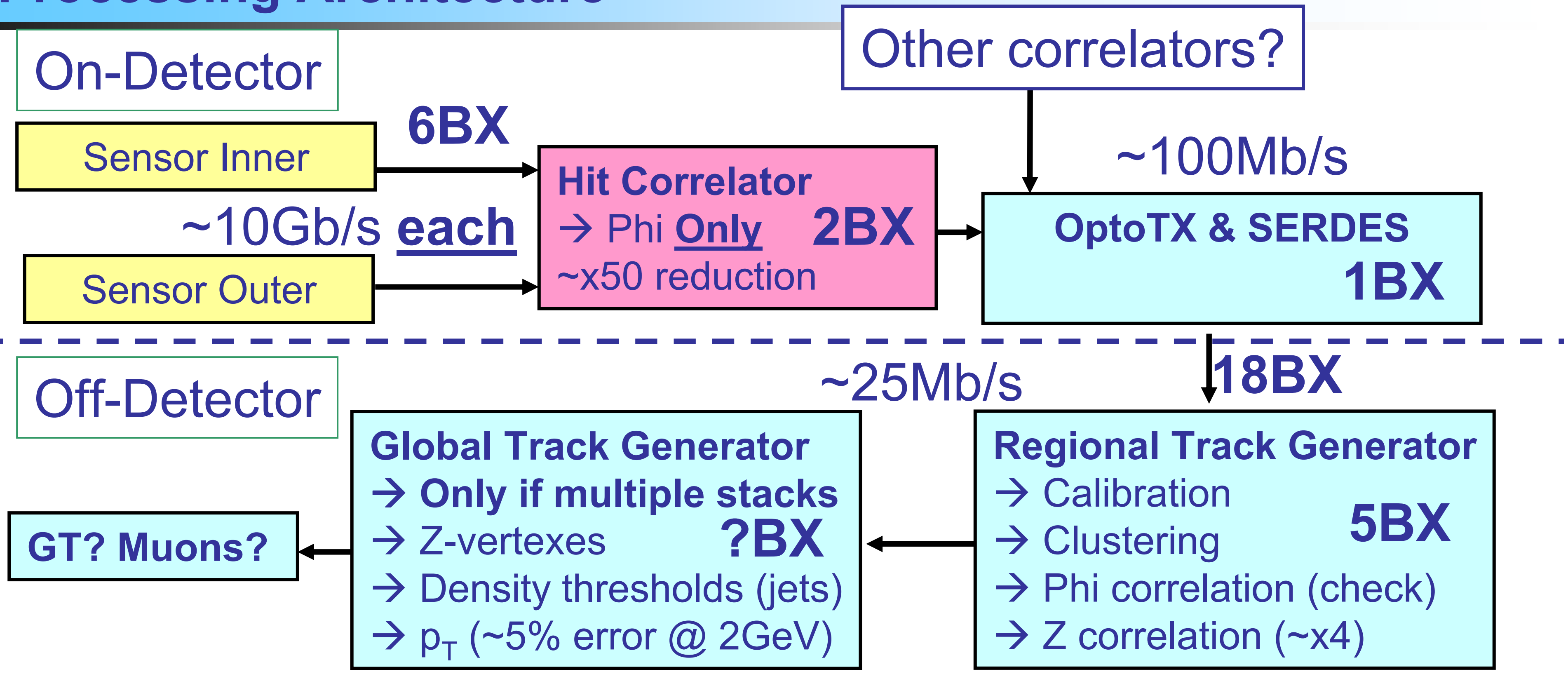
‘Hard’ Requirements and Investigations

- **I’ll leave the technology choices to the other discussions…**

- **Close to 100% fill factor is highly desirable for a pixel detector in CMS**
  - Is MAPS suitable? Will fill factor reach an acceptable level?
  - Can hybrids be used for this approach?
  - Will TFA become standard?
- DSM should be sufficient for speed requirements (other technologies?)
- **In-pixel power requirement needs to be minimised**
  - Mostly power drawn by comparator?
  - It does not appear that correlator will use a significant fraction of the power

- Currently looking at ways of making the design more feasible
- Slower charge collection, preshaper and in-pixel comparator (e.g. 50ns)
  - Pileup becomes a (minor) problem, but possibly not a show-stopper
- Slower readout achieved by bunch tagging in-pixel
  - Readout cycle allowed to take > 1 LHC clock count
  - 4-clock hit buffer makes timing much easier
- Lots of parts of this can be adapted/reused from current CMS pixels / other projects?

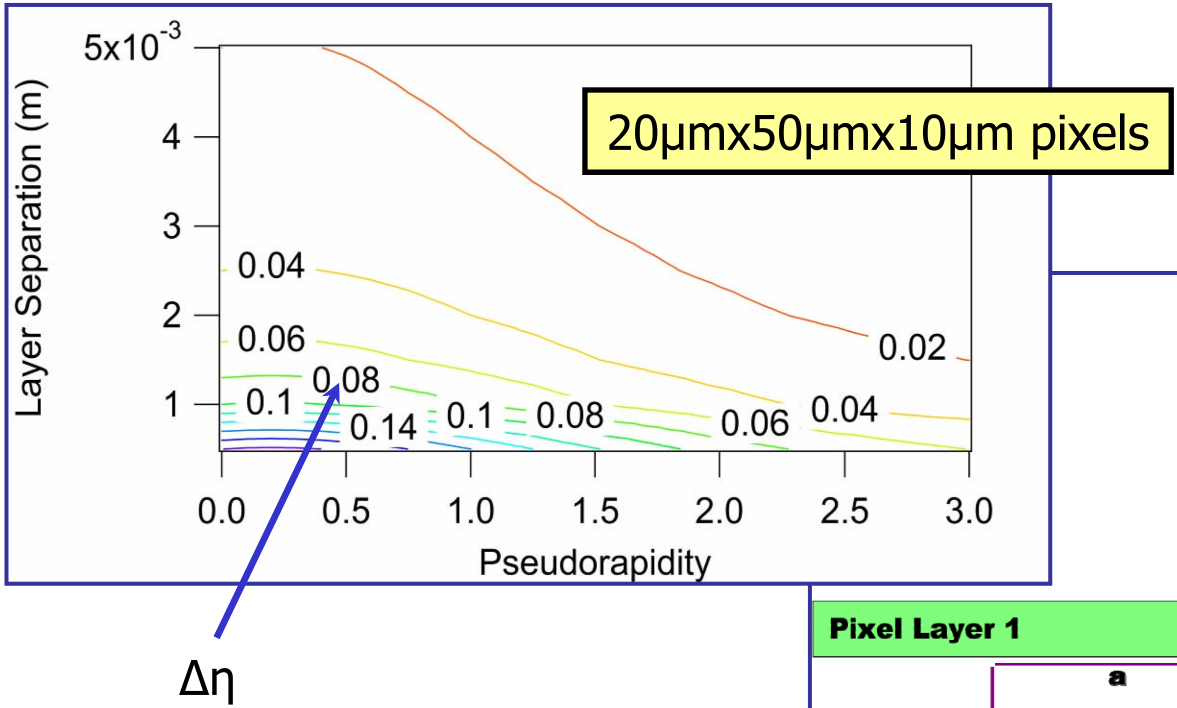
Processing Architecture

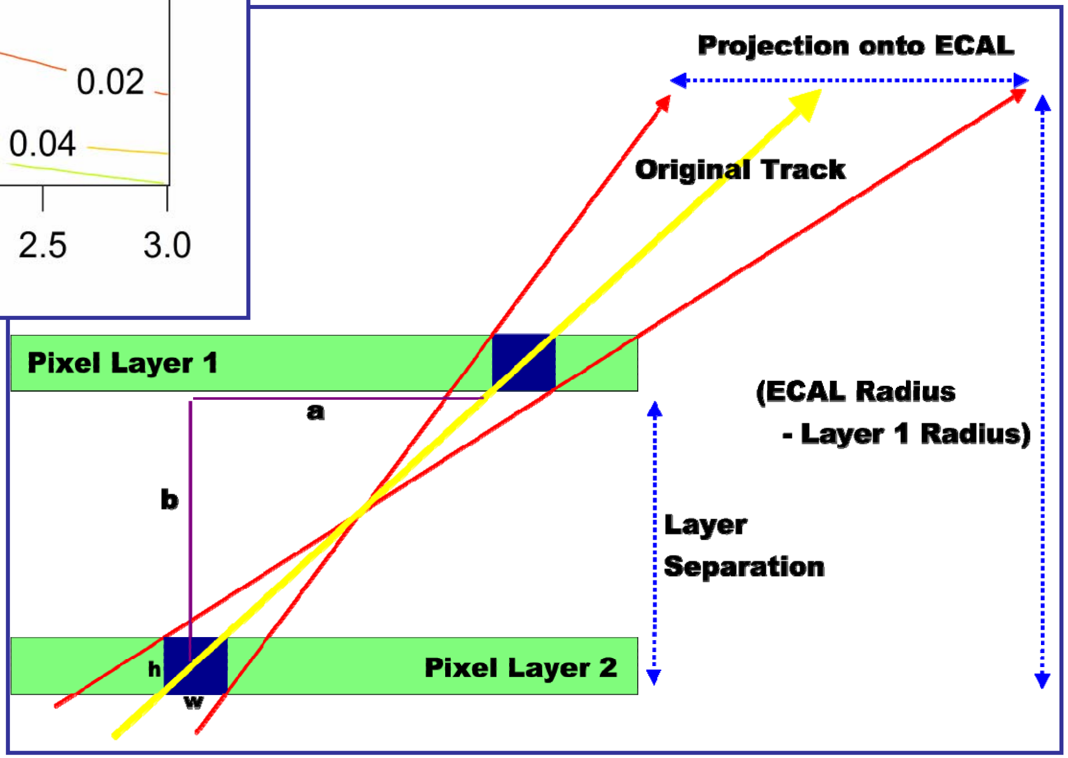


- **Recent result: Reconstruction algorithm implementation at IC**
  - **B. Constance & K. Zhu**
  - 1 stack uses **<1%** of an XC2VP70-7 @ 120MHz (unpacked)
  - Reconstruction latency (internal to FPGA) = **~3 BX ☺**
  - Extrapolating, need **~36 XC2VP70s** for a full system
  - Investigating in more detail…(can be optimised a lot) – assumes sorted hits

Worst-Case Resolution in η

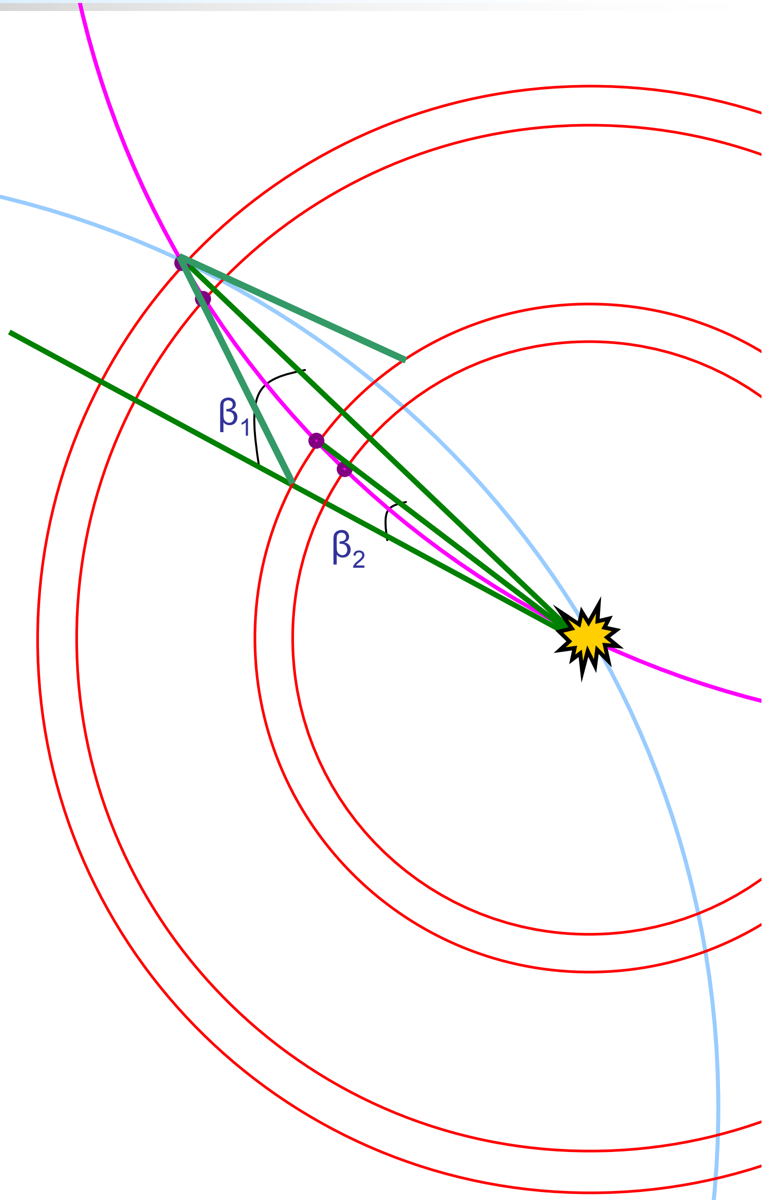
- Project range of possible track paths on to ECAL and show effect on Δη
- Can be made roughly equal-size to current calorimeter trigger tower

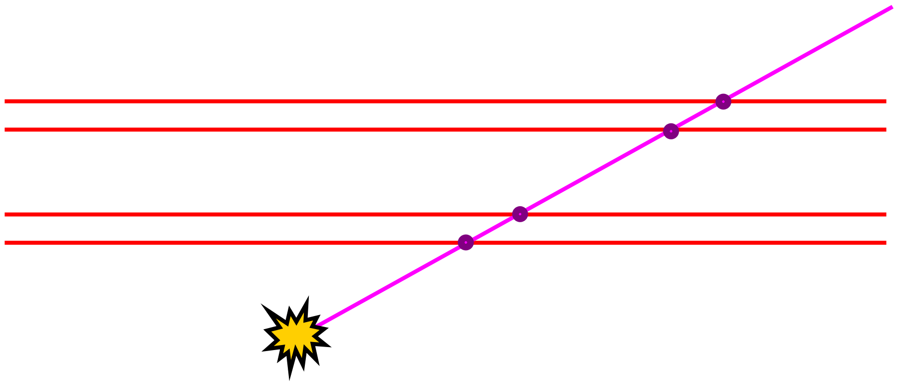




Double Stack Reconstruction

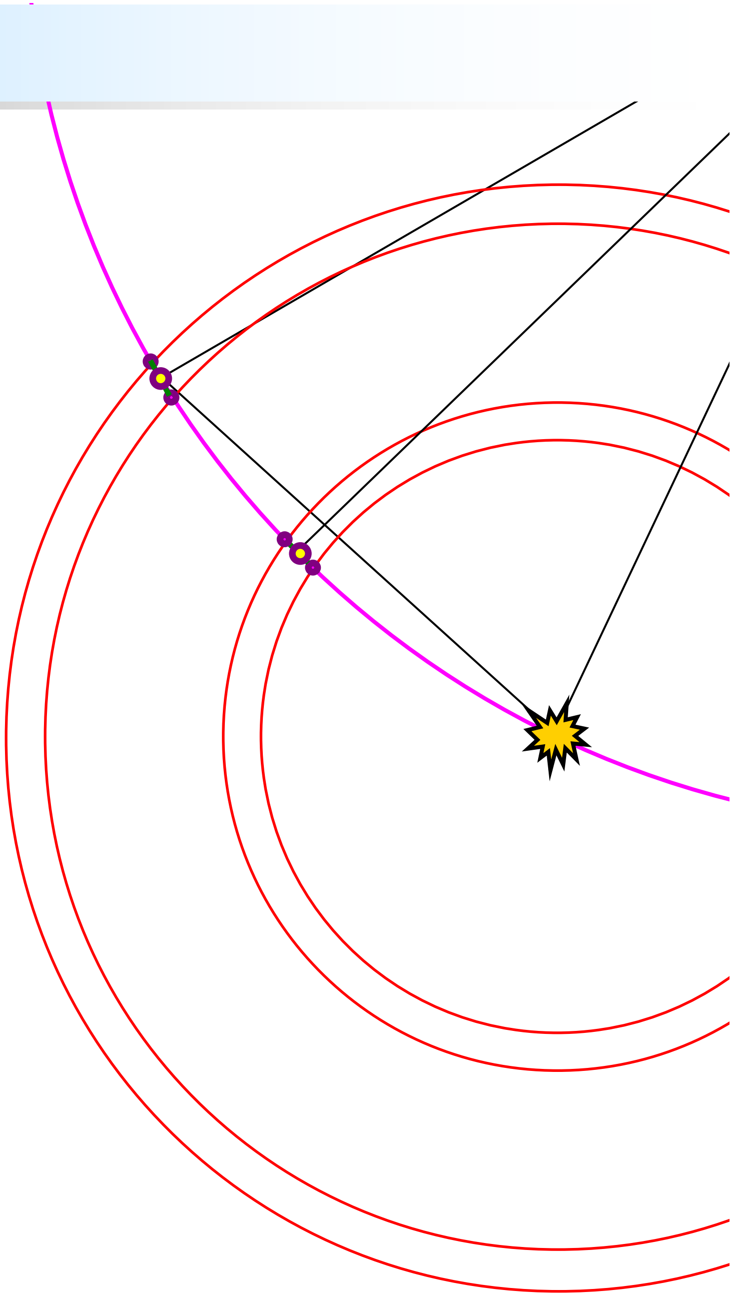
- Cut hits in each region individually
- Could match by binning in r/sin(β)
  - But β is related directly to α…
- **…intersection angle (α) not used due to limited d.o.f.s**
- **Project cone backwards from outer stack**
- **Can also use z-information**
  - **Also gives z-vertex of track**





Double Stack p_T Measurement

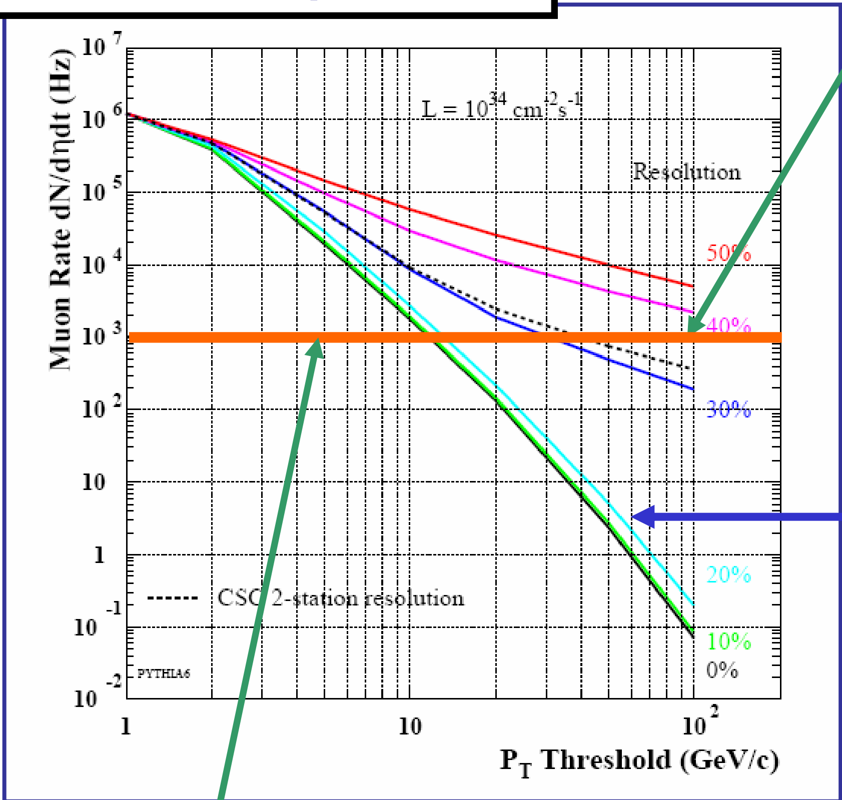
- Tangent itself doesn't give you much information
  - Throw it away… (after all that work! ☺)
- Use centre-point of each pair to measure sagitta
  - Calculate p_T in the usual way… (assuming r=0)
- Should give p_T up to 100GeV (50% error)
  - Only back of envelope calculation (so far)
  - Study underway
  - Gets better at low p_T
- Can be used for low-p_T (1-2GeV) jet tracks?
  - Is this important?

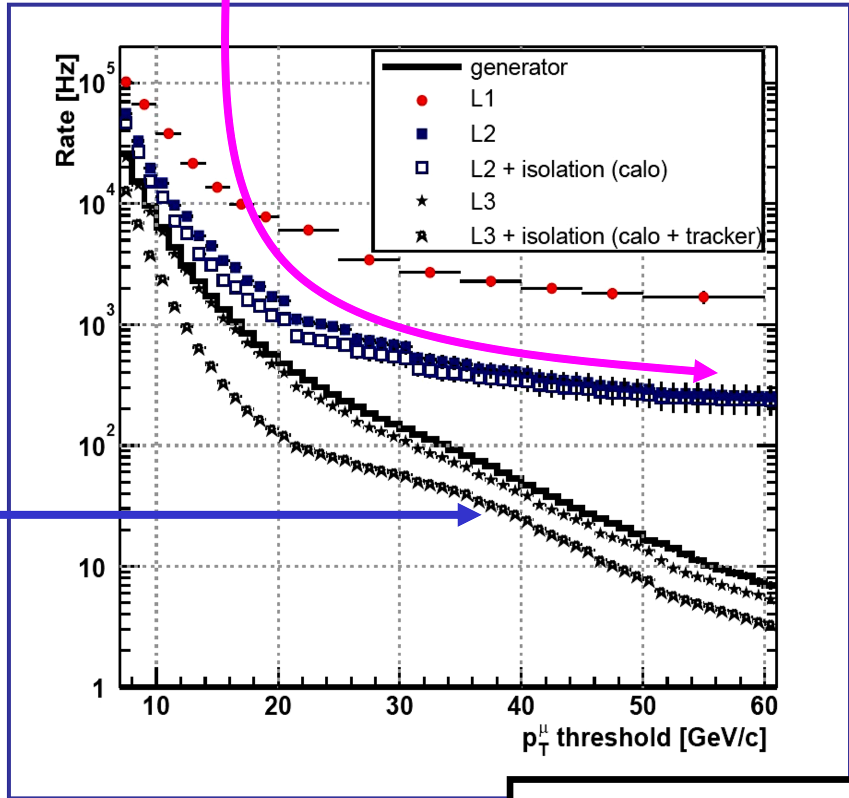


Muon Triggering

S.M. Wang, D. Acosta, CMS IN 2000/026

→ Note reduced resolution @ higher p_T
→ Reduces effectiveness of threshold





CMS DAQ TDR

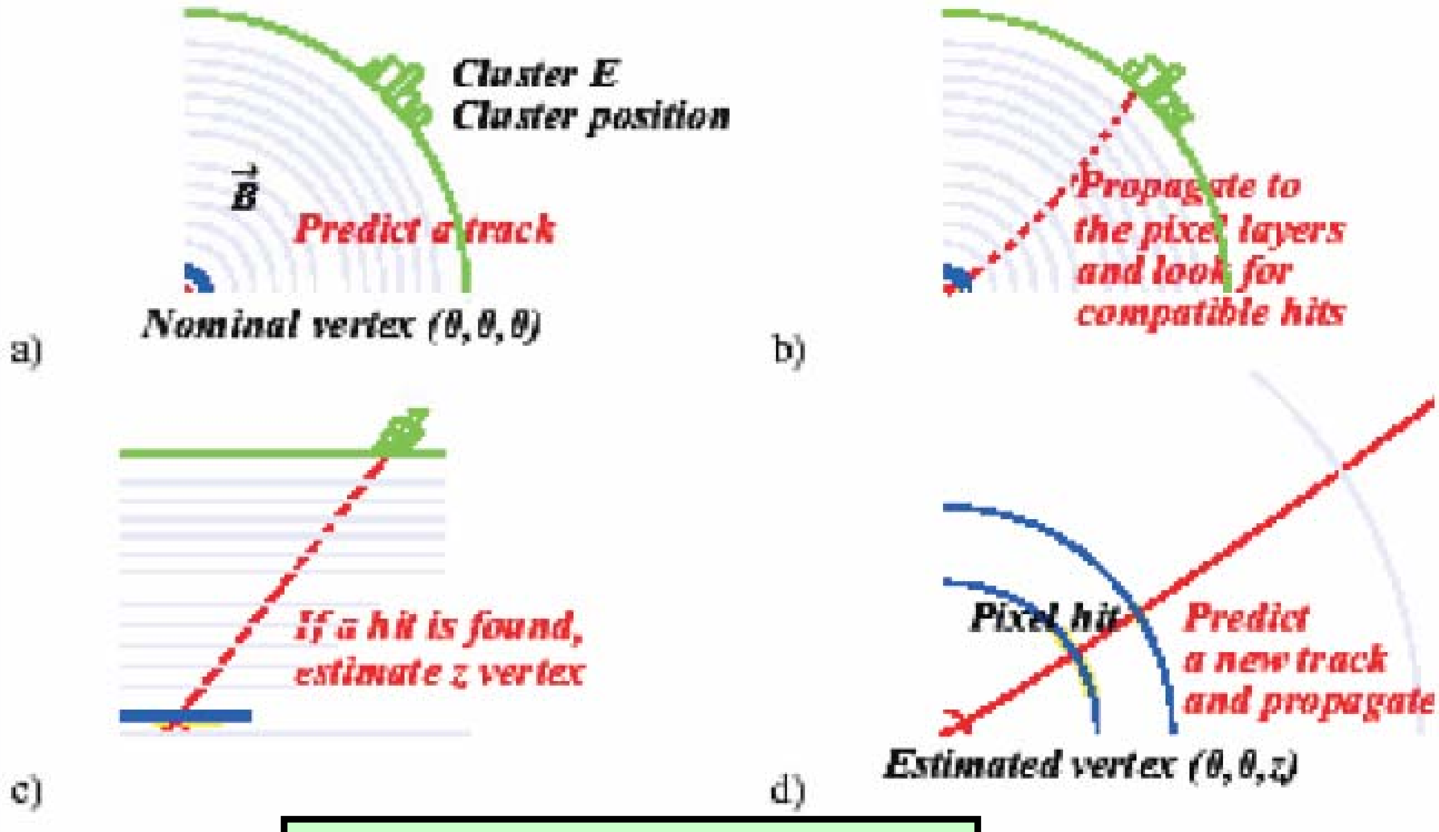
We need to do better than 30% to keep L1 trigger rate down

Tracker information gives us extra resolution we need

Calorimeter Electron Triggering

C. Seez

Gives x10 rejection with only pixels (x30 with outer tracker as well)

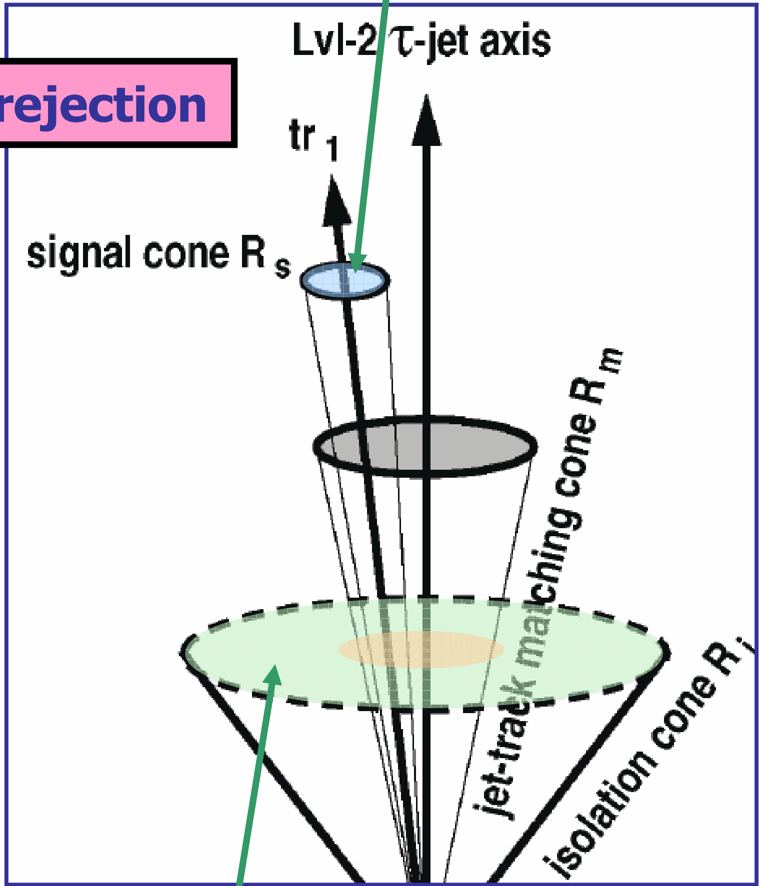


"It's an e^+/e^-, not a γ/π^0"

Calorimeter Jet Triggering

‘Hard’ track with p_T>40GeV/c here

Gives x10 rejection



No tracks with p_T>1GeV/c here
(0.087x0.087)

Data Rate for SLHC pixels @ r=10cm

- Pixel occupancy in SLHC ~4 hits / $(1.28\text{cm})^2$ @ 80MHz BX (or 8 @ 40MHz)
- Assume 20-bit pixel coding scheme (1024x1024 array)
- Base data rate is $80\times10^6 \times 4 \times 20 / (1.28)^2$ = 3.9 $\text{Gbit/cm}^2\text{/s}$

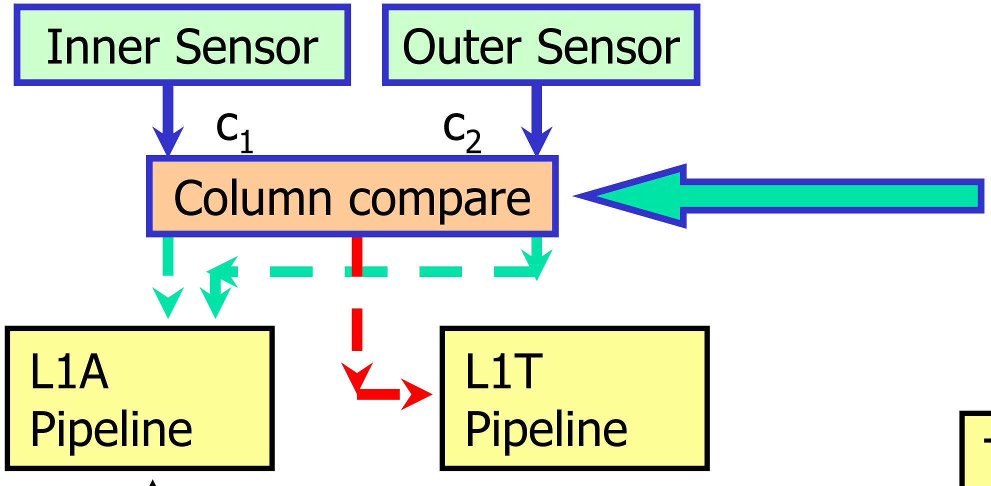
- **BUT** have ignored:
  - **Charge sharing → x2**
  - **Error correction on optical links (Hamming coding / 8b10b) → x1.25**
- Should also add a margin (let's say 20%) for e.g. data coding overheads

- 3.125 x 2 x 1.25 x 1.2 = **~12 $\text{Gbit/cm}^2\text{/s}$**

- I'm not even convinced this is the maximum that is possible, but still worrying

- Even assuming progression in optical link technology, this is tough to implement
  - Power, cabling, etc…..

Correlator Architecture



- If $c_2 > c_1 + 1$, discard c_1
- If $c_2 < c_1 - 1$, discard c_2
- Else copy c2 & c1 into L1 pipeline, next c1

This determines your search window
In this case, nearest-neighbour

At low luminosity, all hits could be read out
Put a ‘bypass’ switch in correlator

L1A pipeline: 512 BX @ 80MHz x 4 hits / $(1.28\text{cm})^2$
→ ~10kByte event buffer