



NEXTSILICON X  ODISSEE

DATAFLOW *INSTEAD OF VON NEUMANN ARCHITECTURE*

THE SOLUTION TO MOORE'S LAW DEMISE

> **ODISSEE 2026**



OUTLINE

1. Me
2. Moore's law
3. Dataflow
4. Summary

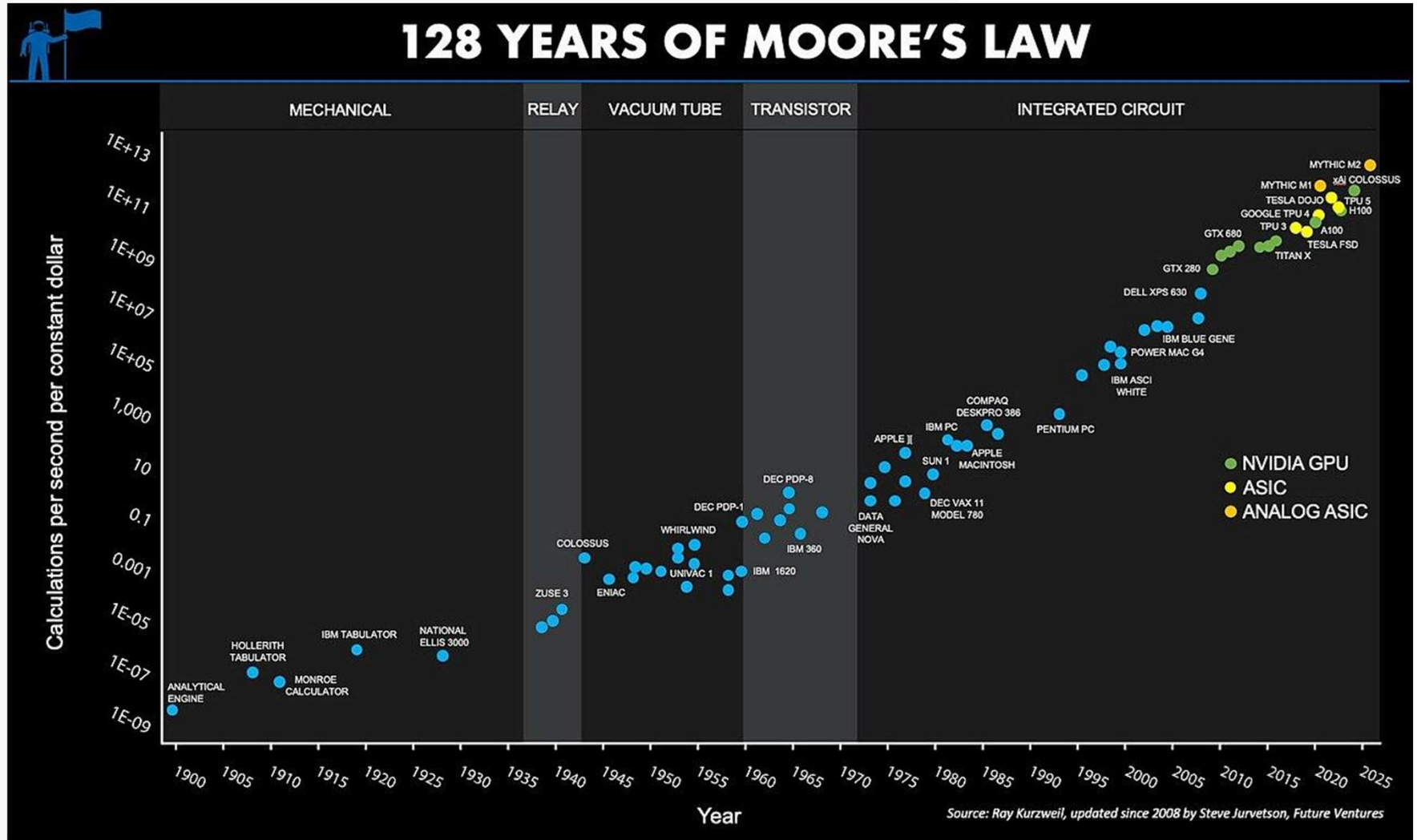
A RIDDLE

A hand-drawn purple arrow pointing from the text 'A RIDDLE' down towards the riddle box.

$$3*7 / 37 / 7*17^2$$



MOORE'S LAW



3*7 / 37 / 7*17^2

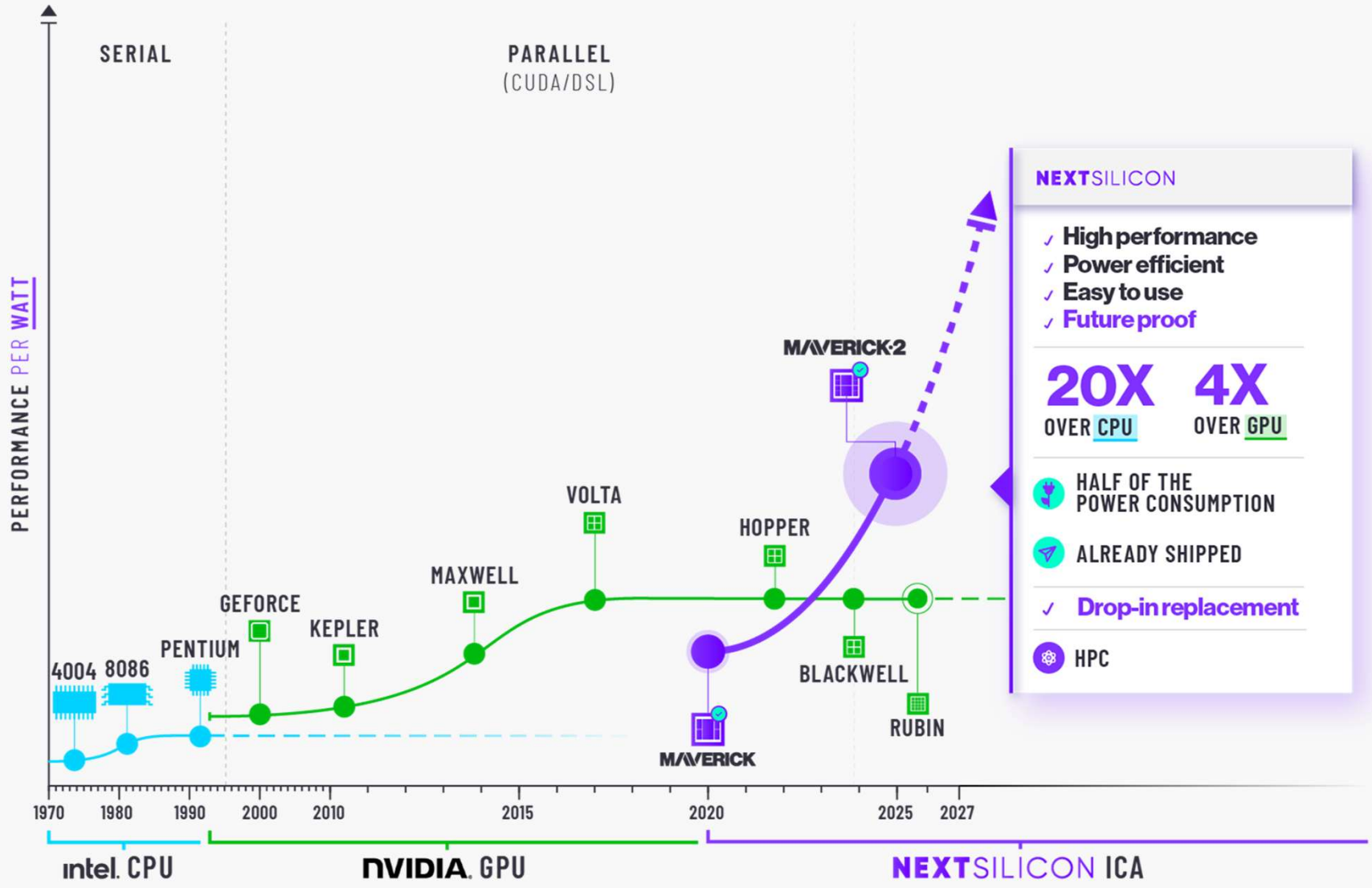


MOORE'S 2ND LAW

The number of people claiming
that **Moore's Law is dead**
doubles every 18 months



MOORE'S LAW PER WATT



3*7 / 37 / 7*17²



VON NEUMANN

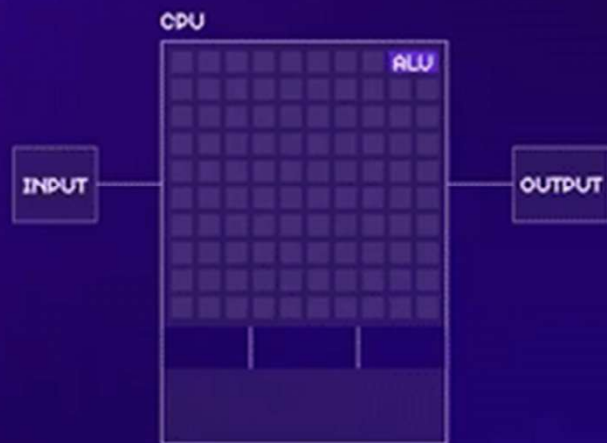
First Draft of a Report on the EDVAC by John von Neumann

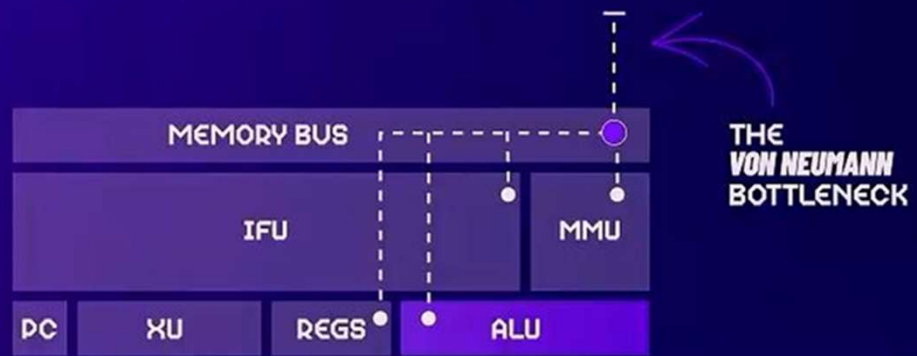
Contract No. W-670-ORD-4926
Between the United States Army Ordnance Department
and the University of Pennsylvania

Moore School of Electrical Engineering
University of Pennsylvania
June 30, **1945**

<https://bit.ly/VonNeumann1945>



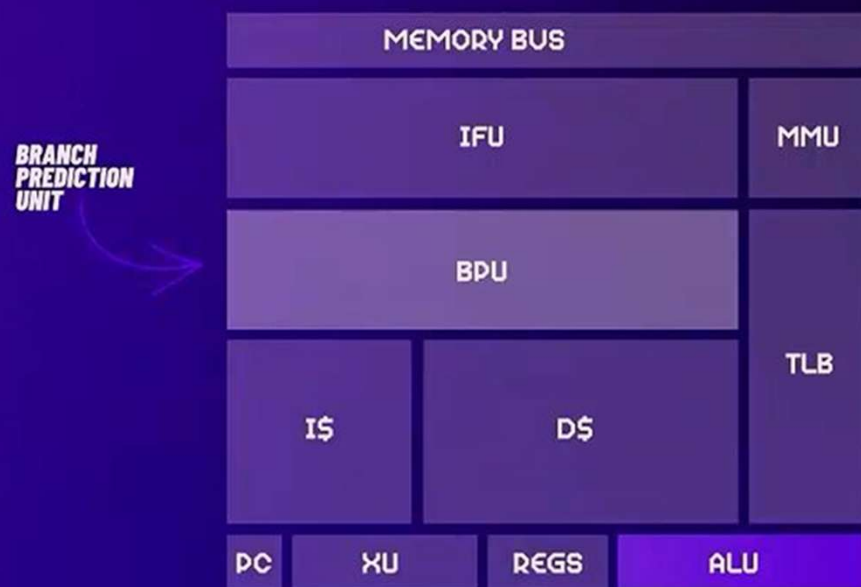




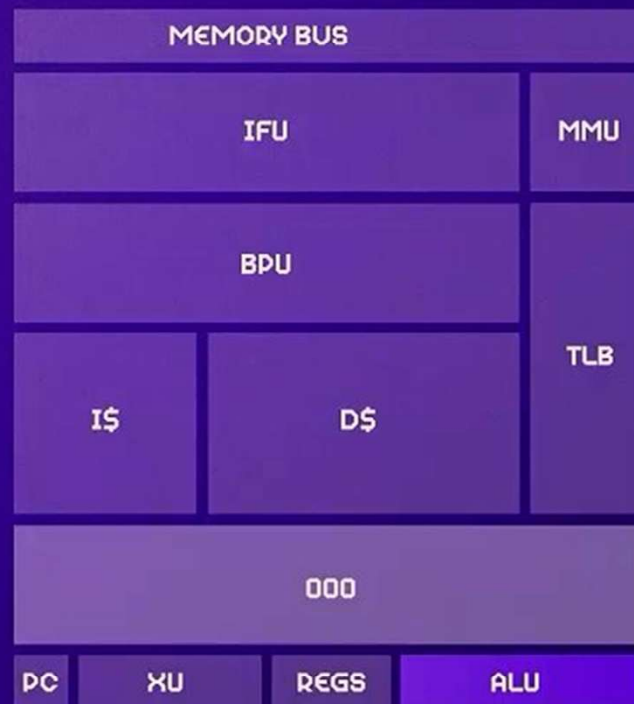
**INSTRUCTION
CACHE**







**OUT-OF-ORDER
ENGINE**



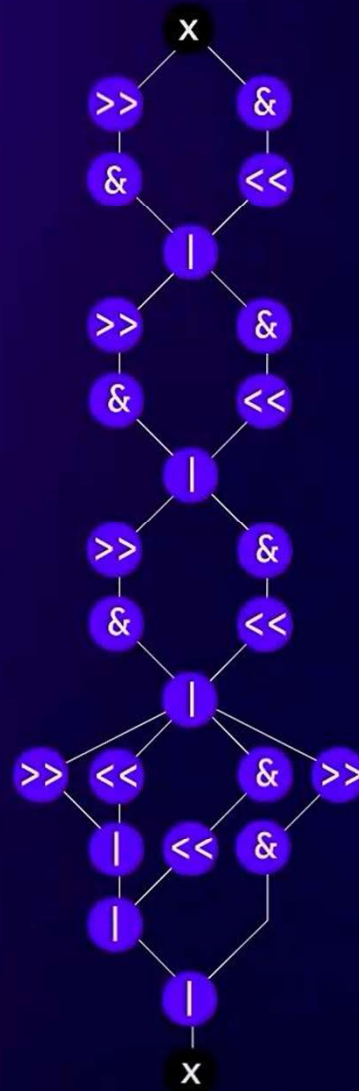
NEXTSILICON

DATAFLOW HARDWARE

COMPILING A FUNCTION

```
// Reverse the bits of the specified 32-bit word
unsigned reverse(unsigned x) {
    x = ((x & 0x55555555) << 1) | ((x >> 1) & 0x55555555);
    x = ((x & 0x33333333) << 2) | ((x >> 2) & 0x33333333);
    x = ((x & 0x0F0F0F0F) << 4) | ((x >> 4) & 0x0F0F0F0F);
    x = (x << 24) | ((x & 0xFF00) << 8) |
        ((x >> 8) & 0xFF00) | (x >> 24);
    return x;
}
```

COMPUTE
GRAPH



	ACTION	ADDRESS	VALUE
	MOV	r2	0x55555555
&	AND	r2	r1
<<	SHL	r2	1
>>	SHR	r1	1
&	AND	r2	r1
	OR	r3	r4
	MOV	r3	r4
	MOV	r2	0x33333333
&	AND	r2	r1
<<	SHL	r2	2
>>	SHR	r1	2
&	AND	r2	r1

INSTRUCTION
SET

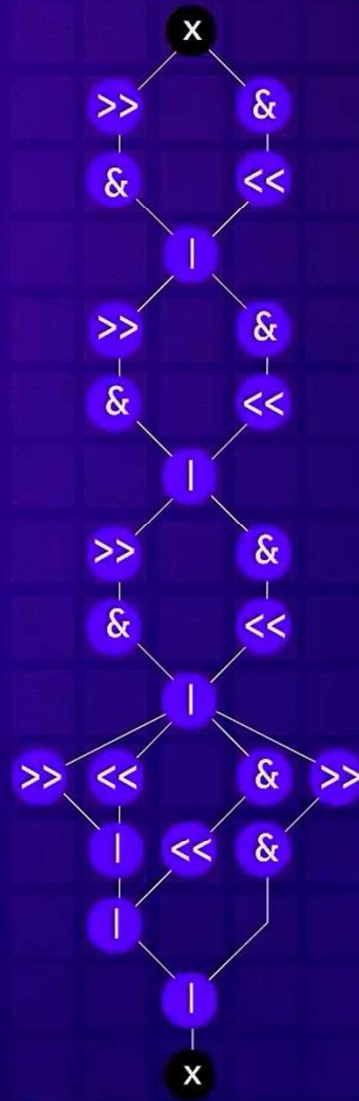


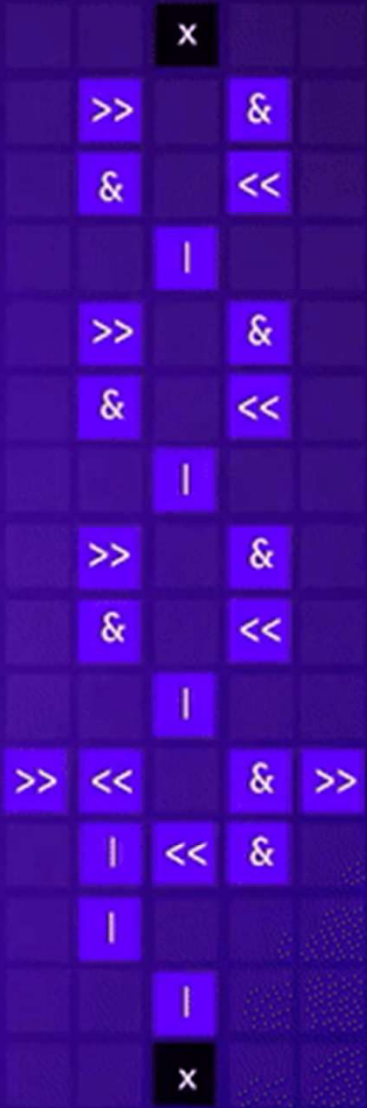
```
0110100101101011001001010010
& 0100110101001011001001000011
<< 1010110101001111001000110010
>> 1011010101001111001000011010
& 0110100101111011001001010010
| 0101110101001011001001000011
  1010110101001111001000110010
  0100110101001011001001000011
& 0110100101101011001001010001
<< 1010110101001111001000110000
>> 0110100101111011001001010011
& 1011010101001111001000011010
```

MACHINE
CODE

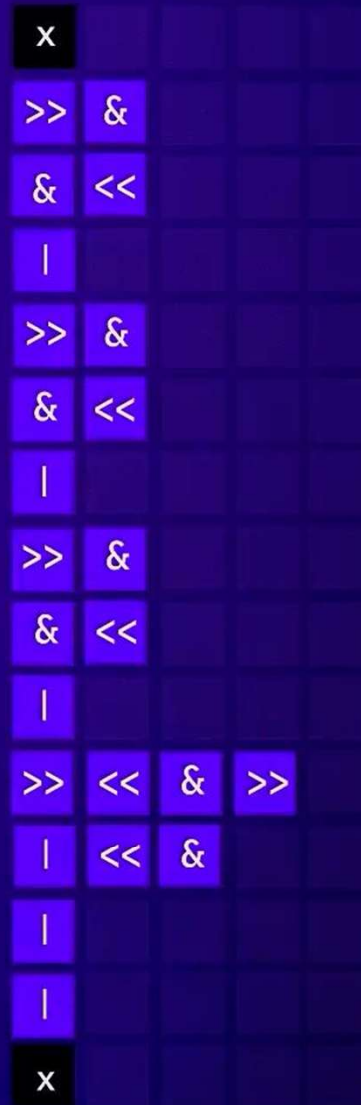


COMPUTE
GRAPH

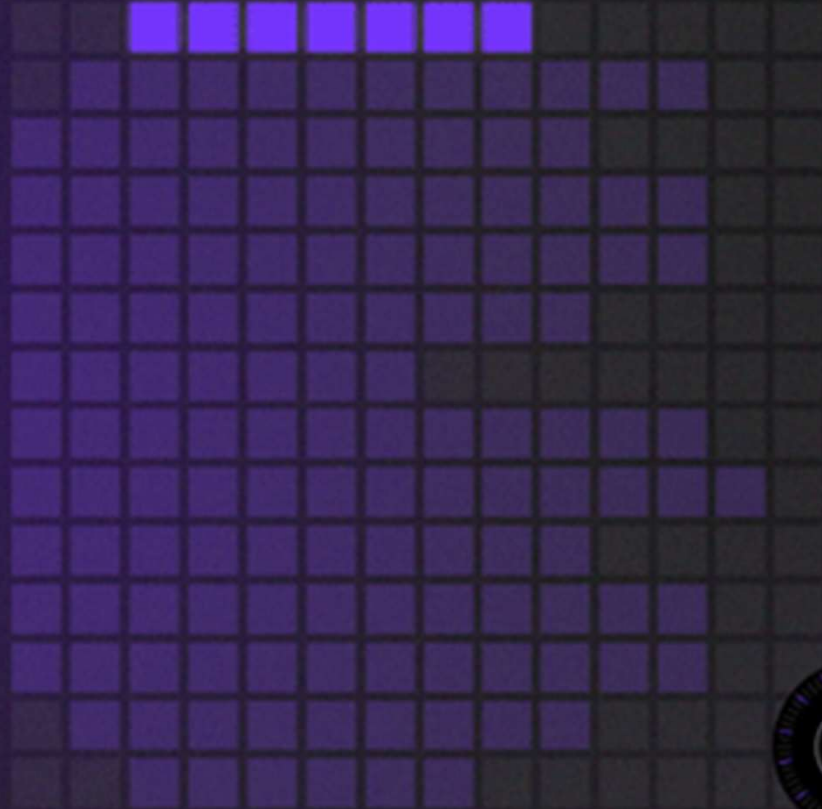




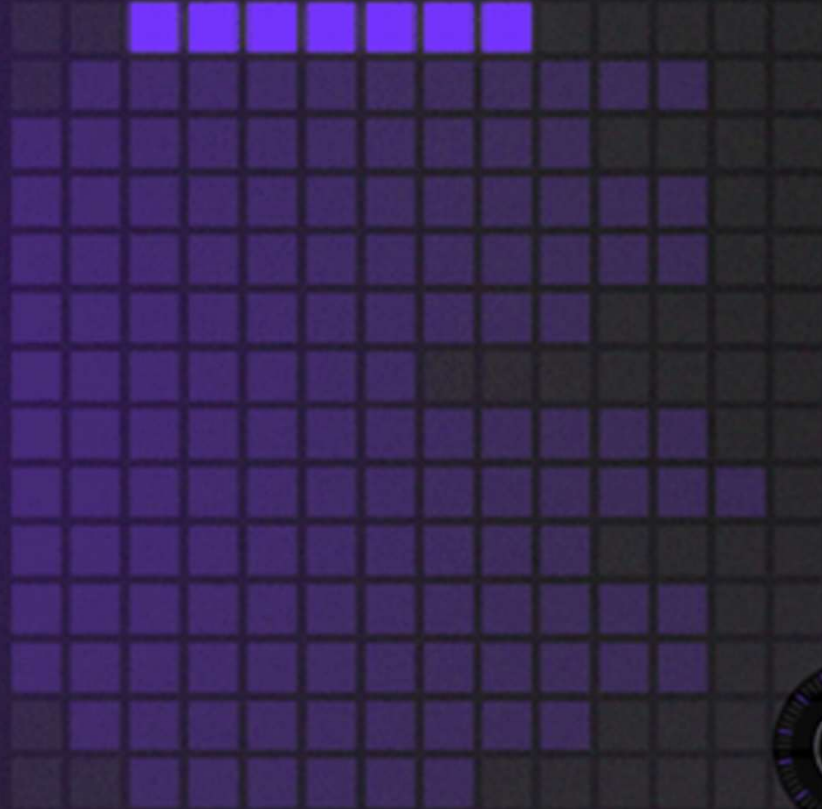
MILL
CORE



T1



T1



YOUR
CODE



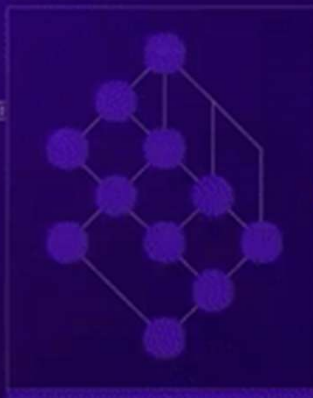
FAT BINARY

```
1 0 1 0
0 1 1 1
1 1 0 0
0 0 0 1
1 0 1 1
```

```
1 0 1 0
0 1 1 1
1 1 0 0
0 0 0 1
1 0 1 1
```

0 1 1 0 0

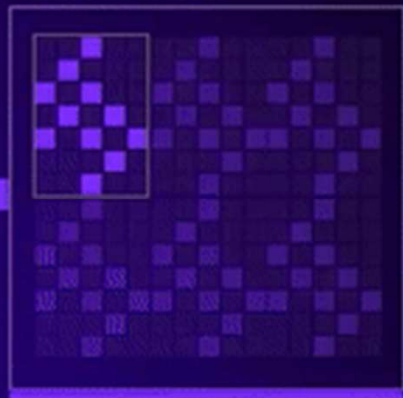
NEXTSILICON
OPTIMIZER



NEXTSILICON
MILL CORE



NEXTSILICON
COMPUTE BLOCK



0
0
1
1
0
0
1
1
0
0

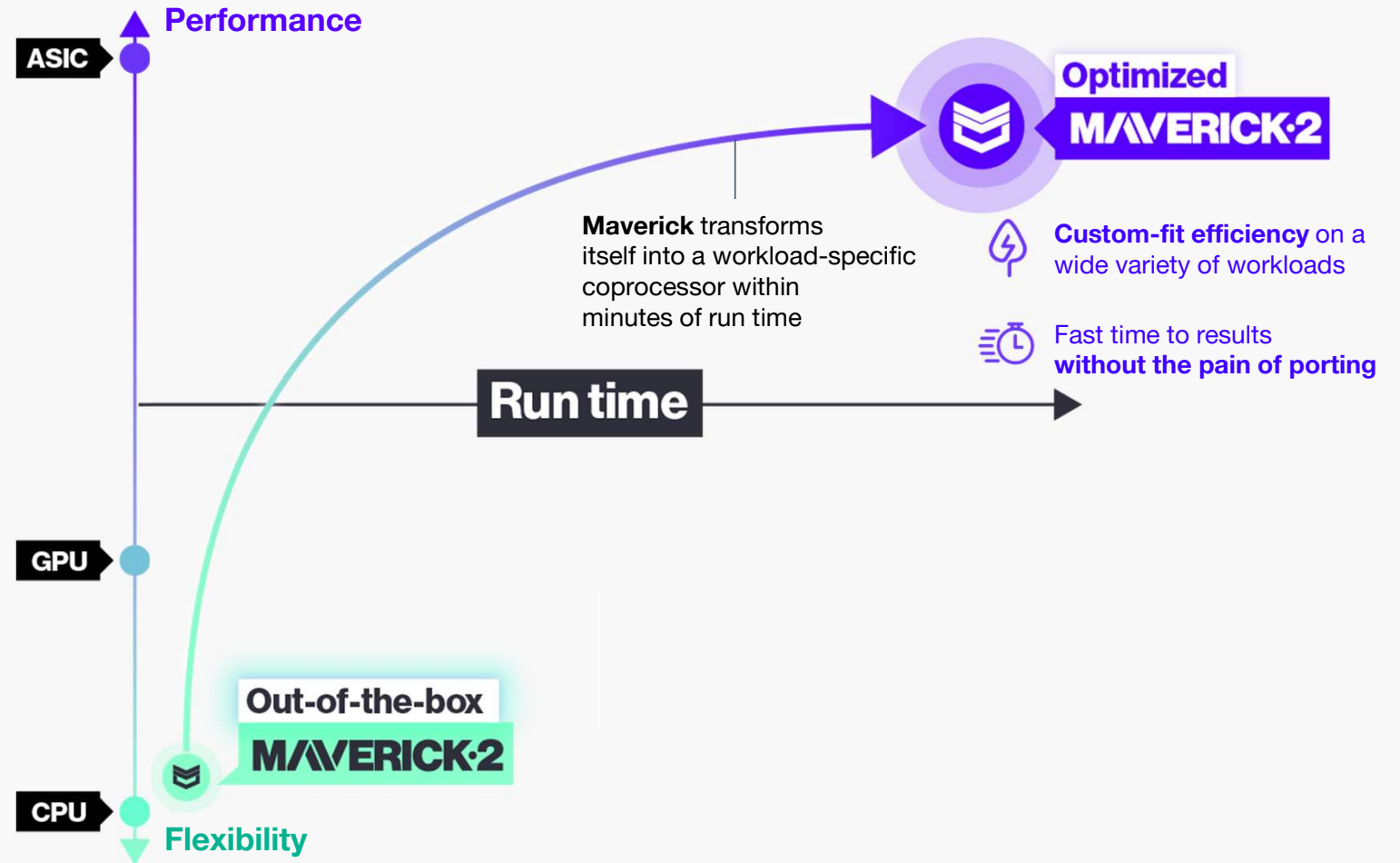
RUNTIME





PARADIGM SHIFT DYNAMIC COMPUTE

A compute platform that dynamically reconfigures itself in run time to adapt for the workload it executes





COMPUTE + NETWORKING

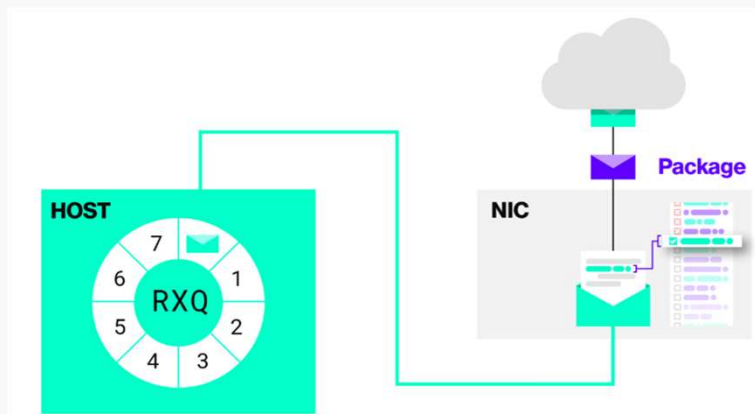
Goal: CPU + GPU + FPGA + NIC replaced with one NextSilicon device.

Raw performance:

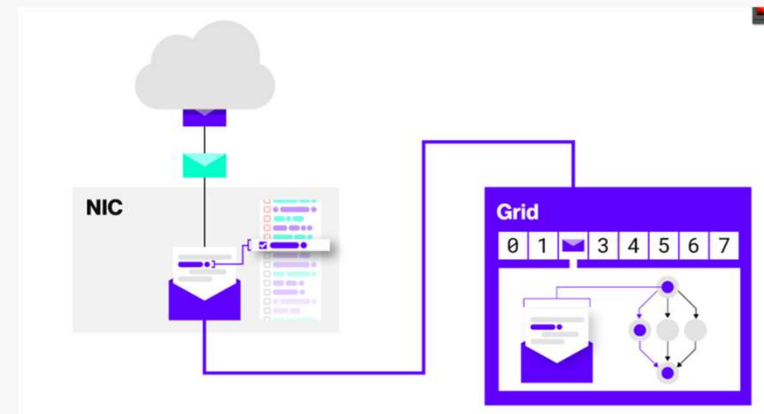
- Maverick-2 single-die: 1 port x 100Gb/s Ethernet
- Maverick-2 dual-die: 2 ports x 100Gb/s Ethernet
- Future products: more ports x faster Ethernet

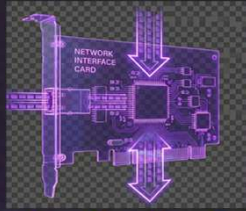
Key feature - packet processing offload:

Legacy: packet processing on the host CPU

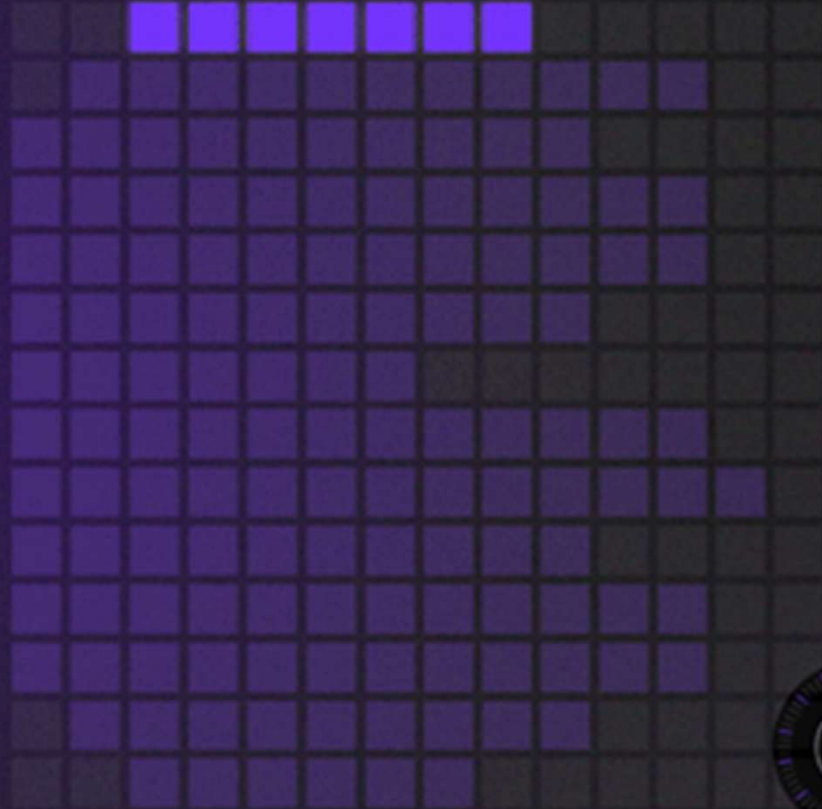


Smart-NIC: data-flow packet processing on the Maverick card



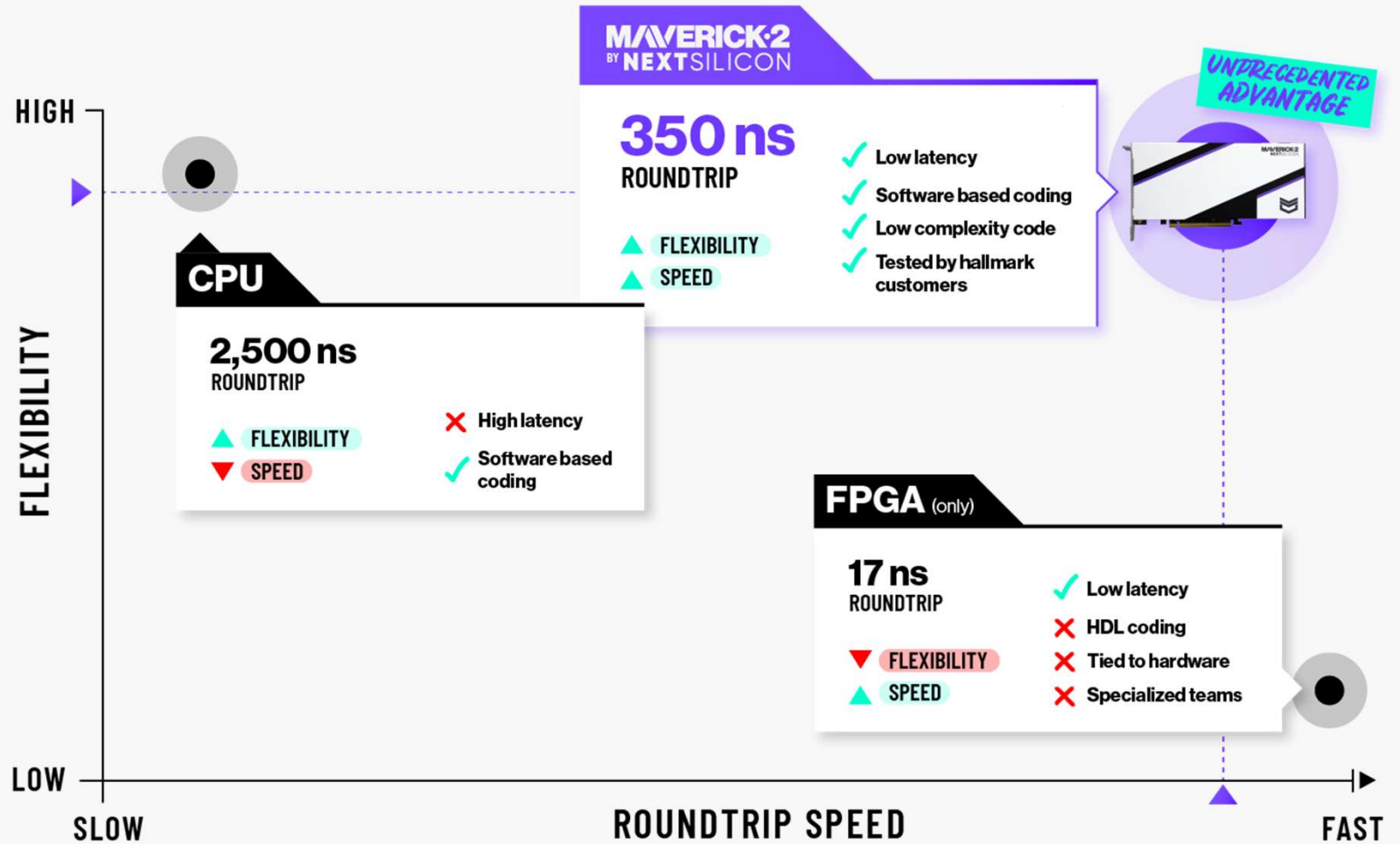


T1



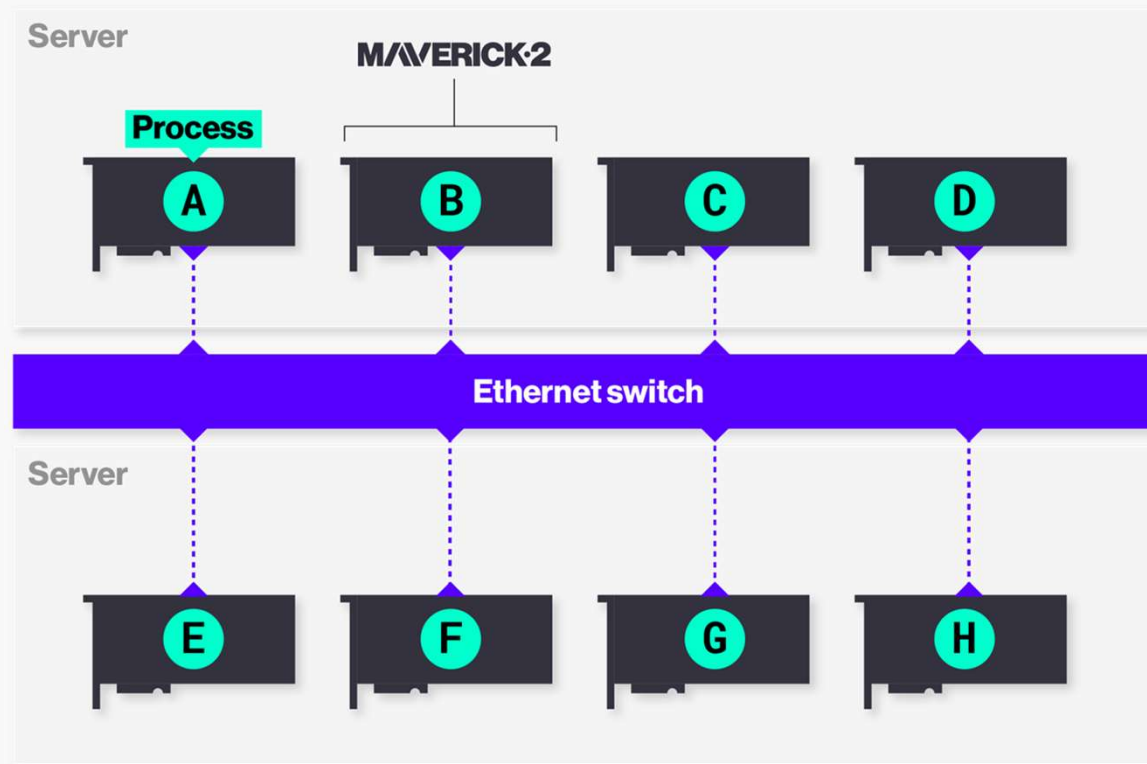


HPC TECH FOR LOW-LATENCY PACKET PROCESSING





MORE BANDWIDTH? NO PROBLEM!





SPECS

ARBEL RISC-V TEST CHIP

ARBEL COMPONENT	SIZE
Frequency	2.5 Ghz
Branch cache	4K
Branch prediction width	128B, 1 taken
Instruction cache	64KB
Issue Width	10
L1 cache	64KB
L2 cache	1MB
L3 cache (per-core)	2MB
ROB	480
integer UOPs dispatch width (ALUs)	6
load dispatch width (AGUs)	3

Store address dispatch width (AGUs)	2
Store data dispatch width	2
Branch dispatch width	3
Integer physical register file	384
Vector/ floating point register file	296
OP\$/MOP\$ BW	20 μ OPs/clk
Vector	RVV
vector/floating point units	4x 128b FMA
DP FLOPS	16 FLOPs/clk
SP FLOPS	32 FLOPs/clk



SUMMARY

1. Dataflow is **more efficient**
2. Works **at scale**
3. Let's prove that it also works for **ODISSEE's use cases**

A RIDDLE

3*7 / 37 / 7*17²





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