LLRF for SPL

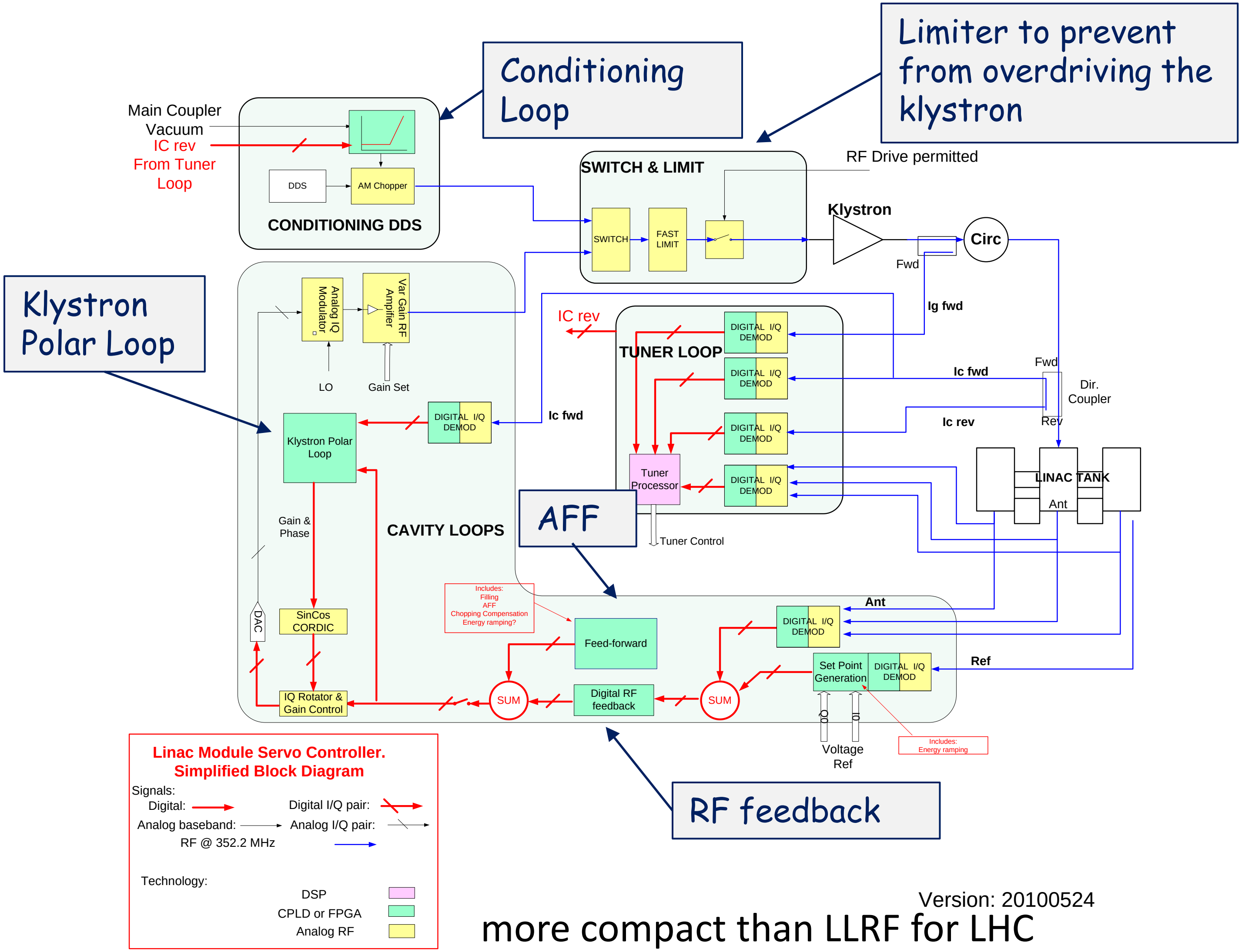
Wolfgang Hofle

Acknowledgements and input:
D. Valuch, P. Baudrenghien, M. Hernandez Flano, F. Gerigk, P. Possoco

Presentation Overview

- SPL versus LINAC4 LLRF architecture
- Hardware developments
- News on simulations: klystron and modulator imperfections
- Optimization in view of cost, high current and low current SPL
- Conclusions

LINAC4 cavity controller block diagram



more compact than LLRF for LHC

compactness could be pushed further for SPL

Differences LINAC4 / SPL

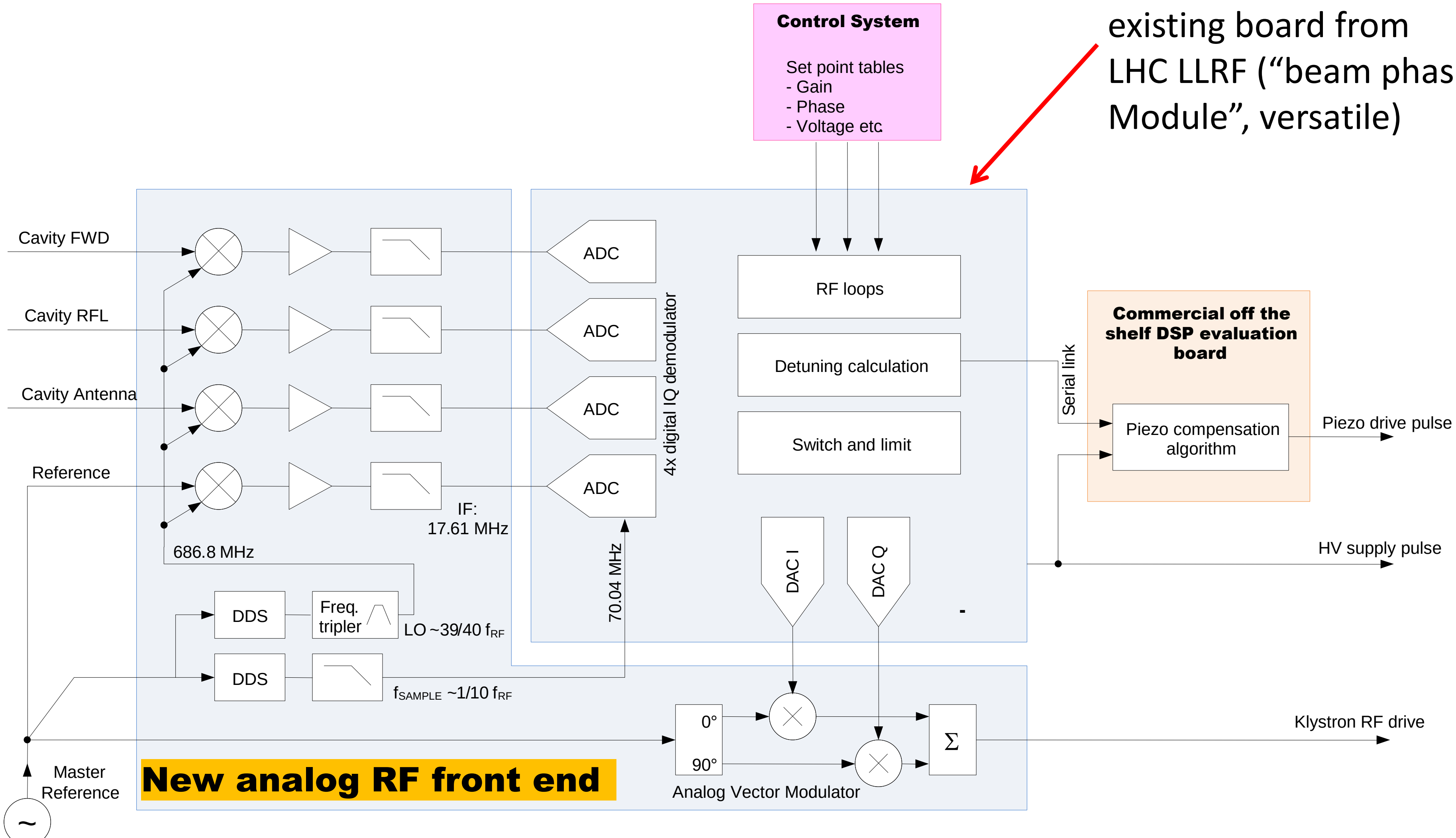
SPL uses super conducting cavities subject to Lorentz Force detuning → piezo control
50 Hz operation in SPL versus 2 Hz operation for LINAC4 → less time for pulse2pulse FF
250+ cavities in SPL → more interesting to compress functionalities on fewer LLRF boards
time scales of projects: LINAC4 commissioning scheduled 2014+
SPL is an R&D activity with a prototype stage in SM18

→ for SPL concentrate on LLRF hardware adapted to SM18 tests
define optimum architecture using results from SM18 tests

goal SPL LLRF:
provide architecture that supplies three technologies for the implementation of control loops: FPGA, DSP, front-end computer in crate

Compact cavity control for SM18

existing board from LHC LLRF ("beam phase Module", versatile)



704.4 MHz

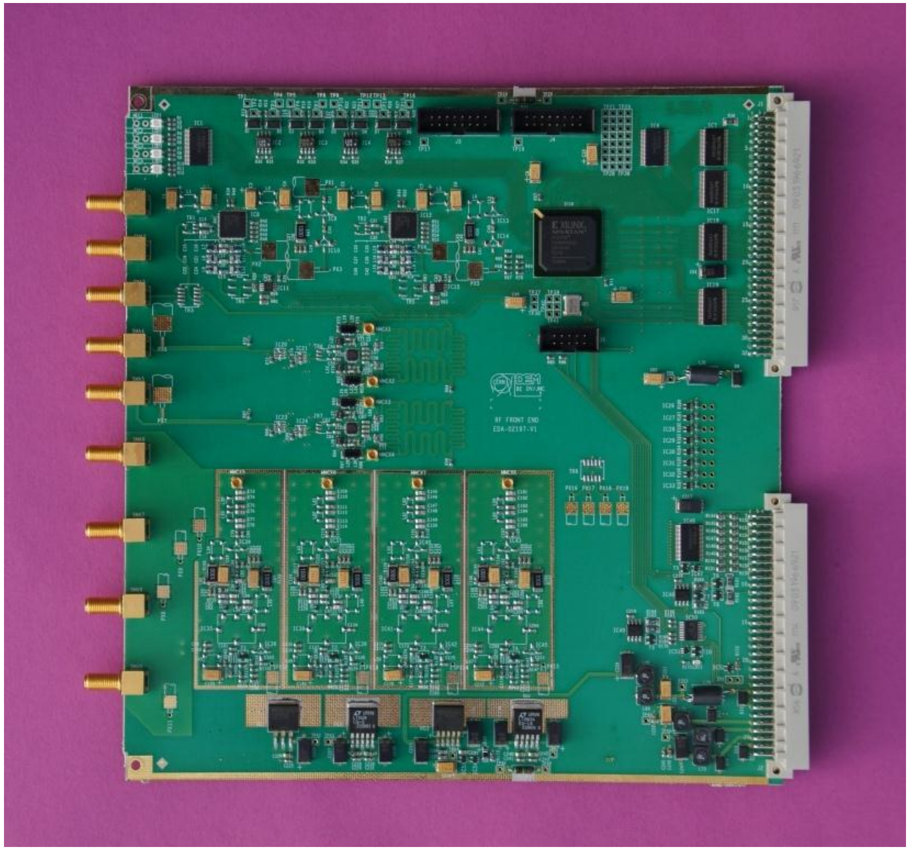
New analog Front-end board

functionality:

clock generation from
reference

de-modulation

modulation



board produced

to be tested

firmware to be developed

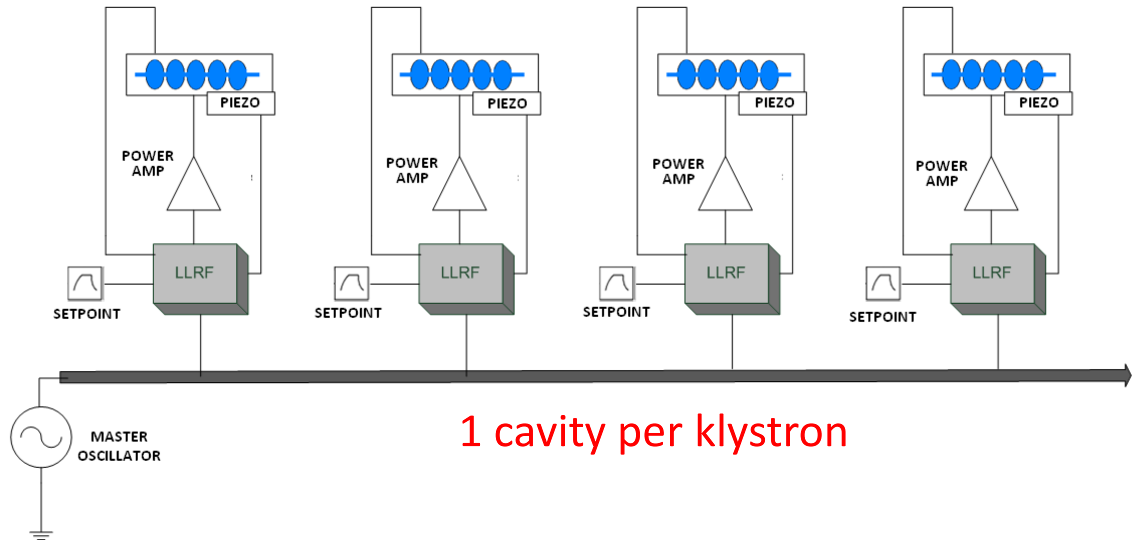
commercial DSP board for

piezo control to be choosen

designer: D. Valuch

Cavity Voltage Control

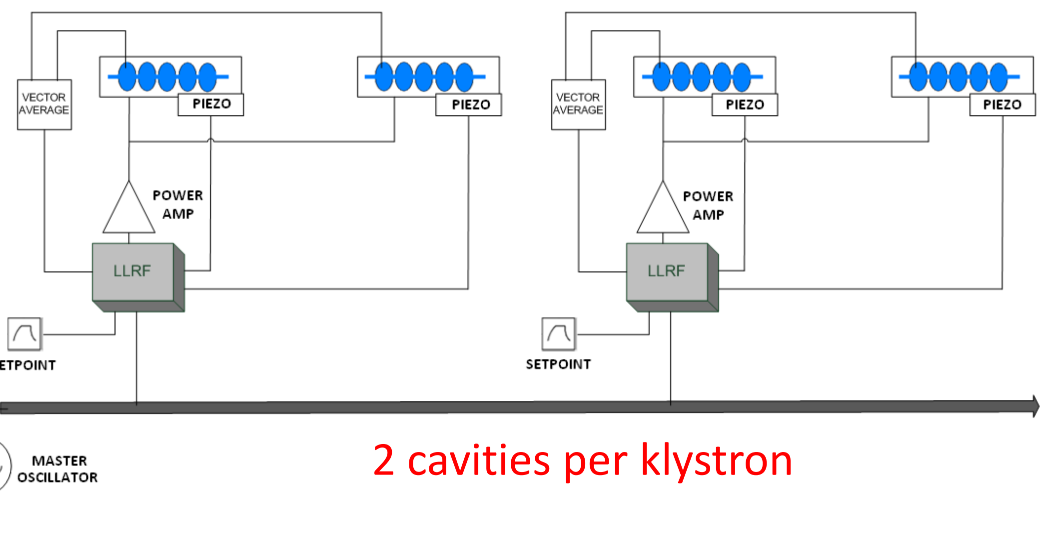
possible operation using 1 or 2 cavities controlled via a single feedback loop



1 cavity per klystron

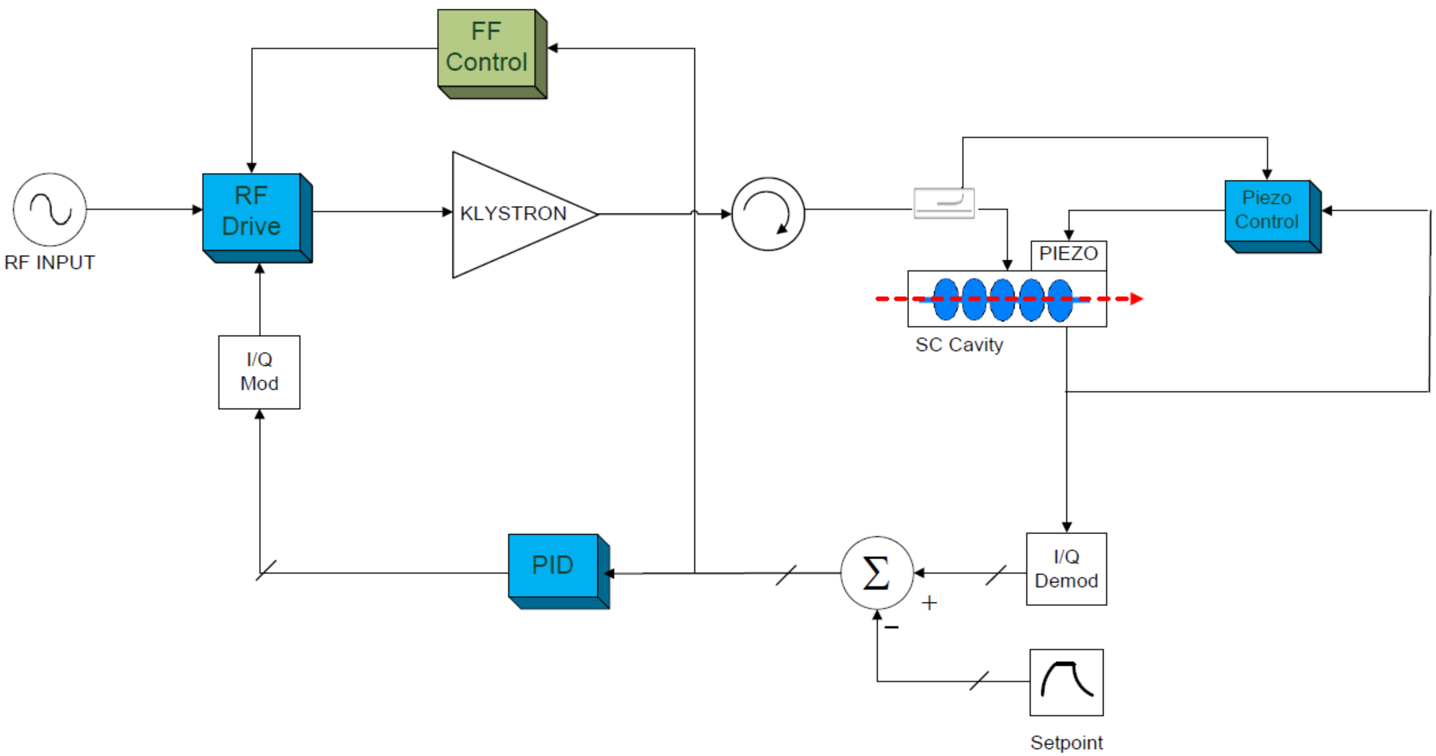
feedback loop acts on cavity voltage vector sum for dual cavity case

feed forward not shown here



2 cavities per klystron

High-Level Diagram of Single Cavity + Control System



$f_{RF} = 704.4 \text{ MHz}$

$I_{b,DC} = 40 \text{ mA}$

$\phi_s = 15^{\circ}$ (LINAC)

$P_b = V_{acc} \times I_{b,DC} \times \cos(\phi_s) = 1.0277 \text{ MW}$

$\frac{R}{Q} = 570\ \Omega$ (LINAC)

$Q_L = \frac{V_{acc}}{\frac{R}{Q} \times I_{b,DC} \times \cos(\phi_s)} = 1.2078 \times 10^6$

$\tau_{beampulse} = 0.4 \text{ ms}$

rep period $= 20 \text{ ms}$

$R_L = 690 \text{ M}\Omega$

$I_g = \frac{V_{acc}}{R_L} + I_{b,DC} \cos(\phi_s) = 77.3 \text{ mA}$

$\tau_{fill} = \frac{2Q_L}{\omega_{RF}} = 0.5458 \text{ ms}$

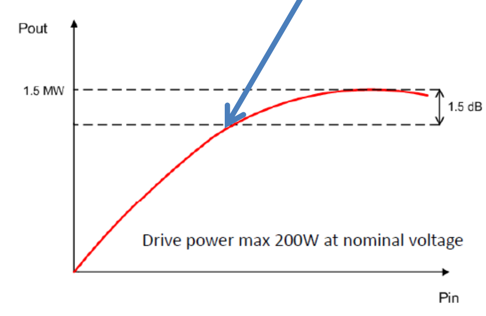
$\alpha = \frac{I_g}{I_{b,DC} \cos(\phi_s)} = 2$

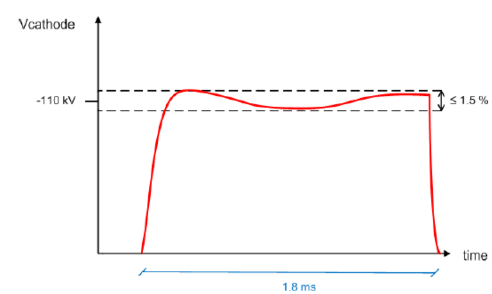
$t_{inj} = \tau_{fill} \ln(\alpha) = 0.3783 \text{ ms}$

Klystron and modulator modeling

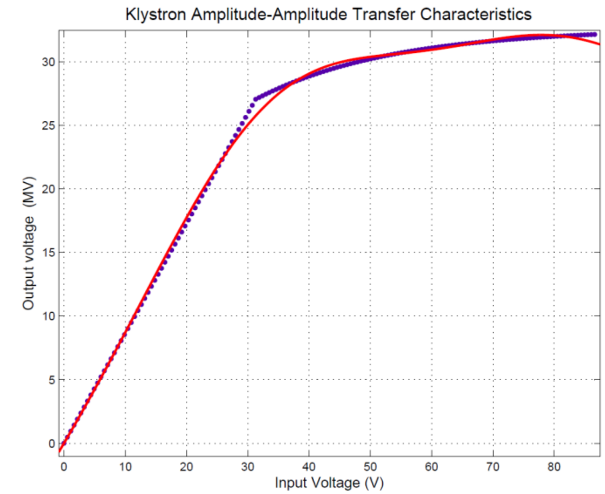
operating point, just above 1 MW

Peak output power at saturation	≥ 1.5 MW
Operating point, below klystron saturation	≤ -1.5 dB
Saturated Gain	≥ 40 dB (Power)
Peak cathode voltage at rated output power	≤ 115 kV
Group delay within frequency range f0 ± 1.5 MHz and operation at -1.5 dB below saturated output	≤ 250 ns
RF Phase over Cathode Voltage variation at constant RF Drive Signal: at saturation: -1.0 dB below saturation: -1.5 dB below saturation:	≤ 15 °/kV
RF Output Power over Cathode Voltage variation at constant RF Drive Signal (-1.5 dB below saturation)	≤ 0.2 dB/%
RF modulator ripple	≤ 1.5 %

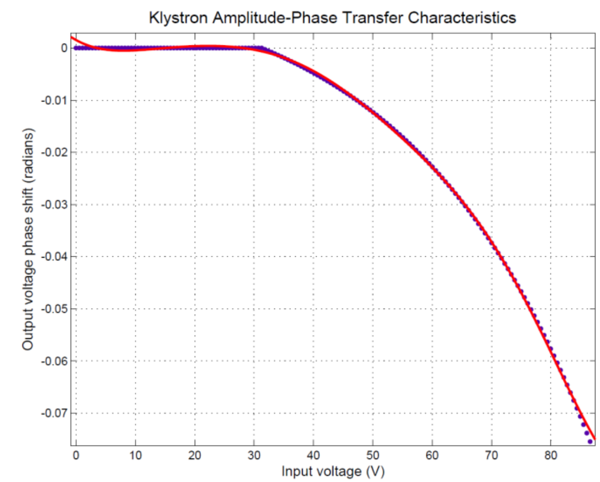




A-A



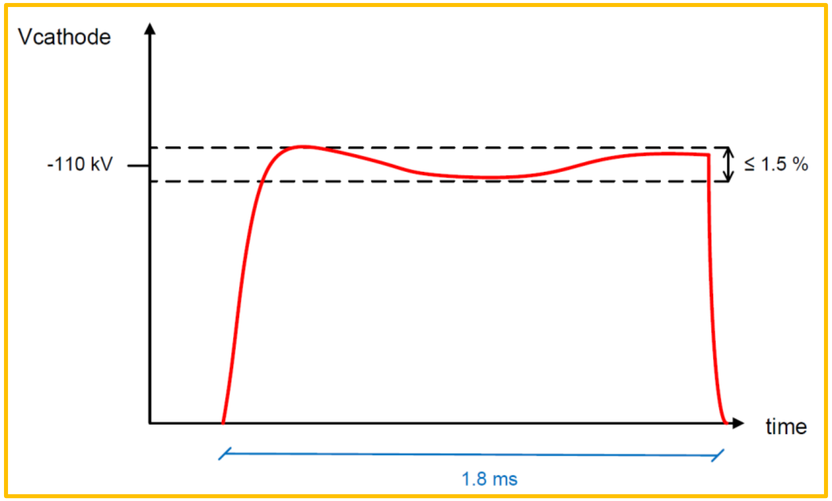
A-P

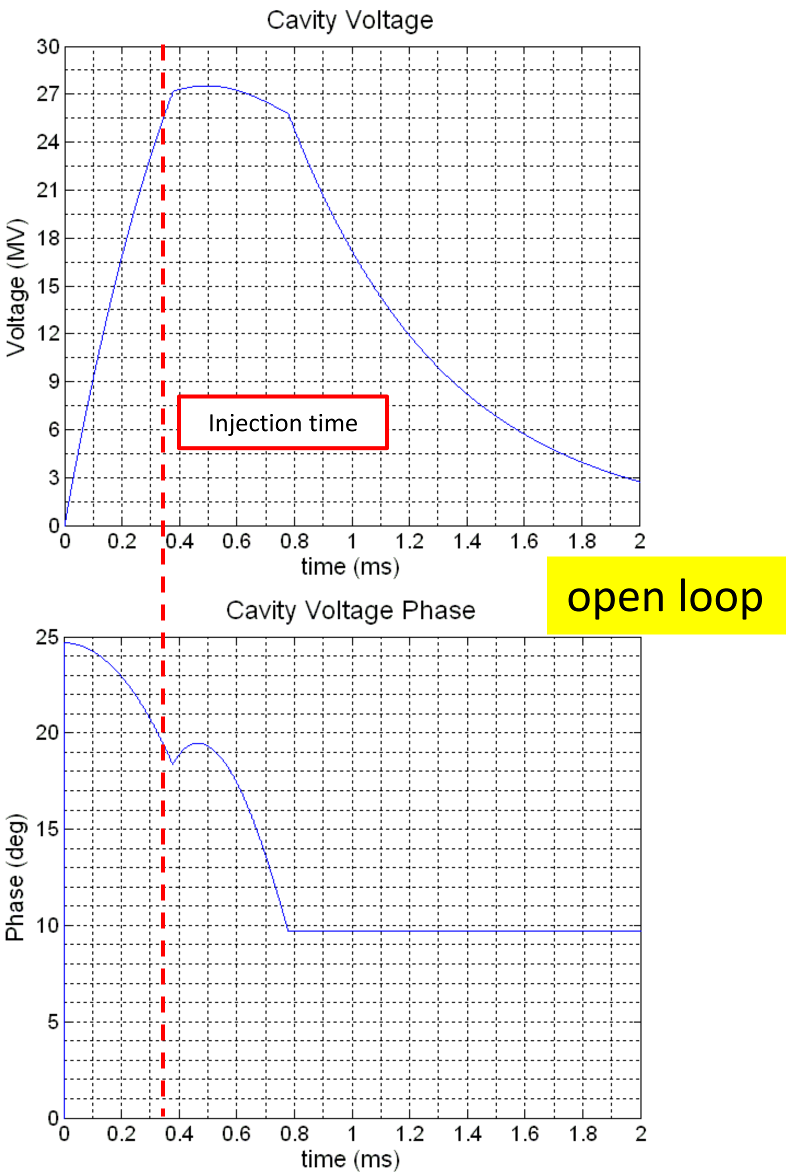


specifications for klystron and modulator ordered for CERN are now taken into account to best knowledge
dominating effect is from modulator (phase change with voltage)
→a combination of a klystron polar loop and feed forward needed; however, actual klystron will not exactly be linear up to 1 MW,
need measurement on klystron in particular for output phase vs power

M. Hernandez

High Voltage Modulator Ripple

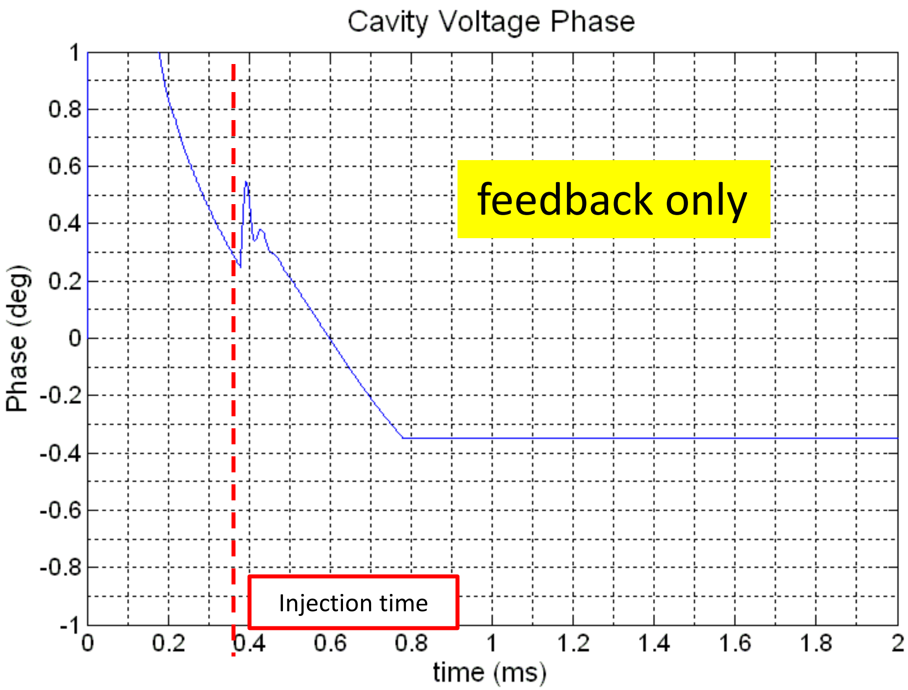




Variations in the high voltage supply from the modulator to the Klystron cathode have noticeable effects on the klystron forward RF in magnitude and phase.

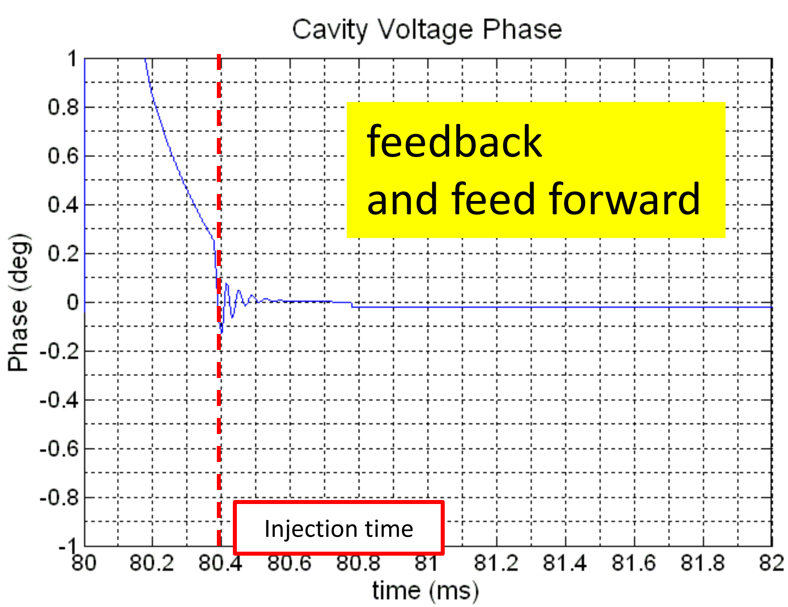
Limits of 0.2 dB/% in magnitude and 15°/kV in phase are specified for the klystron

Correcting modulator feed down to cavity phase with feedback and feed forward

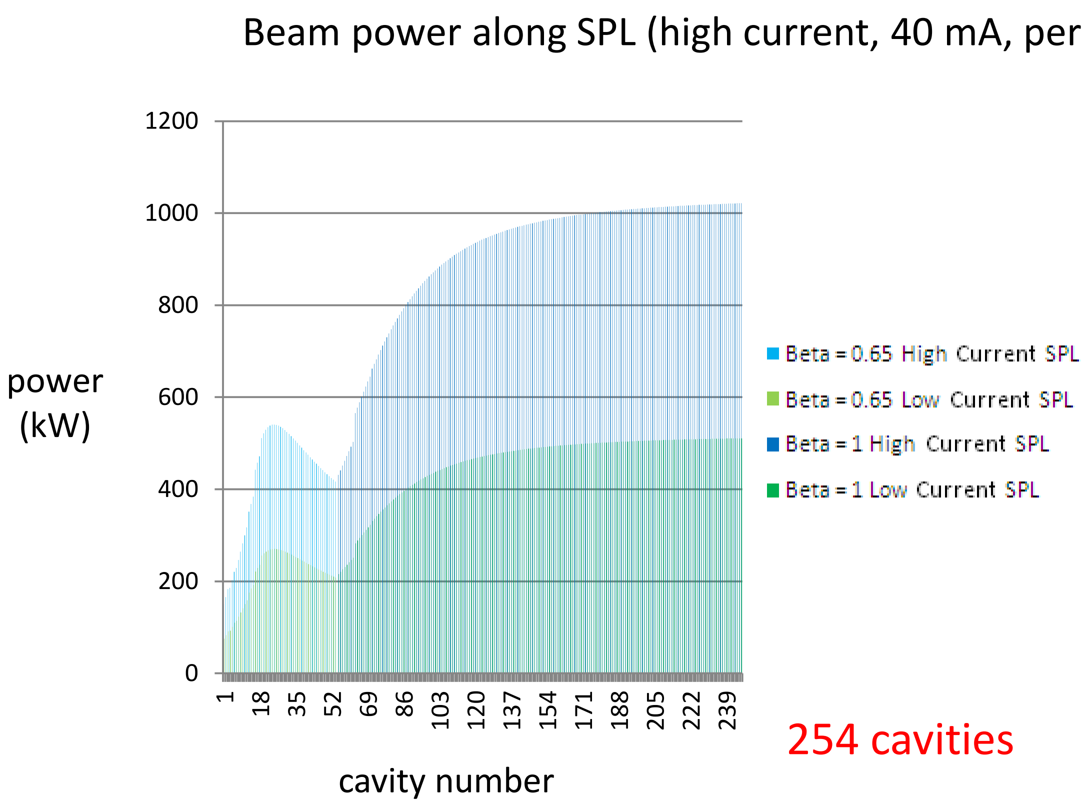


feed-forward recursively corrects the residual error in the cavity voltage from pulse to pulse. After a few pulses, the correction minimizes the modulator ripple effects and the initial transients at beam injection on the cavity voltage waveform.

even with feedback ON, the cavity voltage phase is drifting during the beam pulse,
feed forward needed, alternatively klystron polar loop (not tried)
feed forward: relies on perturbation being repetitive
klystron polar loop does not require the repetitiveness, worth trying

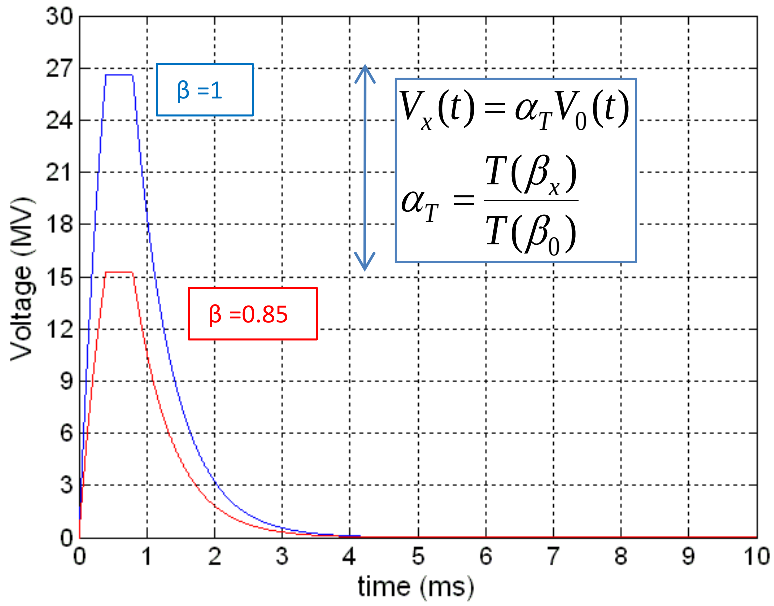


Optimization of power sources for SPL



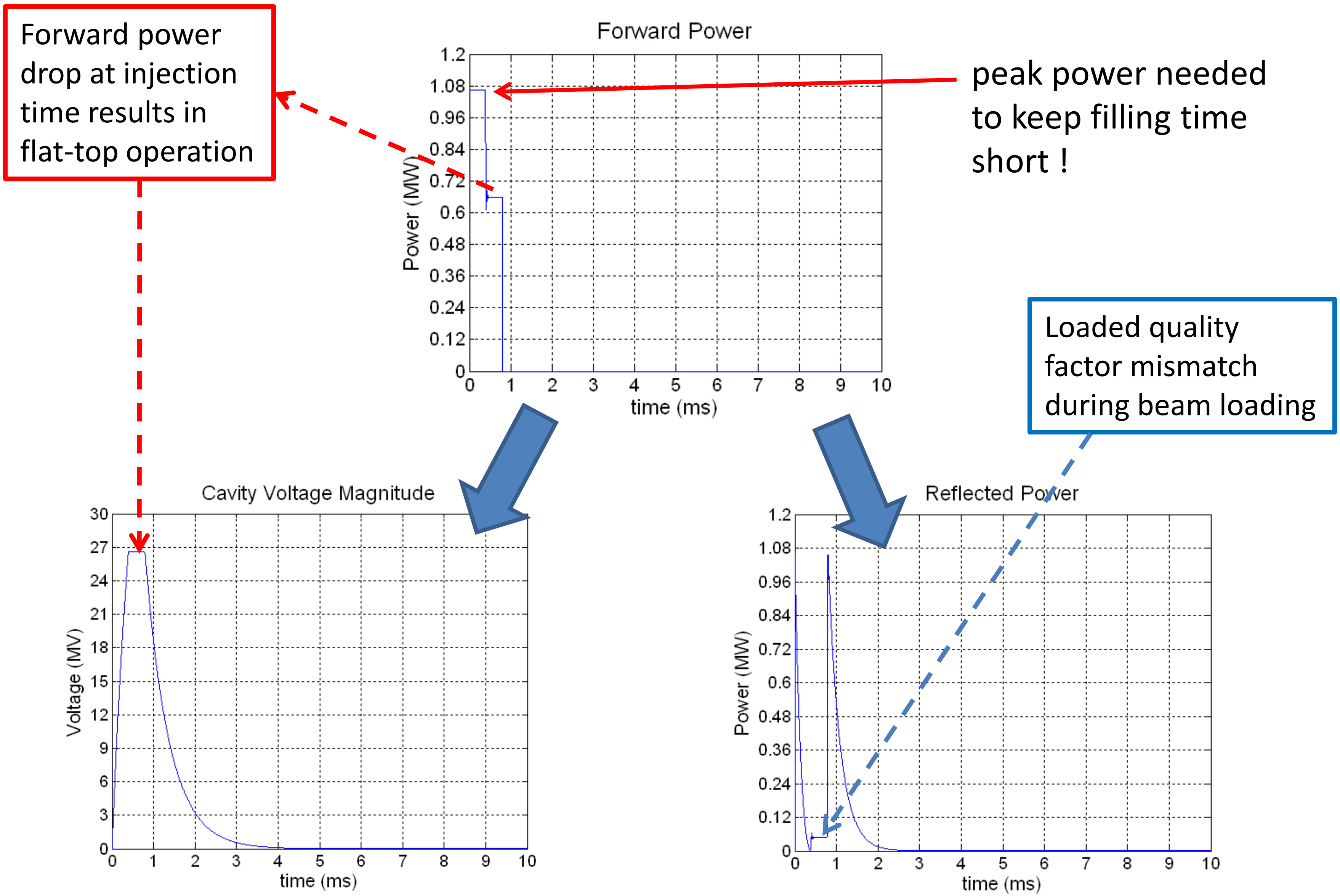
Transit Time Factor Variation with Relativistic Beta (SPL beta=1 cavities)

accelerating voltage



$$V_x^{\infty} = \left(2\alpha_T - \alpha_T^2\right) V_0^{\infty}$$

Situation in the low energy part of the β=1 section



Scenarios for optimization (1)

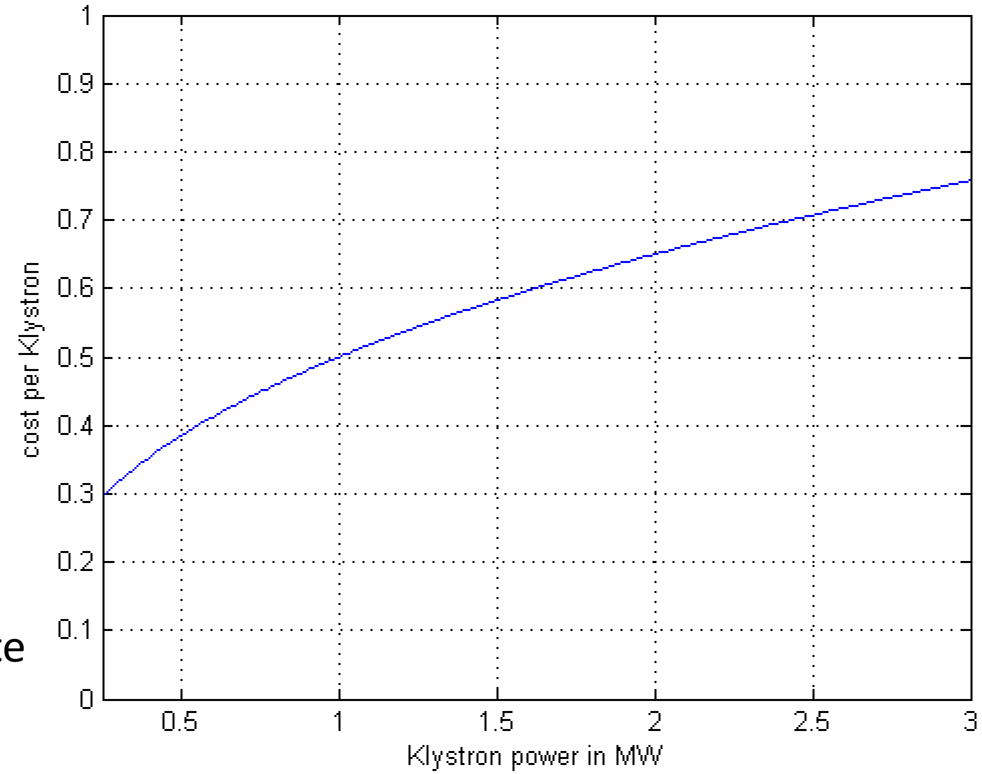
Low current (20 mA, 0.8 ms) and high current (40 mA, 0.4 ms) options

same beam power, but low current option potentially
only needs half the klystron peak power
(if slower filling permitted; change of Q_{ext} between these two versions ?)
low current option needs however longer modulator pulse

Question: is it worth adapting the size of power of klystrons to requirements along SPL
price to pay: different filling times, i.e. also different modulator pulse lengths

five options looked at from klystron cost point of view, assuming the klystron cost
follows a law described by "doubling power" equals 30% klystron cost increase

Scenarios for optimization (2)



pick your favorite currency

Scenarios for optimization (3)

Scenario	relative cost of klystrons
1a) high current one cavity / klystron 160x 1.4 MW 30x 1 MW 70x750 kW	1.34
1b) high current, 95x two cavities per klystron 95x 2.8 MW 70x 750 kW	1.0
2a) low current, single cavity per klystron 260x 700 kW	1.11
2b) low current, 100x two cavities per klystron 100x 1.4 MW 60x 700 kW	0.81
2c) low current 50x four cavities per klystron 50x 2.8 MW 60x 700 kW	0.62

Most of these scenarios can be tested with the CERN ordered klystron and modulator without beam

(1b: with 1.4 MW limit → longer filling time in test stand, assumption no beam)

(2c: longer filling time and shorter flat top in test stand, assumption no beam)

Summary

- compact LLRF hardware under development for SM18 tests
- klystron and modulator imperfections can be compensated with feed forward
- foresee klystron polar loop if non-repetitive perturbations ?
- optimizations possible using different klystrons along SPL, worth the effort ?
  need full cost estimate incl. RF distribution and modulators
- from previous simulations: good piezo compensation essential

  two and four cavities per klystron feasible, but constraints

  from beam dynamics due to adjacent cavities doing the “opposite”