Update on R&D for OT FE electronics (Nikhef)

T. Sluijk, W. Vink, A. Zwart

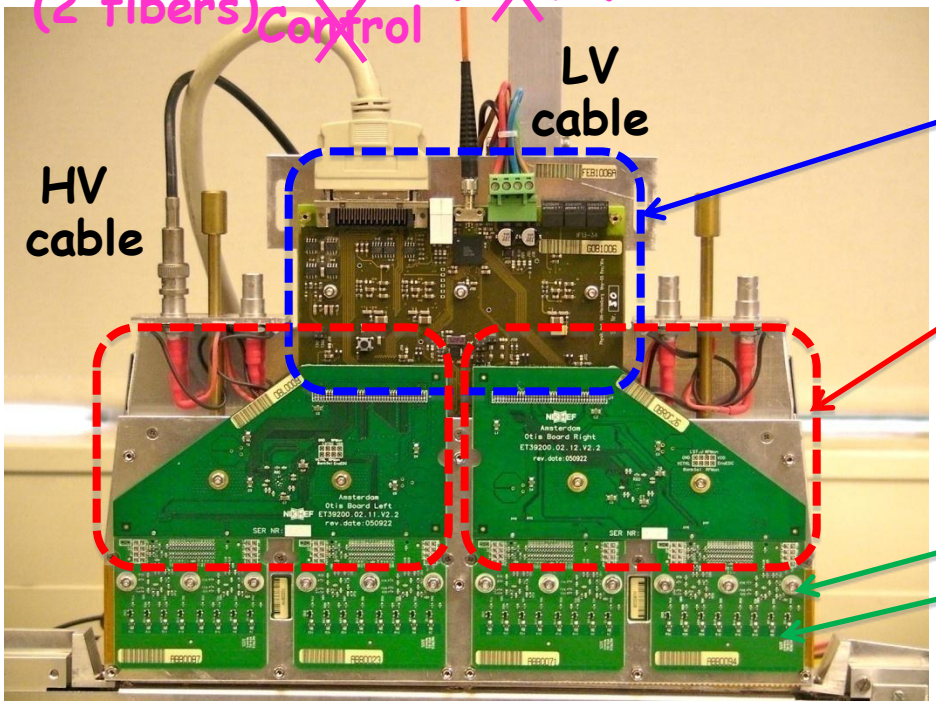
CERN, 15-09-2011

- introduction
- TDC design on Actel FPGA
- TDC prototype board
- plans and outlook

Overview of OT 40MHz Upgrade

We have 432 of these objects (FE Boxes in OT)

- 36 per C-Frame (12 C-Frames)



GOL/AUX Board (and ASIC) needs replacement

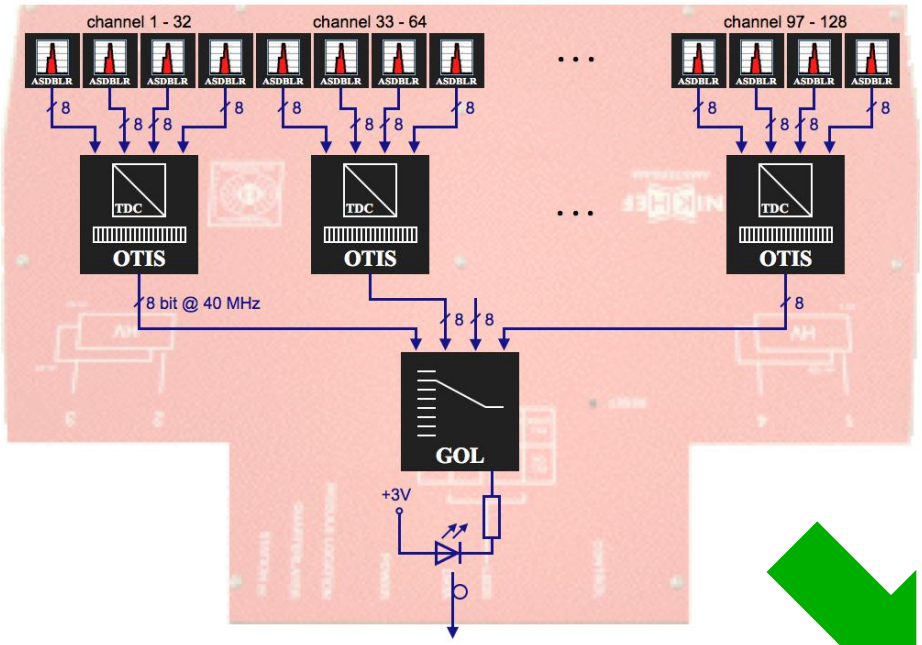
OTIS Boards (and ASIC) need replacement

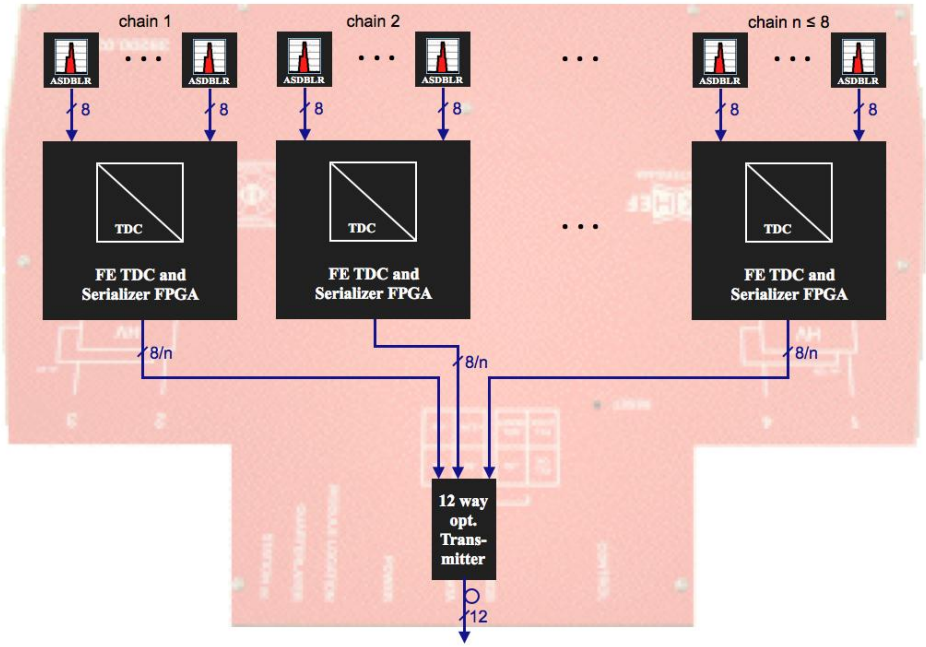
HV and ASDBLR Boards may remain unchanged

Reuse HVB+ASDBLR+FE Mechanics (73% of present OT FE cost)!

Keep present design and redesign OTIS and GOL/AUX Board is really a good idea!!

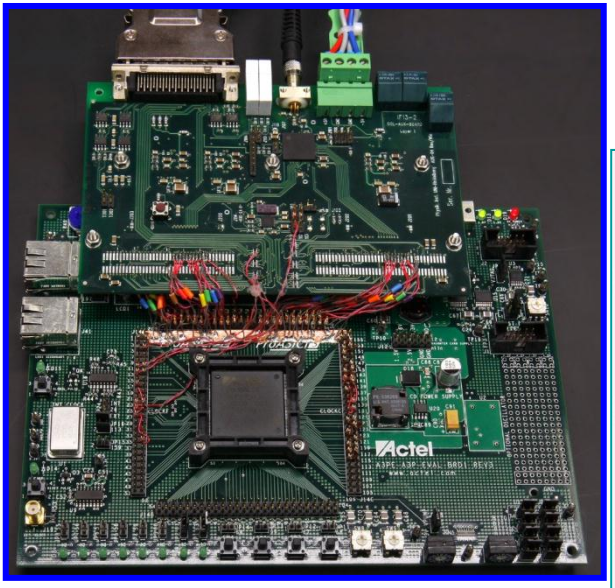
Past and Future





Nikhef Work Package

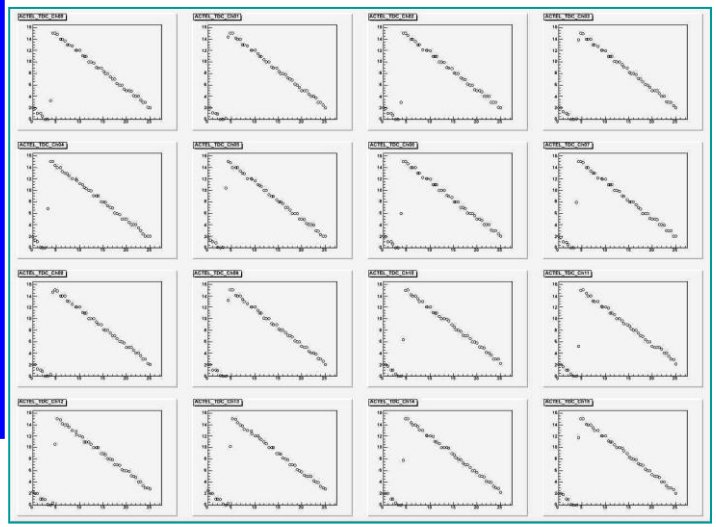
This R&D project is under way, designing prototypes…

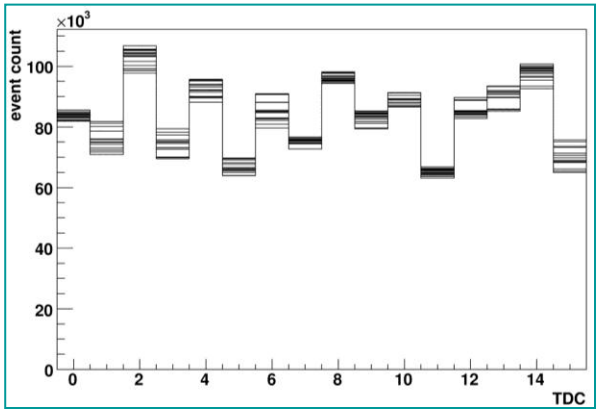


40MHz TDC implemented in Actel FPGA

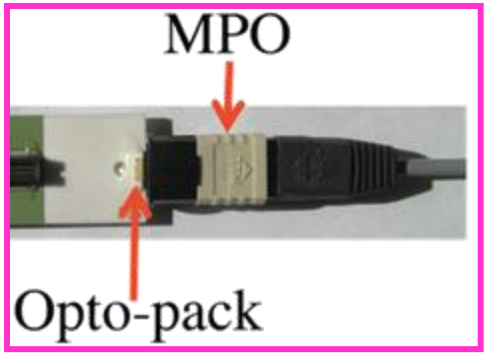
Gen. rad. tests positive, now testing PLL at Fermilab

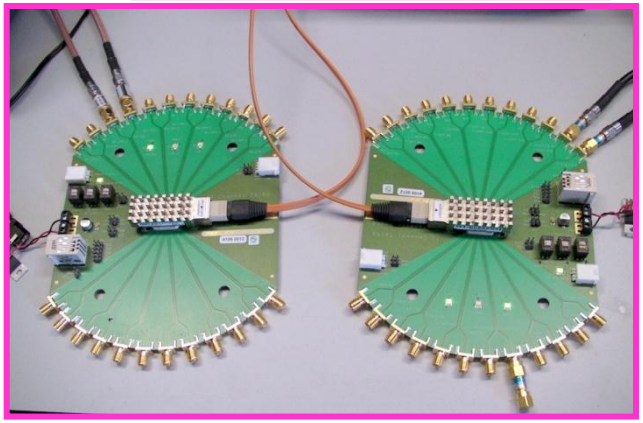
Integral and differential non-linearity OK



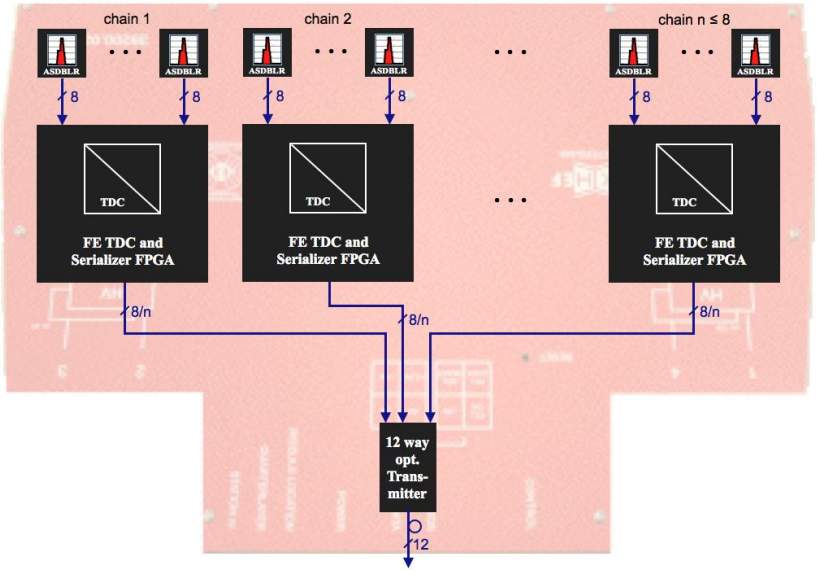


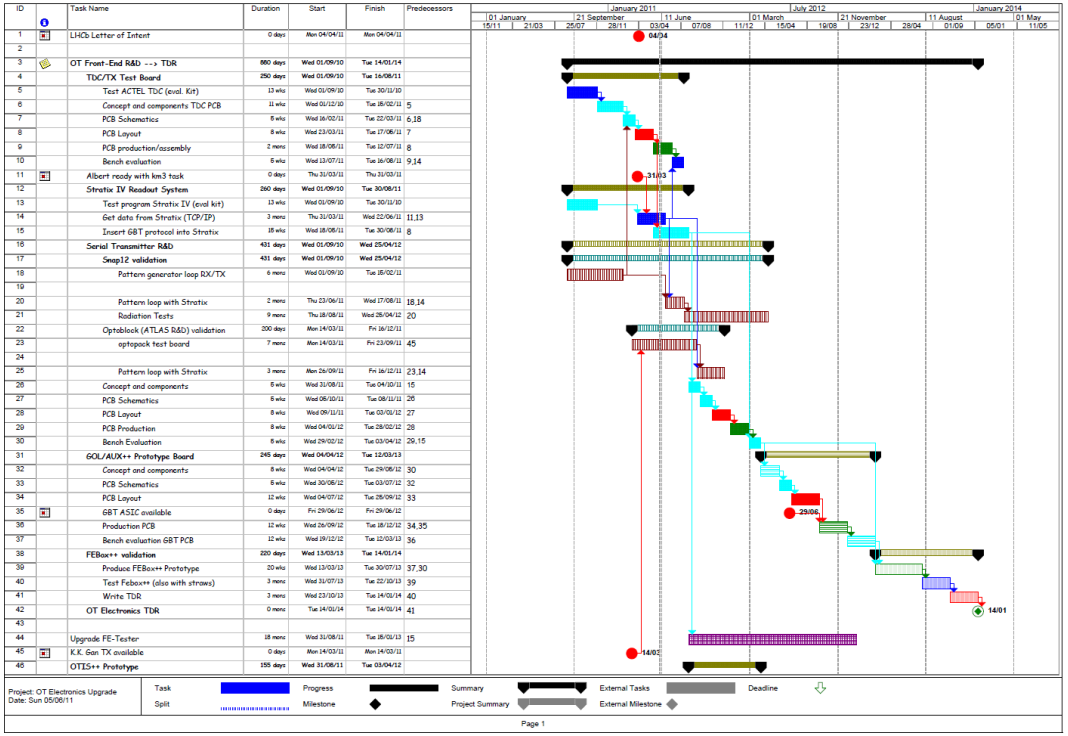
12-chan. Transmitters (industrial and common R&D with ATLAS)





OT FE 40 MHz Plans/Ambitions



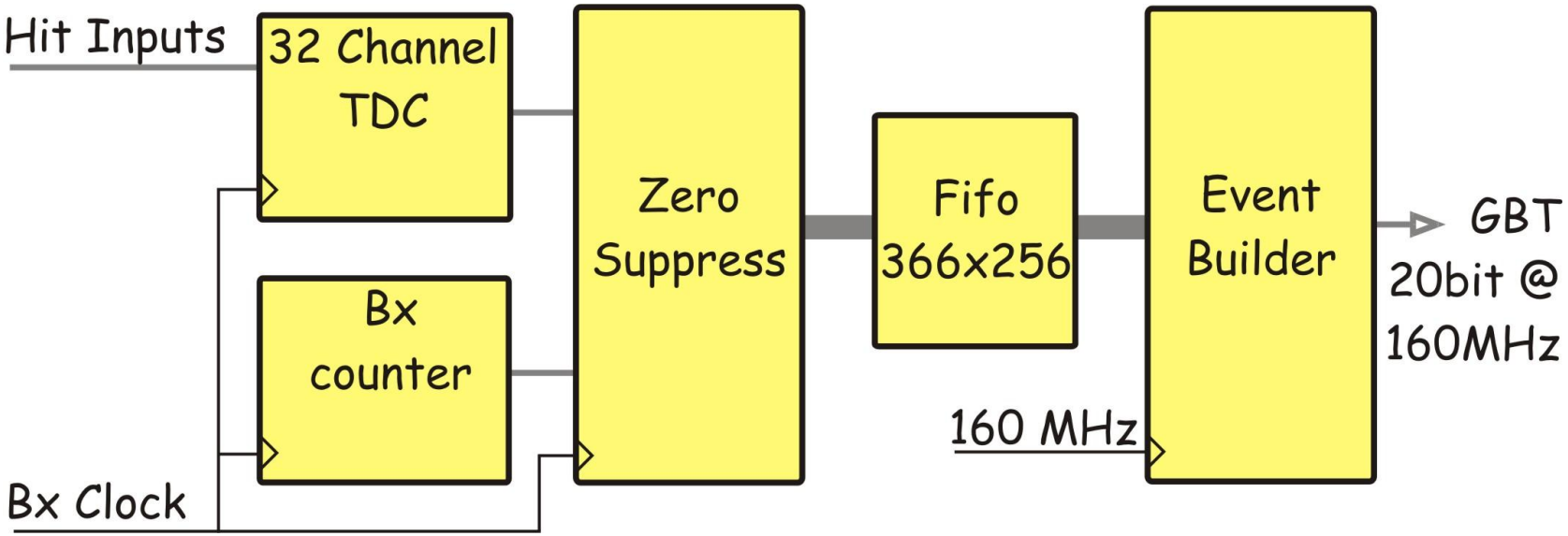


Man-power ET:

- TDC Board ~1.5 FTE x 1y
- optical transmitter ~1 FTE x 2y
- serializer/transmitter board ~1.5 FTE x 1y
- FE prototype + Tester ~1 FTE x 1y

Man-power CT: ~0.5 FTE x 2y

TDC Schematics Overview



- Design of TDC in ACTEL Proasic3E FPGA because of the radiation properties
- 32 Channel 5 bit TDC (bin size 785 ps)
- Zero Suppress data format
- Output 20 bit LVDS @ 160 MHz to GBT
- I2C interface to set Mask Register, data format

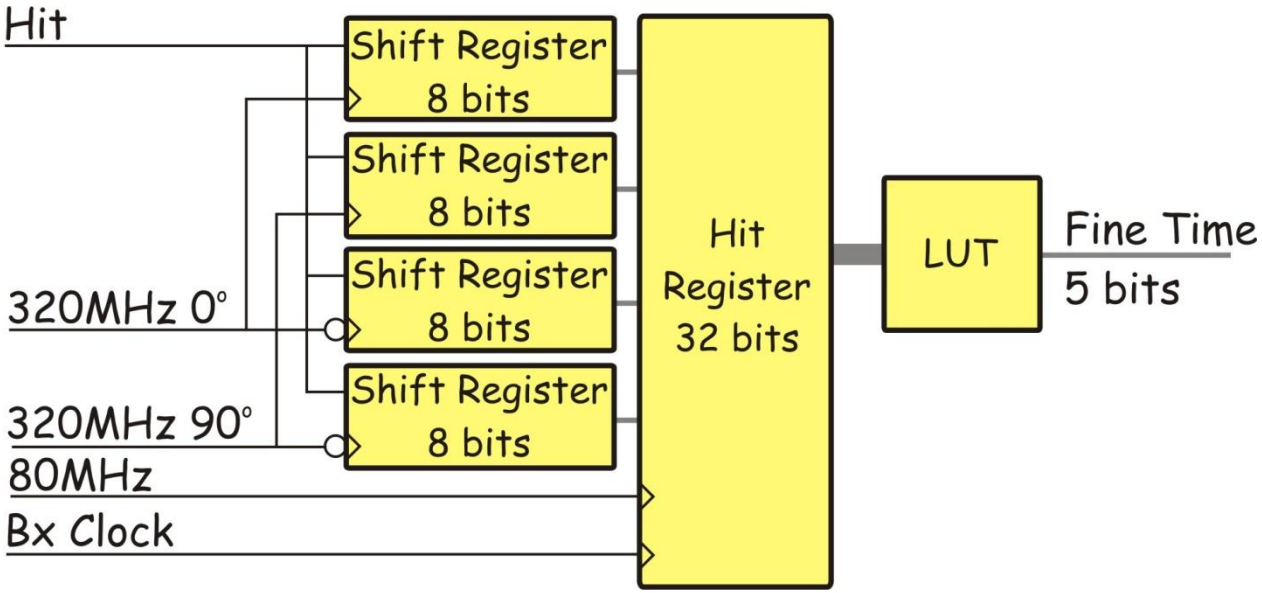
Compile Report

Family : ProASIC3E
Device : A3PE1500
Package : 484 FBGA

Compile report:

CORE	Used: 21956	Total: 38400	(57.18%)
IO (W/ clocks)	Used: 127	Total: 280	(45.36%)
Differential IO	Used: 58	Total: 139	(41.73%)
GLOBAL (Chip+Quadrant)	Used: 6	Total: 18	(33.33%)
PLL	Used: 2	Total: 6	(33.33%)
RAM/FIFO	Used: 21	Total: 60	(35.00%)
Low Static ICC	Used: 0	Total: 1	(0.00%)
FlashROM	Used: 0	Total: 1	(0.00%)
User JTAG	Used: 0	Total: 1	(0.00%)

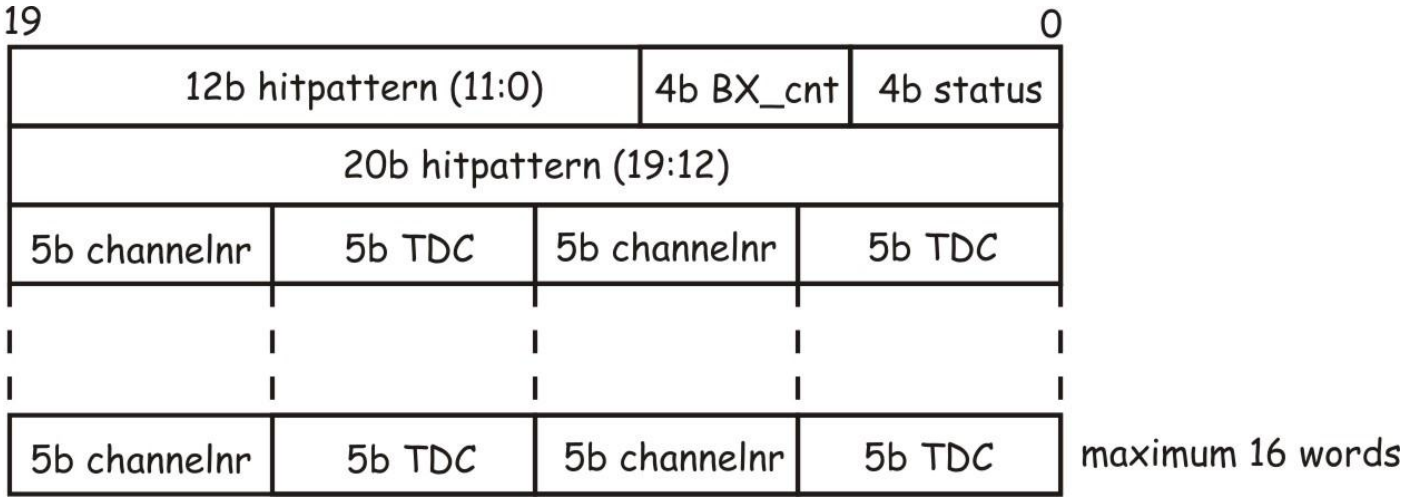
1-channel functional scheme



- PLL generates 3 clock signals; 8x Bx (320 MHz), 8x Bx (320MHz) phase shift 90°, 2x Bx (80 MHz)
- 4 Shifter registers, shifting on the positive edge and the negative edge of the 320 MHz clocks, dividing the Bx in 32 phases
- After each BX period the state of the shifter registers are latched in the Hit Register
- The LUT translates the 8 bit Hit Register into 5 bit time info

Data Format (prelim.)

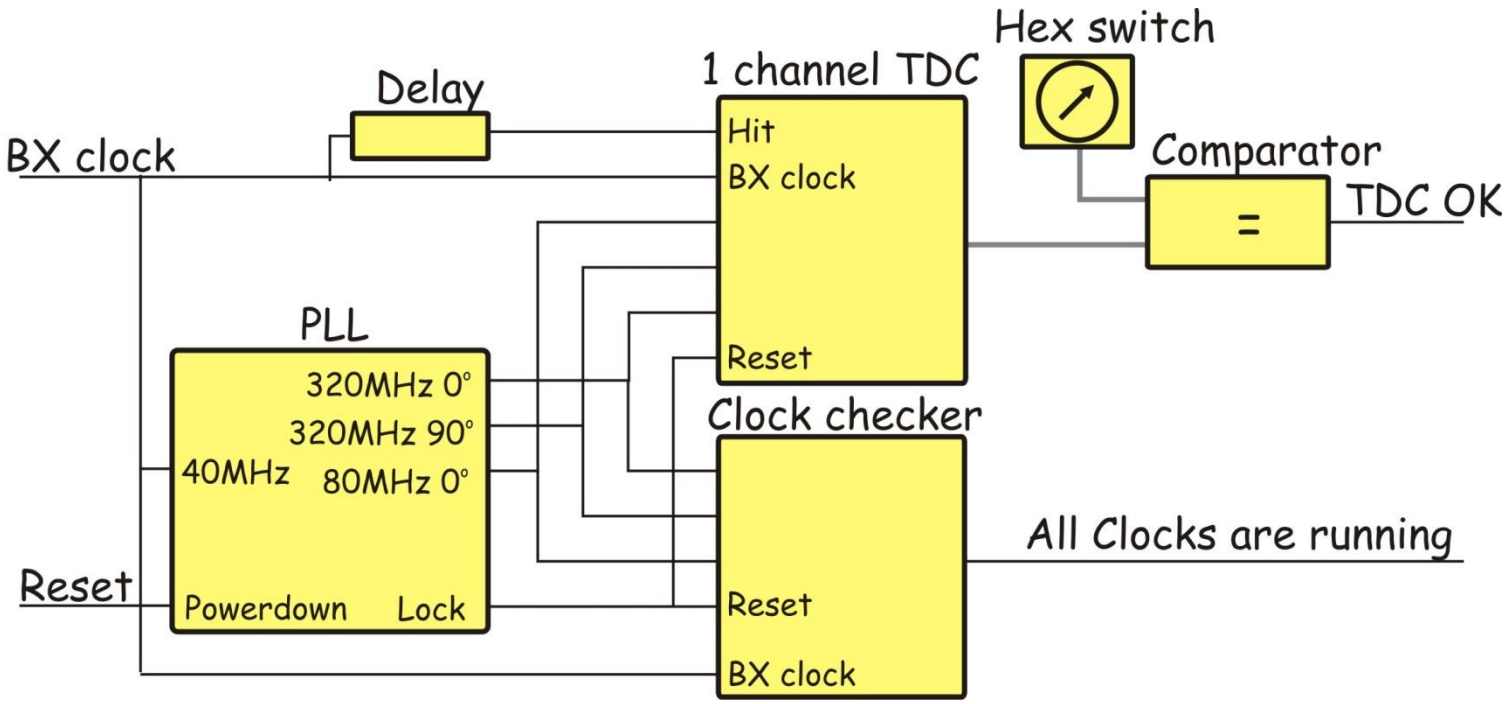
For the moment, use (redundant)



- Status register:
  - Bit(0) = truncate
  - Bit(1) = zero suppress
  - Bit(2) = fifo flag error
  - Bit(3) = spare

PLL tests under irradiation

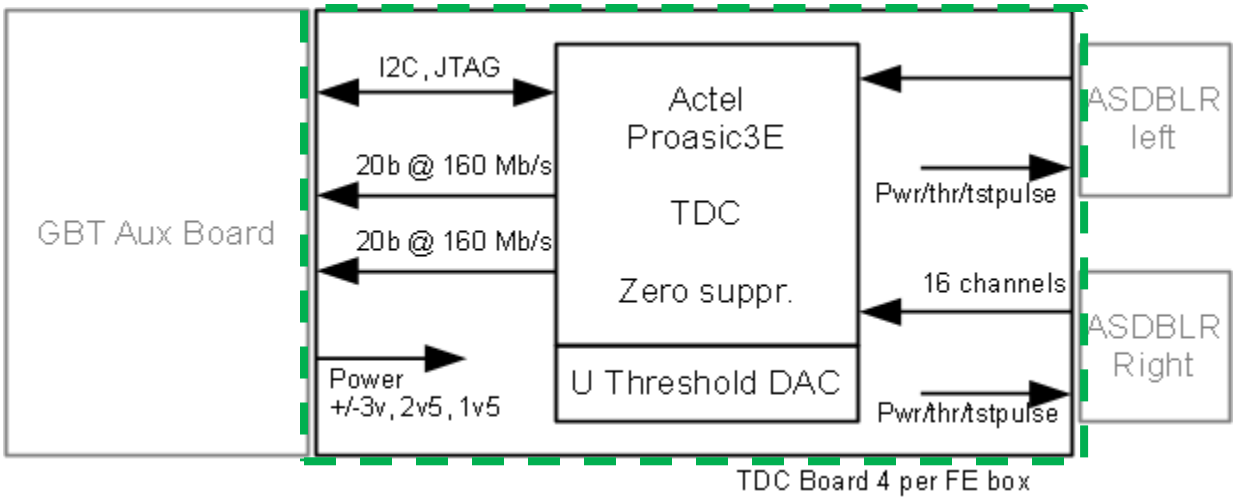
In cooperation with Syracuse (R. Mountain), results expected soon



- The 3 outputs of the PLL are used for the shifter clocks of a TDC
- The BX clock is delayed to get a synchronous Hit signal this gives a fixed TDC value
- The presence of the PLL clocks are continuously checked

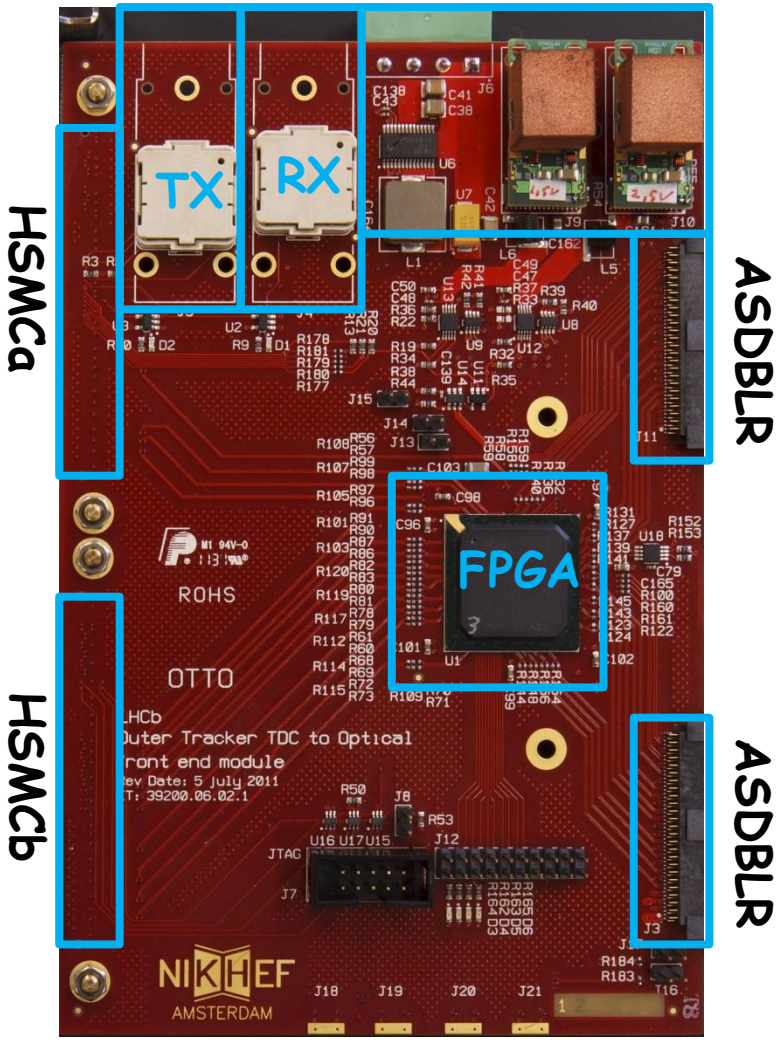
TDC Prototype Board (OTTO) Goals

- TDC board replaces OTIS board
  - Identical mech. dimensions
- Actel ProAsic3E FPGA (one or two TBD)
  - TDC 1(or 2) 16 channel inputs from ASDBLR
  - Zero suppression
  - I2C controlled
- Threshold DAC (TBD)
  - Threshold voltage ASDBLR
- Interfaces GBT aux board
  - 20b @ 160Mb/s data bus to GBT

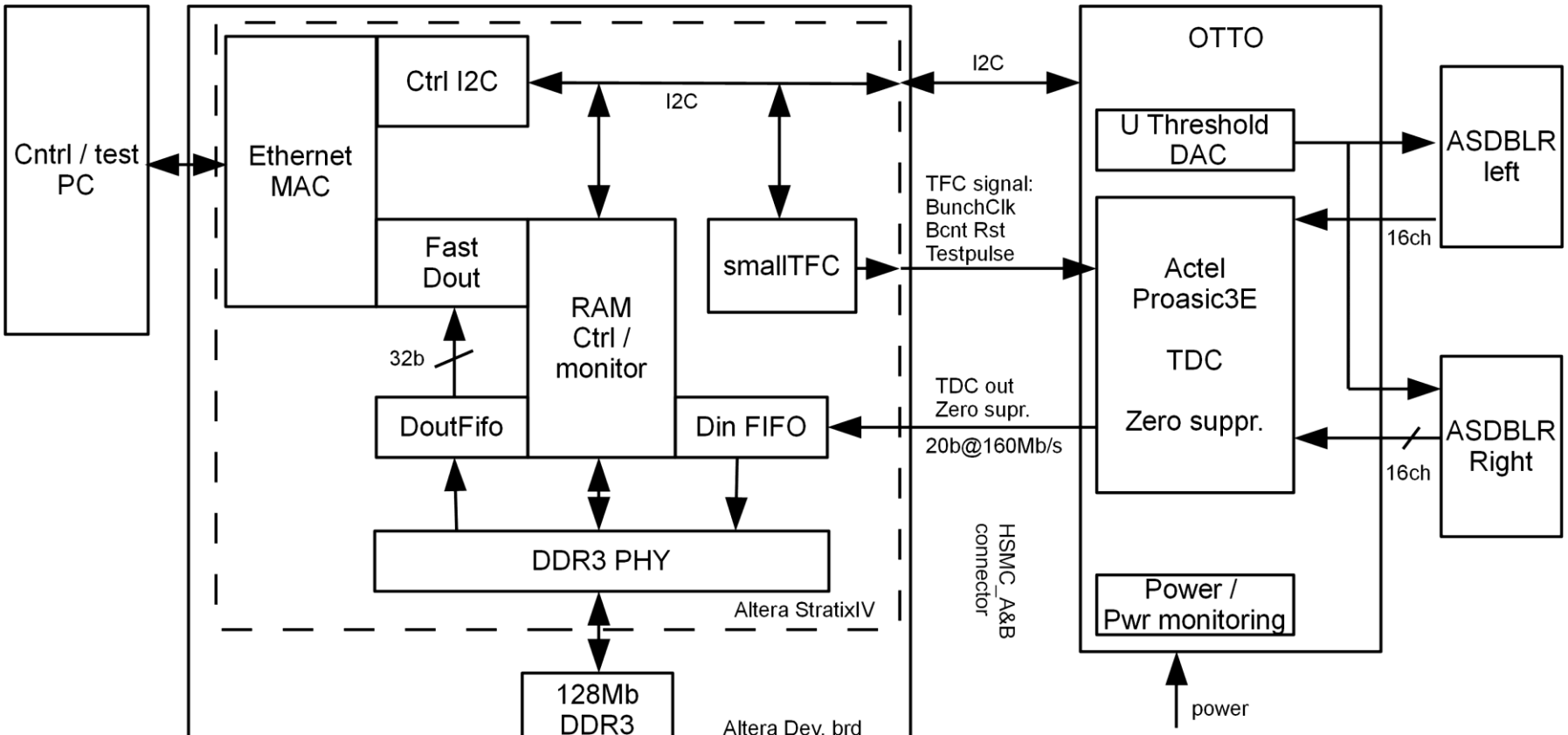


OT TDC to Optical (OTTO)

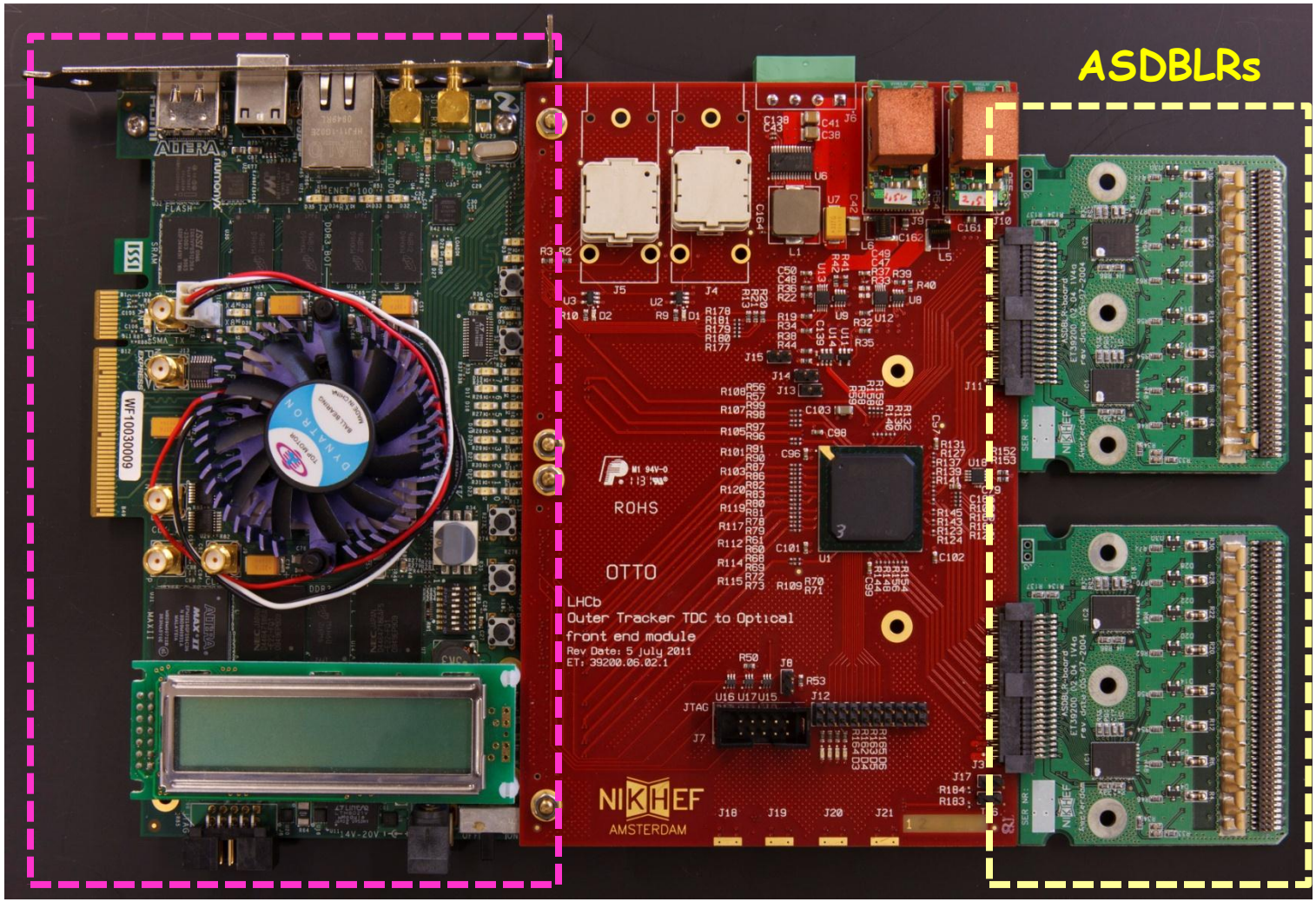
- First prototype OTTO
  - Ready for test
  - Actel ProAsic3eFGG494
    - 2 * 16 channel TDC in
    - 1 * 20bits@160Mb/s out to Stratix IV
  - Connect to stratix IV development board with HSMC connectors
  - Two ASDBLR connectors
  - SM01C DCDC converters
  - Power monitoring, overcurrent protection (prevent latchup damage, radiationtest)
- Data analysis:
  - 128MB DDR3(upgradable to 512)
  - Readout through 1Gb ethernet
- Second stage:
  - Include GBT (Tx/Rx) protocol in data path
  - Use "GBT-FPGA Firmware Starter Kit"



OTTO Test Setup (schematics)



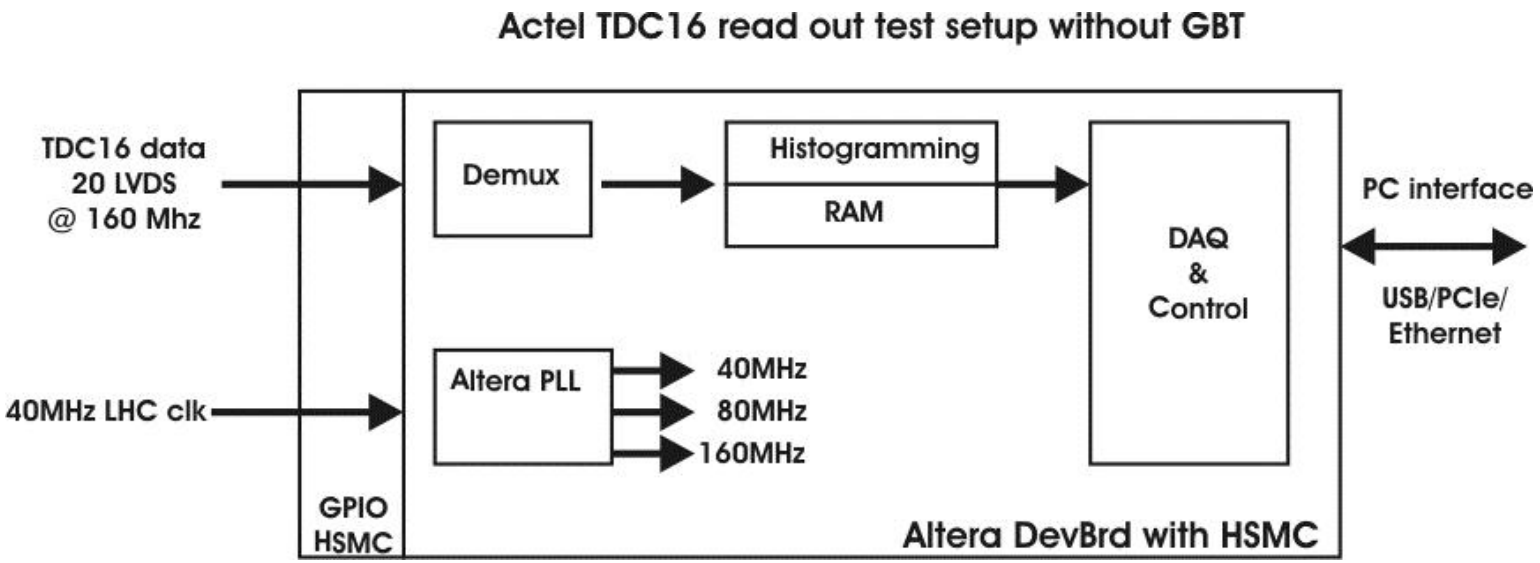
OTTO Test Setup (the real thing)



Stratix IV (readout and GBT emulator)

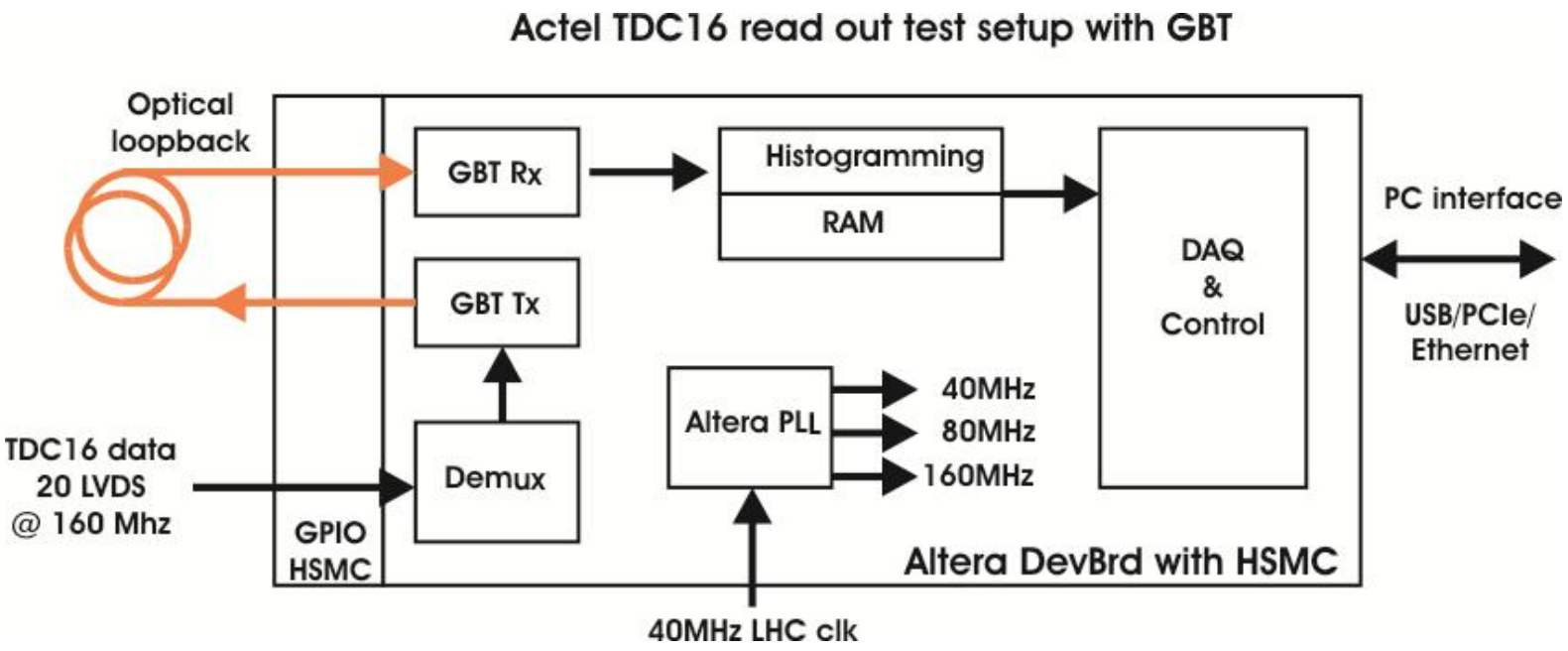
Test Board for TDC readout

- TDC Data analysis, without GBT data TxRx
  - Analyze 32 channel TDC output (low testpule rate)
  - Analyze 16 channel TDC output (high testpule rate)
- 20 bits @ 160 Mb/s LVDS data interface with Actel 2*16ch TDC
  - HSMC pio to interface TDC data bus



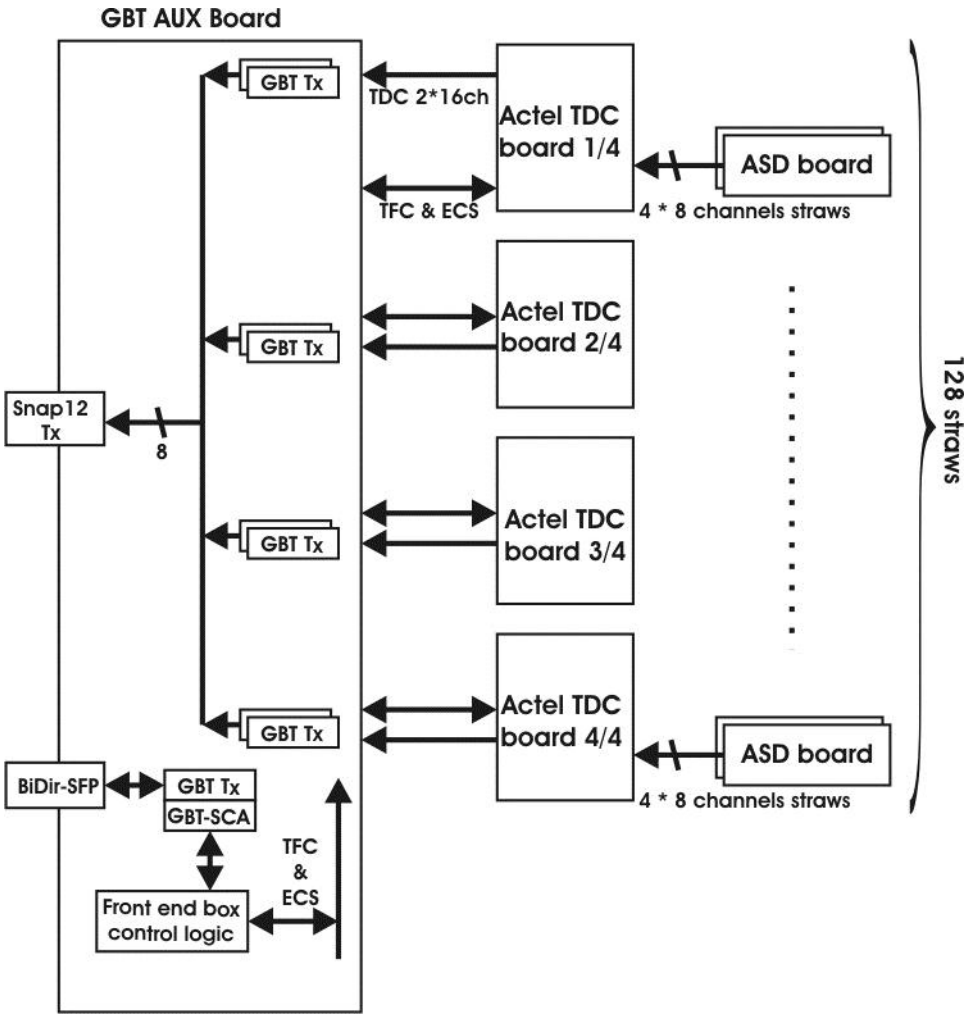
Test Board + GBT emulator

- Expanded with GBT Tx Rx loopback in data path
  - 12 channel MPO TX/RX on OTTO proto pcb
  - Use "GBT-FPGA Firmware Starter Kit"
- Data analysis includes check of GBT data path

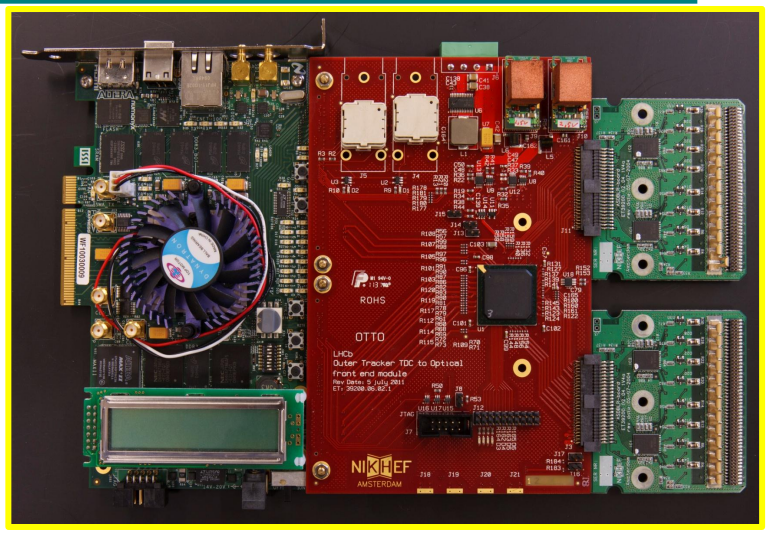


In reality what we want...

- GBT AUX board replaces GoI board
  - Identical mech. dimensions
- 8 GBT -> data transmission Snap 12 MPO opt. Tx
  - Option use of 4 Dual SFP Tx
- 1 GBT / GBT-SCA for TFC/ECS
  - Bidir SFP ?
- Interfaces four TDC cards
  - 128 TDC channels @ 40MHz



In Summary



- Combined functionality
  - TDC board (upgraded OTIS board)
  - 1/8 GBT aux board (upgraded GOL board)
- First proto based on Altera Stratix IV dev kit
  - 4SGX230N expanded with High Speed Mezzanine Card OTTO
- Actel ProAsic APA1500 with 2*16 TDC channels(OTTO)
- GBT like data bus 20b @ 160 Mb/s
- Functionality:
  - Prove Actel TDC / ZS concept
  - Test GBT data transmission
  - Histogram of TDC Zero Suppressed data
  - Buffer burst of consecutive TDC output in RAM
    - Offline analysis ZS data
    - Short runs, length to be defined depending on ZS and memory
- Data interface to host for offline analysis (proto only)
  - Gb Ethernet