Update on R&D for OT FE electronics (Nikhef)

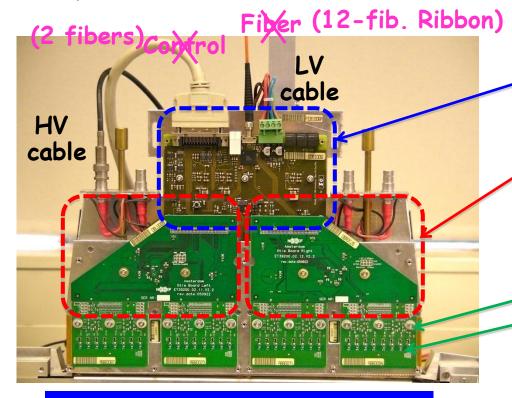
T. Sluijk, W. Vink, A. Zwart CERN, 15-09-2011

- o introduction
- o TDC design on Actel FPGA
- o TDC prototype board
- o plans and outlook

Overview of OT 40MHz Upgrade

We have 432 of these objects (FE Boxes in OT)

· 36 per C-Frame (12 C-Frames)



GOL/AUX Board (and ASIC)
needs replacement

OTIS Boards (and ASIC)

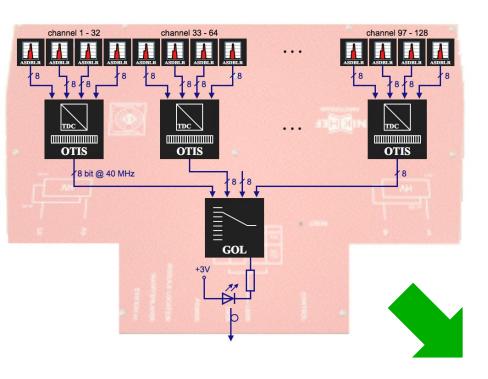
need replacement

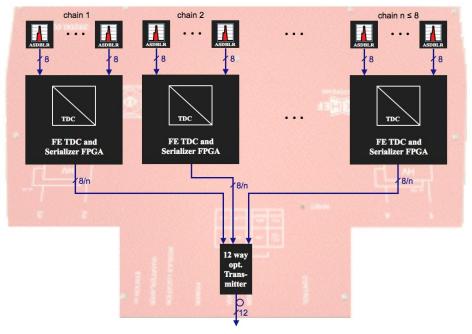
HV and ASDBLR Boards may remain unchanged

Reuse HVB+ASDBLR+FE
Mechanics (73% of present
OT FE cost)!

Keep present design and <u>redesign OTIS</u> and <u>GOL/AUX Board</u> is really a good idea!!

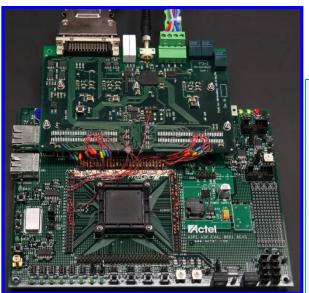
Past and Future





Nikhef Work Package

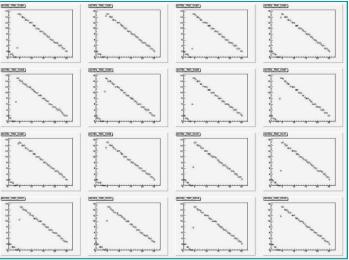
This R&D project is under way, designing prototypes...

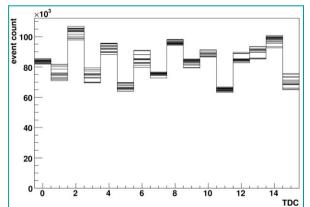


40MHz TDC implemented in Actel FPGA

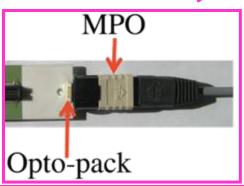
Gen. rad. tests positive, now testing PLL at Fermilab

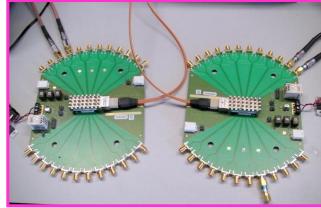
Integral and differential non-linearity OK



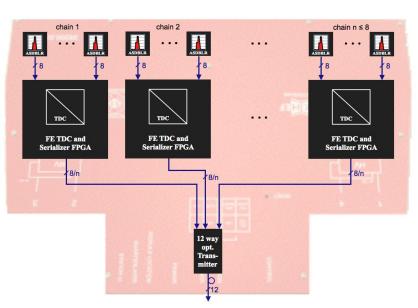


12-chan.
Transmitters
(industrial and common R&D with ATLAS)





OT FE 40 MHz Plans/Ambitions



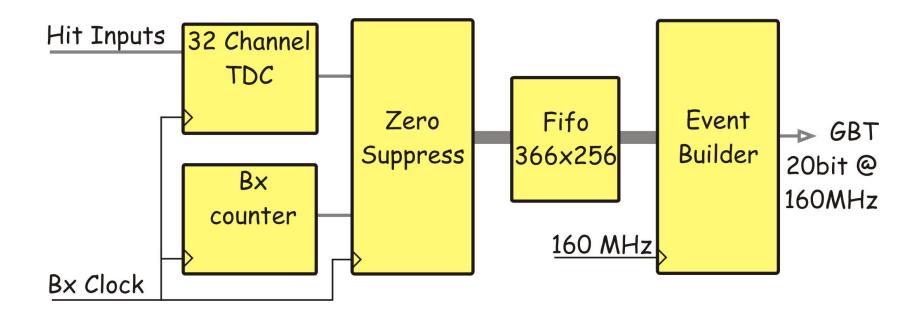
ID	_	Task Name		Duration	Start	Finish	Predecessors	D1 January 21 September 11 June 01 March 21 November 11 August
1	0	111011		0.000	Mon 04/04/11	Mon 04/04/11		
2	•	LHCb Letter of Inte	ent	O days	AN 04/04/11	Man 04/04/11		04/04
3	(OT Front-End R&D	The	880 days	Wed 01/09/10	Top 14/01/14		
4	>	TDC/TX Test		250 days	Wed 01/09/10	Tue 16/08/11		
5			L TDC (eval. Kit)	13 wks	Wwf.01/09/10	Tue 30/11/10		
8				13 wks	Wed 01/09/10	Tue 16/02/11		
_			d components TDC PCB					
′		PCB Schem		5 wks	Wed 16/02/11	Tus 22/03/11		
8		PCB Layout		8 wkz	Wed 23/03/11	Tue 17/06/11		
9			tion/assembly	2 mons	Wed 18/06/11	Tue 12/07/11		
10		Bench eval	action	5 wks	Wed 13/07/11	Tue 16/08/11		
	¥	Albert ready w		O days	Thu 31/03/11	Thu 31/03/11		_31\sqrt{3}
2		Stratix IV Rec	dout System	260 days	Wed 01/09/10	Tue 30/08/11		V
13		Test progr	am Stratix IV (eval kit)	13 wks	Wed 01/09/10	Tue 30/11/10		
4			rom Stratix (TCP/IP)	3 mons	Thu 31/03/11	Wed 22/06/11	11,13	
5			protocol into Stratix	15 wks	Wed 18/06/11	Tus 30/08/11	8	
6		Serial Transmi		431 days	Wed 01/09/10	Wed 25/04/12	-	
17		Snap12 va		431 days	Wed 01/09/10	Wed 25/04/12		
18	-			6 mons	Wwt.01/09/10	Tue 15/02/11		
19		Patter	n generator loop RX/TX	0 mons		-w 10/00/11		
				2 mons	Thu 23/06/11			
20			n loop with Stratix			Wed 17/08/11	,	
21			ion Tests	9 mons	Thu 18/08/11	Wed 25/04/12		
22		Optoblock	(ATLAS R&D) validation	200 days	Mon 14/03/11	Fri 16/12/11		
23		optopo	ck test board	7 mone	Mon 14/03/11	Fri 23/09/11	45	
24								↑
25		Patter	n loop with Stratix	3 mone	Mon 26/09/11	Fri 16/12/11	23,14	Time
28			d components	5 wks	Wed 31/08/11	Tue 04/10/11	15	
27		PCB Schem		5 wkz	Wed 06/10/11	Tue 08/11/11	26	
28		PCB Layout		8 wks	Wed 09/11/11	Tus 03/01/12		
29		PCB Produc		8 wkz	Wed 04/01/12	Tue 28/02/12		
30		Bench Evol		5 wice	Wed 29/02/12	Tue 03/04/12		
31				245 days	Wed 04/04/12	Tue 12/03/13		
		GOL/AUX++ Pr						
32			d components	8 wks	Wed 04/04/12	Tue 29/06/12		
33		PCB Schem		6 wkz	Wed 30/06/12	Tue 03/07/12		
34		PCB Layout		12 wks	Wed 04/07/12	Tue 26/09/12		
	*	GBT ASIC		0 days	Fri 29/06/12	Fri 29/06/12		● 29/06
36		Production	PCB	12 wks	Wed 26/09/12	Tue 18/12/12		
37		Bench eval	action GBT PCB	12 wka	Wed 19/12/12	Tue 12/03/13	36	
38		FEBox++ valido	tion	220 days	Wed 13/03/13	Tue 14/01/14		
39			Box++ Prototype	20 wks	Wed 13/03/13	Tue 30/07/13	37,30	
40			++ (also with straws)	3 mons	Wed 31/07/13	Tue 22/10/13		
41		Write TDR		3 mons	Wed 23/10/13	Tue 14/01/14	**	
42		OT Electronics		0 mons	Tue 14/01/14	Tue 14/01/14		
43	_	O1 Electronics	TUK	O MENS			71	
13				18 mone	Wed 31/08/11	Tue 16/01/13	45	
_		Upgrade FE-Tester						
	•	K.K. Gan TX availabl	•	O days	Mon 14/03/11	Mon 14/03/11		● J4402
46		OTIS++ Prototype		155 days	Wed 31/08/11	Tue 03/04/12		
_			Task		Progress			Summary External Tasks Deadline
oject:	OT Elect in 05/06	tronics Upgrade /11	_					<u>· · · · · · · · · · · · · · · · · · · </u>
30	00.00		Split		Milestone	•		Project Summary External Milestone
_								Page 1

Man-power ET:

- o TDC Board
- o optical transmitter
- serializer/transmitter board
- FE prototype + Tester

Man-power CT: \sim 0.5 FTE x 2y

TDC Schematics Overview



- Design of TDC in ACTEL Proasic3E FPGA because of the radiation properties
- 32 Channel 5 bit TDC (bin size 785 ps)
- Zero Suppress data format
- Output 20 bit LVDS @ 160 MHz to GBT
- I2C interface to set Mask Register, data format

Compile Report

Family: ProASIC3E

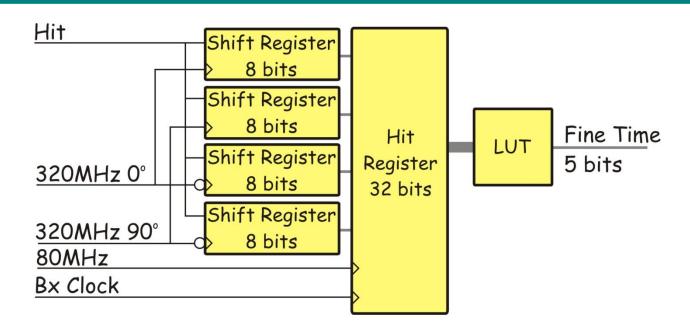
Device: A3PE1500

Package : 484 FBGA

Compile report:

CORE	Used: 21956	Total: 38400 (57.18%)
IO (W/ clocks)	Used: 127	Total: 280 (45.36%)
Differential IO	Used: 58	Total: 139 (41.73%)
GLOBAL (Chip+Quadrant)	Used: 6	Total: 18 (33.33%)
PLL	Used: 2	Total: 6 (33.33%)
RAM/FIFO	Used: 21	Total: 60 (35.00%)
Low Static ICC	Used: 0	Total: 1 (0.00%)
FlashROM	Used: 0	Total: 1 (0.00%)
User JTAG	Used: 0	Total: 1 (0.00%)

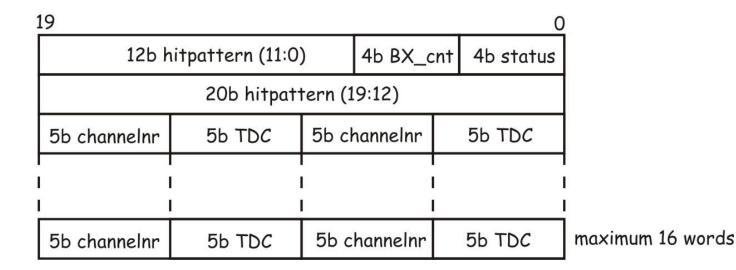
1-channel functional scheme



- PLL generates 3 clock signals; 8x Bx (320 MHz), 8x Bx (320MHz) phase shift 90°, 2x Bx (80 MHz)
- 4 Shifter registers, shifting on the positive edge and the negative edge of the 320 MHz clocks, dividing the Bx in 32 phases
- After each BX period the state of the shifter registers are latched in the Hit Register
- The LUT translates the 8 bit Hit Register into 5 bit time info

Data Format (prelim.)

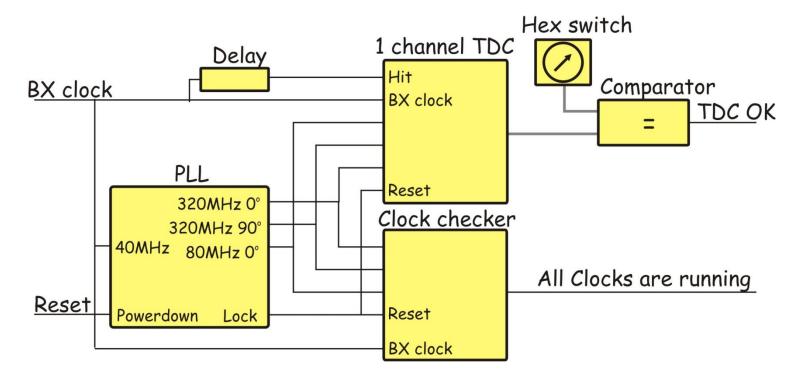
For the moment, use (redundant)



- Status register:
 - Bit(0) = truncate
 - Bit(1) = zero suppress
 - Bit(2) = fifo flag error
 - Bit(3) = spare

PLL tests under irradiation

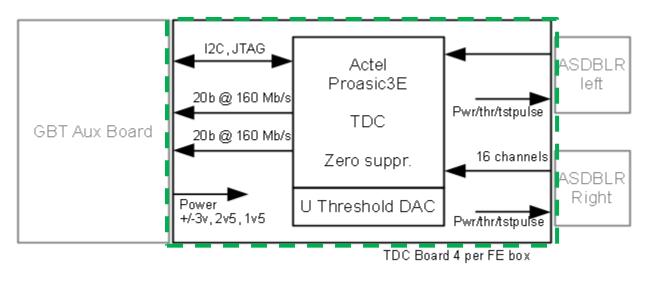
In cooperation with Syracuse (R. Mountain), results expected soon



- The 3 outputs of the PLL are used for the shifter clocks of a TDC
- The BX clock is delayed to get a synchronous Hit signal this gives a fixed TDC value
- The presence of the PLL clocks are continuously checked

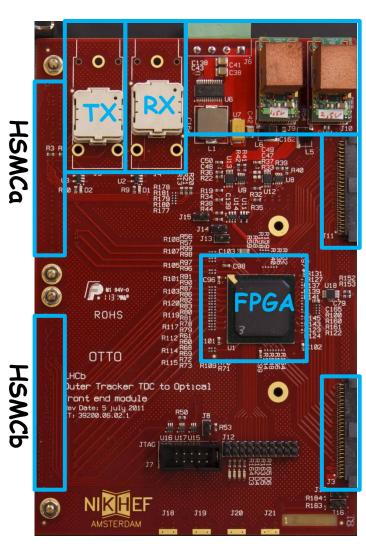
TDC Prototype Board (OTTO) Goals

- TDC board replaces OTIS board
 - → Identical mech. dimensions
- Actel ProAsic3E FPGA (one or two TBD)
 - → TDC 1(or 2) 16 channel inputs from ASDBLR
 - Zero suppression
 - → I2C controlled
- Threshold DAC (TBD)
 - Threshold voltage ASDBLR
- Interfaces GBT aux board
 - 20b @ 160Mb/s data bus to GBT

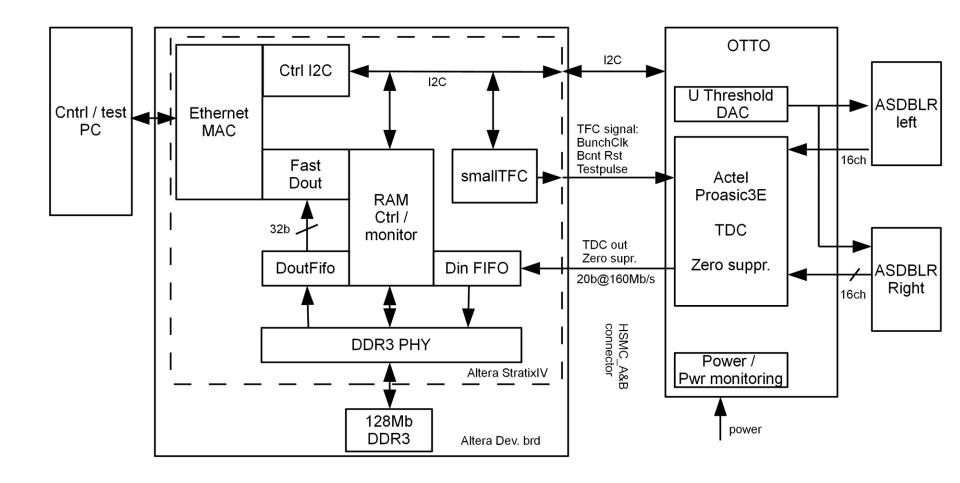


OT TDC to Optical (OTTO)

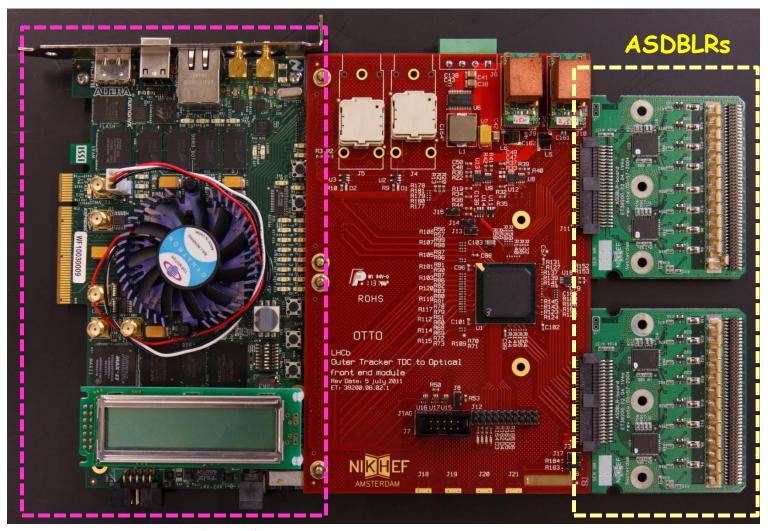
- First prototype OTTO
 - Ready for test
 - Actel ProAsic3eFGG494
 - ▶ 2 * 16 channel TDC in
 - ▶ 1 * 20bits@160Mb/s out to Stratix IV
 - Connect to stratix IV development board with HSMC connectors
 - Two ASDBLR connectors
 - → SM01C DCDC converters
 - Power monitoring, overcurrent protection (prevent latchup damage, radiationtest)
- Data analysis:
 - → 128MB DDR3(upgradable to 512)
 - Readout through 1Gb ethernet
- Second stage:
 - ➡ Include GBT (Tx/Rx) protocol in data path
 - Use "GBT-FPGA Firmware Starter Kit"



OTTO Test Setup (schematics)



OTTO Test Setup (the real thing)

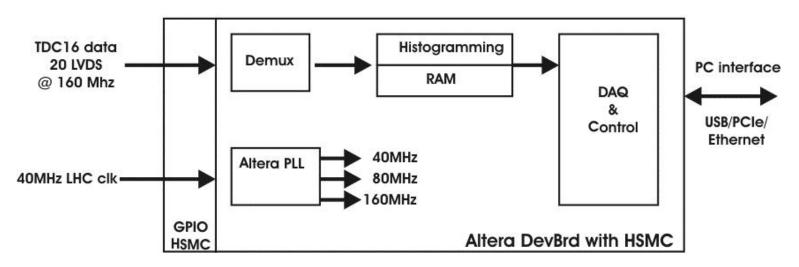


Stratix IV (readout and GBT emulator)

Test Board for TDC readout

- TDC Data analysis, without GBT data TxRx
 - → Analyze 32 channel TDC output (low testpule rate)
 - ➡ Analyze 16 channel TDC output (high testpule rate)
- 20 bits @ 160 Mb/s LVDS data interface with Actel 2*16ch TDC
 - → HSMC pio to interface TDC data bus

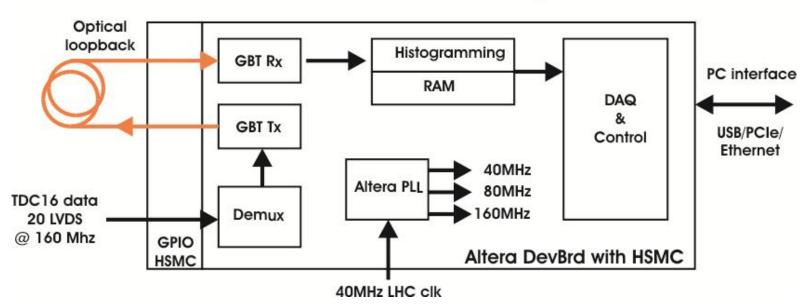
Actel TDC16 read out test setup without GBT



Test Board + GBT emulator

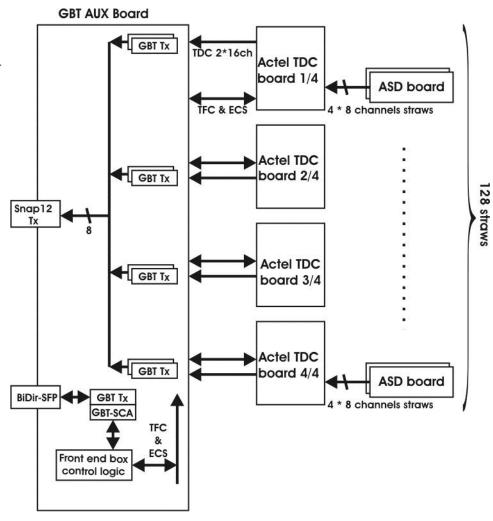
- Expanded with GBT Tx Rx loopback in data path
 - → 12 channel MPO TX/RX on OTTO proto pcb
 - **▶** Use "GBT-FPGA Firmware Starter Kit"
- Data analysis includes check of GBT data path

Actel TDC16 read out test setup with GBT



In reality what we want...

- GBT AUX board replaces Gol board
 - **▶** Identical mech. dimensions
- 8 GBT -> data transmission Snap 12 MPO opt. Tx
 - Option use of 4 Dual SFP Tx
- 1 GBT / GBT-SCA for TFC/ECS
 - **▶** Bidir SFP?
- Interfaces four TDC cards
 - → 128 TDC channels @ 40MHz



In Summary

- Combined functionality
 - TDC board (upgraded OTIS board)
 - 1/8 GBT aux board (upgraded GOL board)
- ☐ First proto based on Altera Stratix IV dev kit
 - 45GX230N expanded with High Speed Mezzanine Card OTTO
- □ Actel ProAsic APA1500 with 2*16 TDC channels(OTTO)
- □ GBT like data bus 20b @ 160 Mb/s
- □ Functionality:
 - Prove Actel TDC / ZS concept
 - Test GBT data transmission
 - Histogram of TDC Zero Suppressed data
 - Buffer burst of consecutive TDC output in RAM
 - · Offline analysis ZS data
 - Short runs, length to be defined depending on ZS and memory
- □ Data interface to host for offline analysis (proto only)
 - o Gb Ethernet

