



ATLAS and Beam Failures

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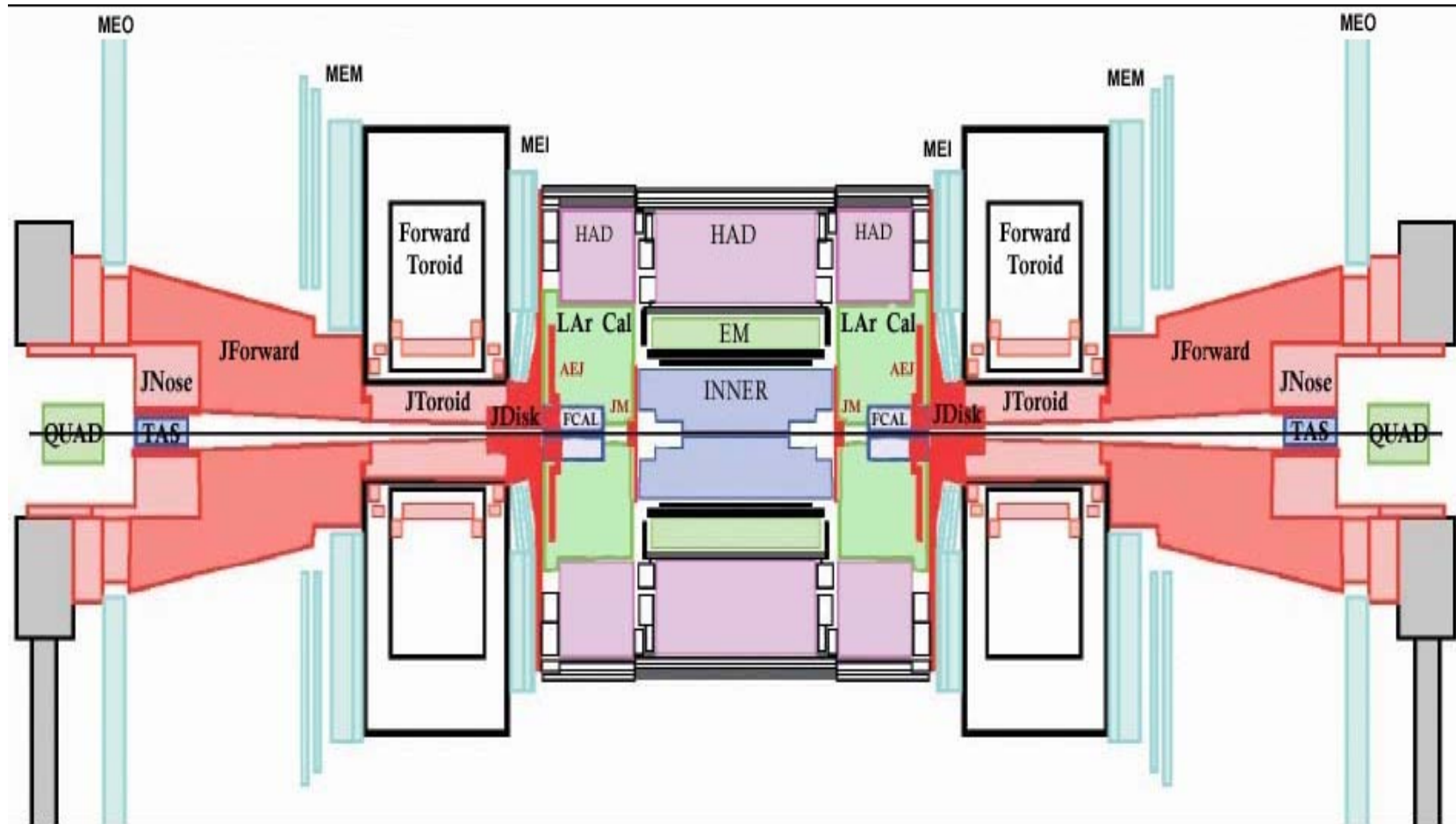
Workshop 12-06-07

The header features a complex network diagram with nodes and edges in various colors (blue, yellow, red) on a dark background. A red octagonal stop sign with the word "STOP" in white is positioned in the center, partially overlapping the network lines. Below the stop sign, the word "Outline" is written in a large, black, sans-serif font.

Outline

- Beam loss at injection
- Loss of circulating beam
- ATLAS BIS
 - Logic
 - Hardware solution
 - Status

ATLAS Experiment





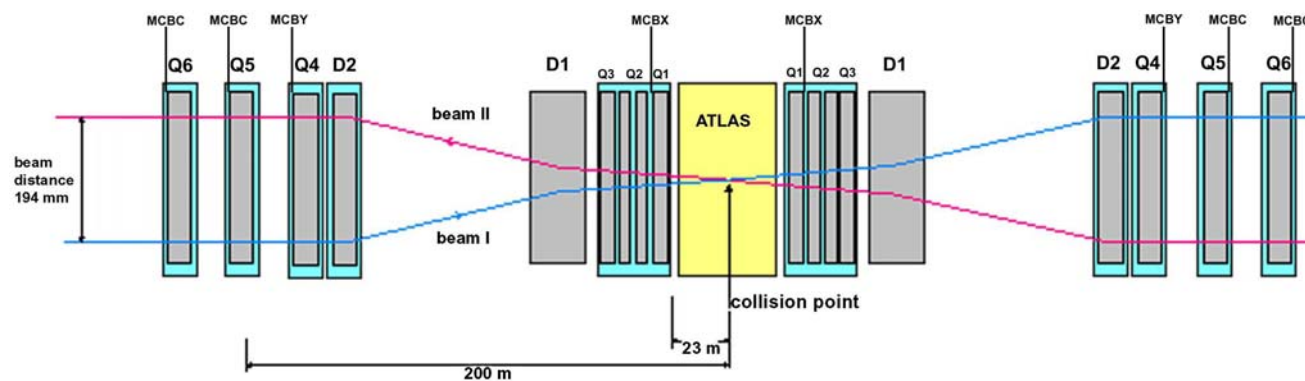
Beam Loss at Injection (1)

Studies based on

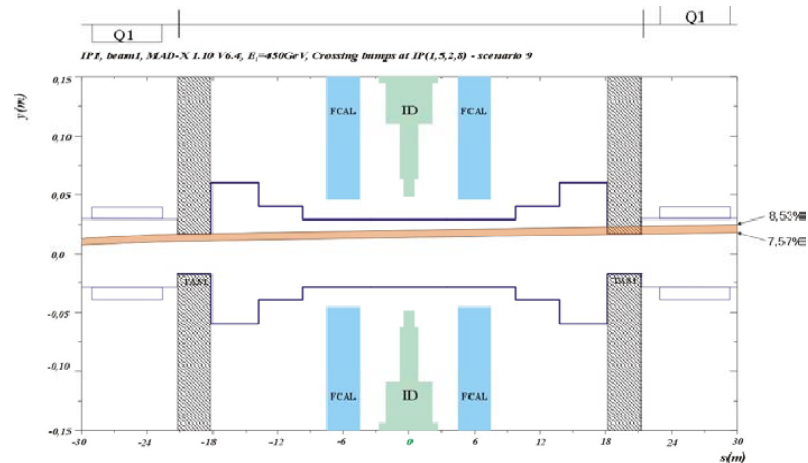
- Pilot bunch
 - Number of bunches: 1
 - Protons/bunch: 5×10^9
 - Proton momentum: 450 GeV/c
 - Bunch length (RMS): 11.2 cm
 - Beam size (RMS): 375 μm
 - Stored Energy: 360 J
- Certainly not on (safe beam) 10^{12} in empty machine

Beam Loss at Injection (2)

- LHC Project Note 335
Accidental Beam Losses during Injection in the Interaction Region IR1
Dariusz Bocian, January 2004
 - Various wrong settings of Magnets MCBXV, MCBXH, D1, D2
 - **Most critical setting scenarios ?**
 - Nominal setting only few percent of maximum strength
 - Wrong settings accordingly “small”
 - **What if setting close to the one for 7 TeV/c ?**

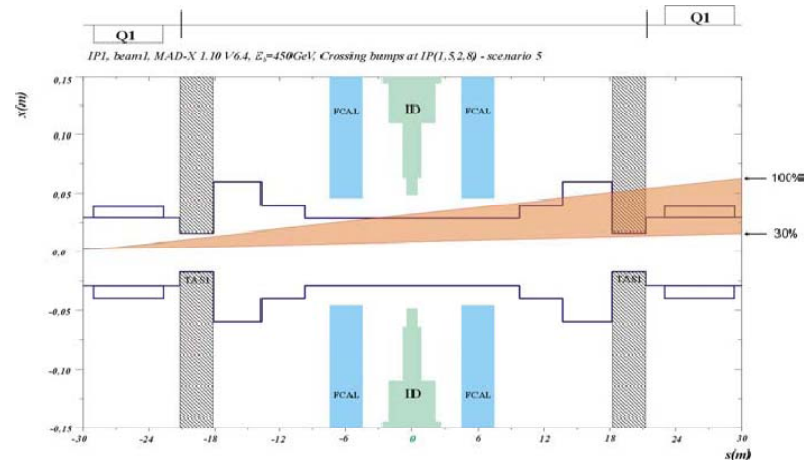


Beam Loss at Injection (3)



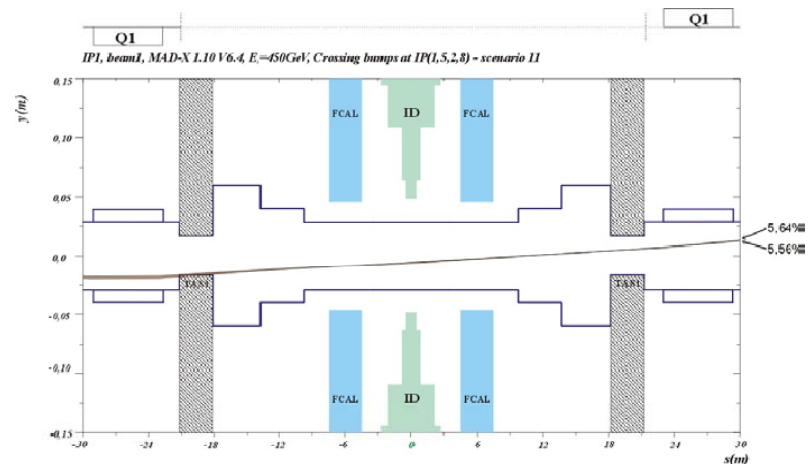
- Beam scrapes TAS towards IP (here: wrong setting of D1)
- Simulation of consequences for ATLAS detector
 - Muon system: o.k.
 - FCAL: o.k.
 - Pixel inner layer: 5×10^{-3} Gy → C. Gemme et al, *NIM A565, 2006, 50*
- Beam scrapes TAS from IP → 6.1×10^6 J in Q1

Beam Loss at Injection (4)



- Beam hits beam pipe near Pixel Detector (wrong setting of MCBX)
- Simulation of consequences for ATLAS detector
 - Muon system: ?
 - FCAL: Factor 27 more
 - Pixel inner layer: Factor 42 more

Beam Loss at Injection (5)



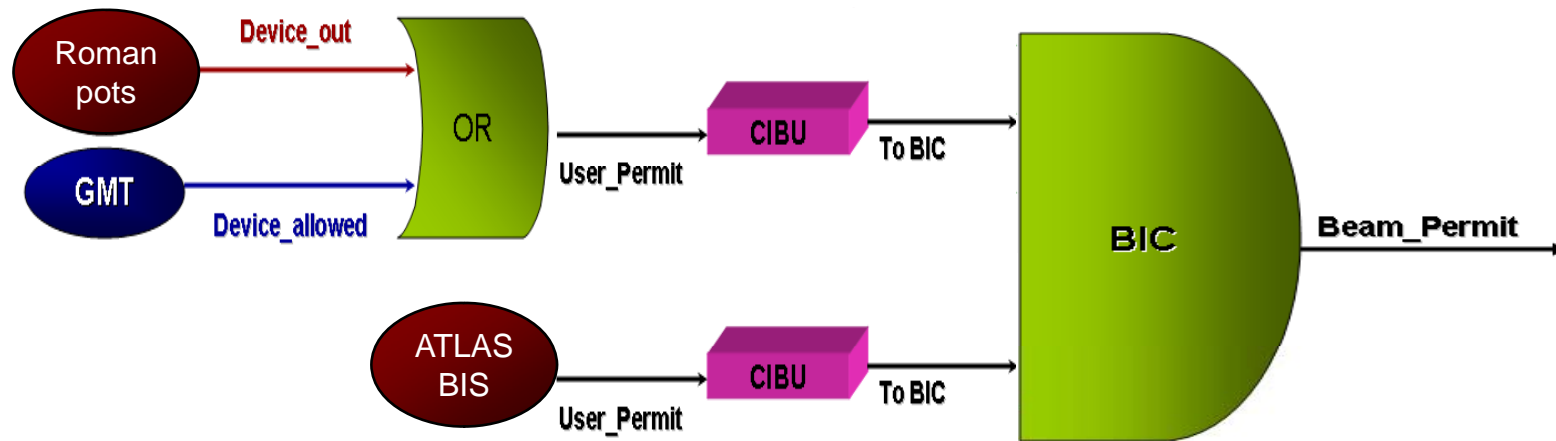
- Beam has large angle (wrong setting of D2)
 - 5.56% - 5.64% of max. strength (nominal 4.32%)
- What happens if field much higher (e.g. 7 TeV/c setting)?
 - Can beam bend into detectors ?
 - Or does it hit the TAS ?



Loss of Circulating Beam

- Machine protection should protect experiments
 - Collimation
 - Beam Loss Monitors
 - Long time constants in case of magnet failures
 - Also valid for safe beam mode ?
 - Where is last BLM ?
 - Can large bunch asymmetry lead to blow up at IP ?
 - How loss of vacuum close to IP is treated ?
- Nevertheless ATLAS will have beam interlock (part of LHC-BIS)
 - Protection of detector against eventual damage

ATLAS as User System

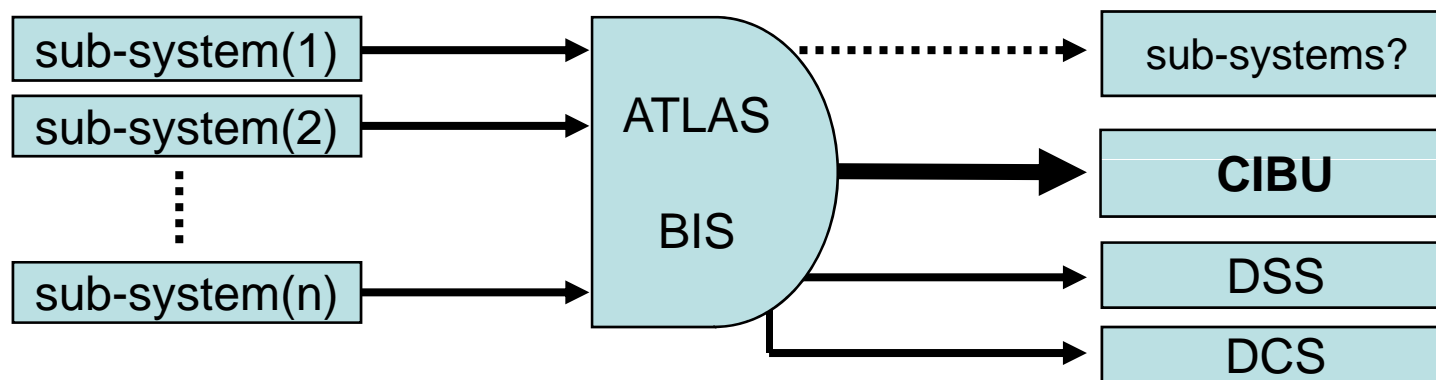


- CIBU-1 for ATLAS movable devices (Roman Pots)
- CIBU-2 for ATLAS sub-detectors

Realization of ATLAS-BIS

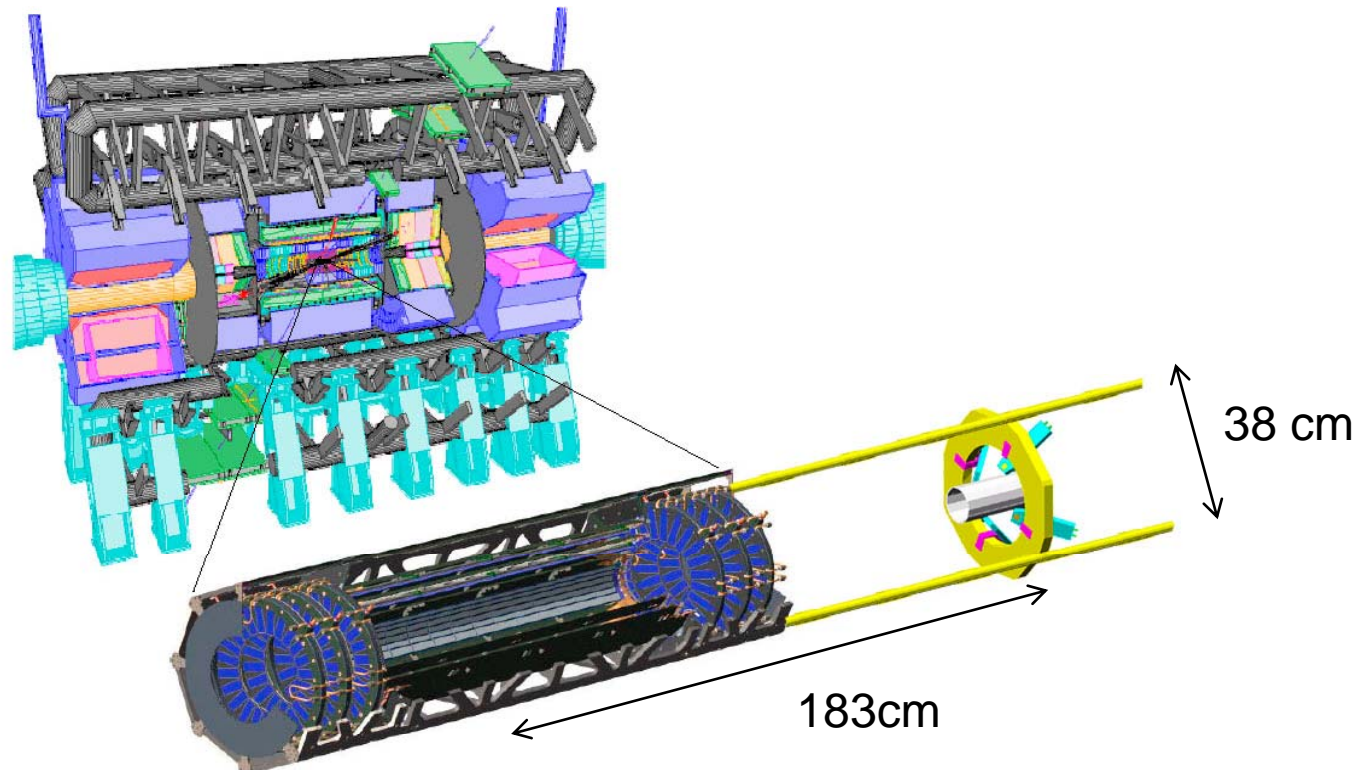
Follow logic of LHC-BIS

- Collect sub-system User_Permit signals
- Combinatorial logic creates ATLAS User_Permit for LHC-BIS
- If one sub-system User_Permit=False → beam dump request
- If beam dump request sent
 - Inform sub-systems via DSS for safety actions (slow)
 - Inform DCS
 - Inform sub-systems directly, if fast action needed

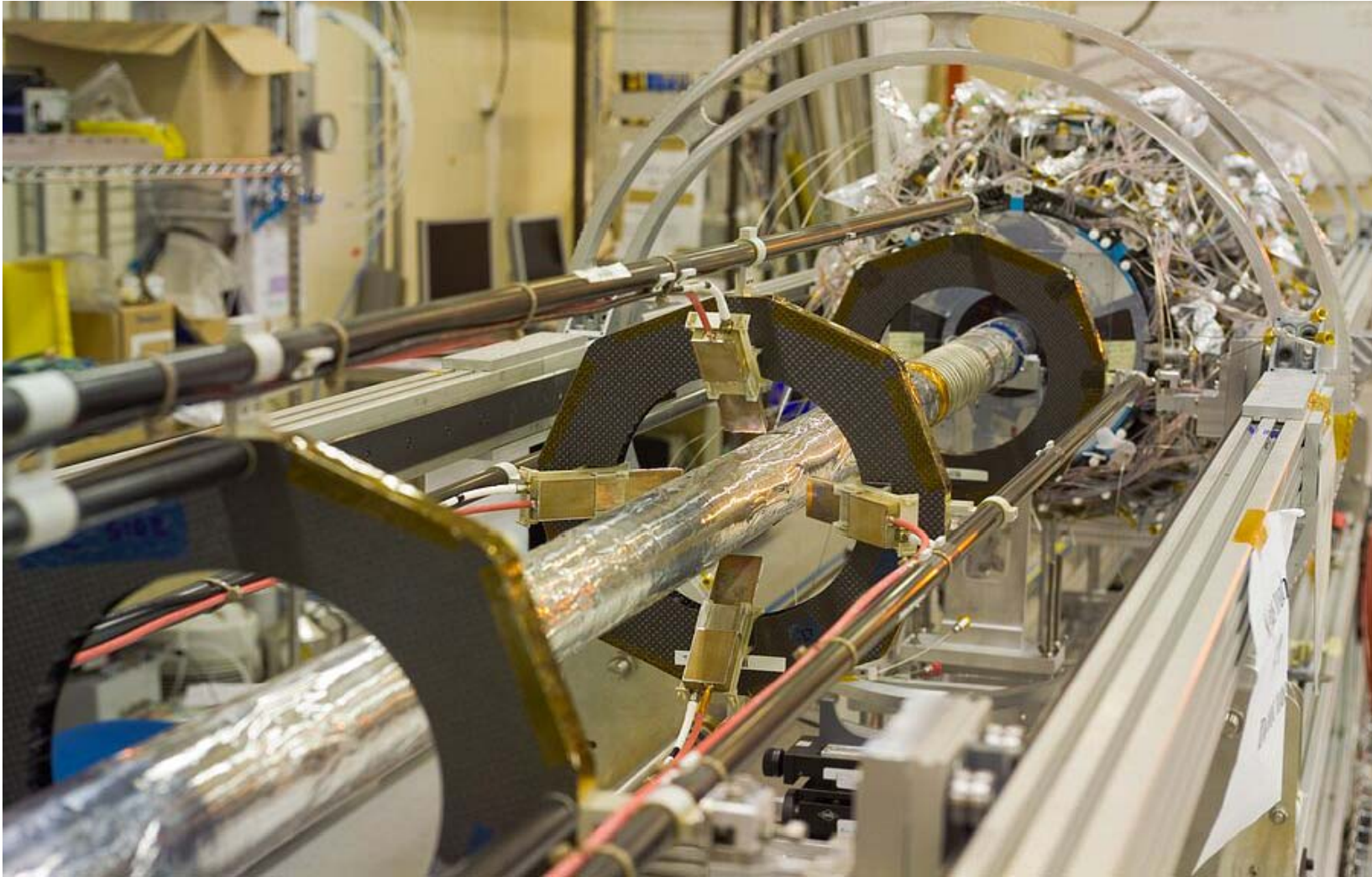


Sub-System(1) BCM

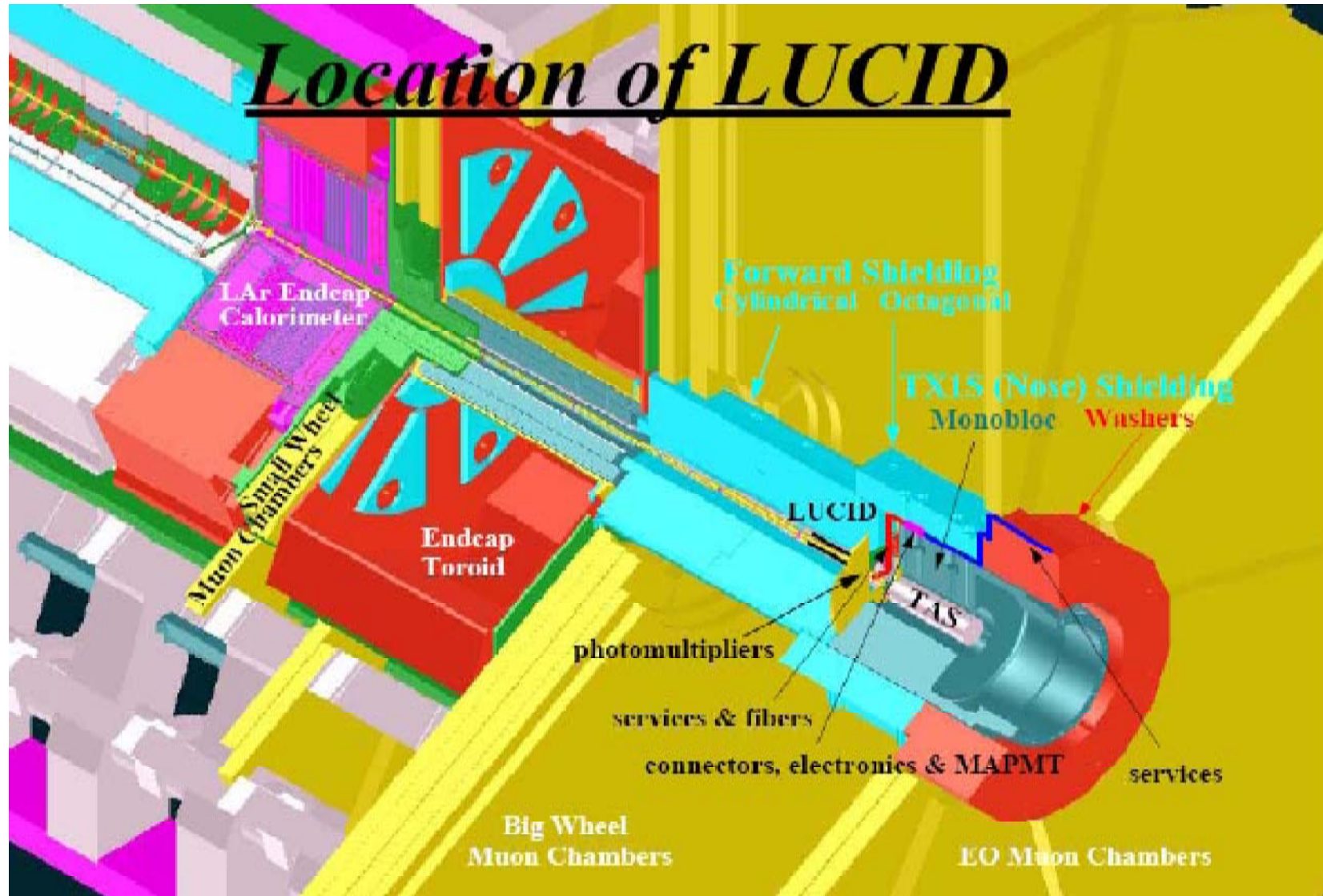
- 4 BCM stations on each side of the Pixel detector
 - Mounted on Pixel support structure at $z = \pm 183.8$ cm and $r = 7$ cm
 - Each station: 1cm^2 detector element + Front-end analog readout



ATLAS Beam Condition Monitors



Sub-System(2) LUCID



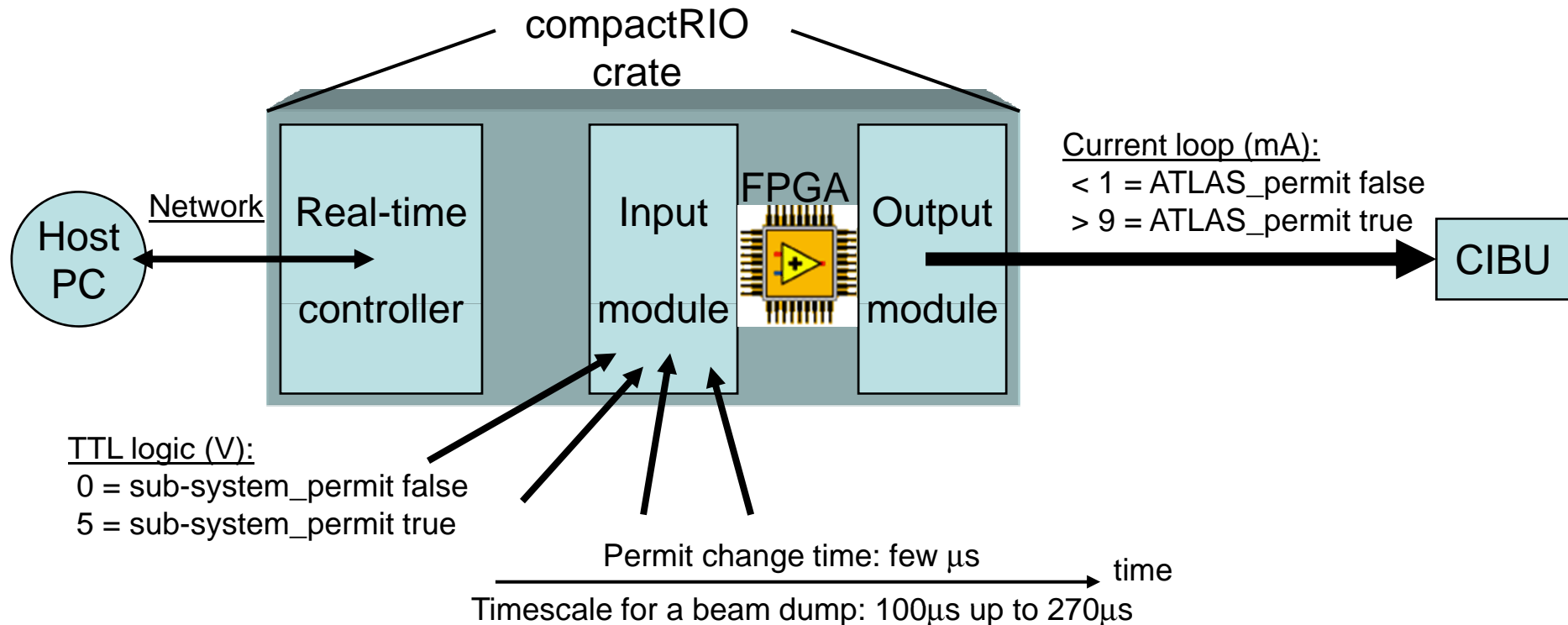


ATLAS-BIS SET-UP (1)

- Safety integrity level required leads to system based on hardware
- Studied 2 possibilities:
 - ASIC (application specific integrated circuit) chip not suitable:
 - Non-evolutive system (functionality defined at the very beginning)
 - Long development time
 - High cost
 - FPGA (Field Programmable Gate Array) well adapted:
 - Configured by programming the target (matrix of configurable-logic blocks surrounded by a periphery of I/O blocks)
 - Evolutive system with reconfigurable hardware after being put into service
 - Flexible and modular platform with a lot of different I/O modules

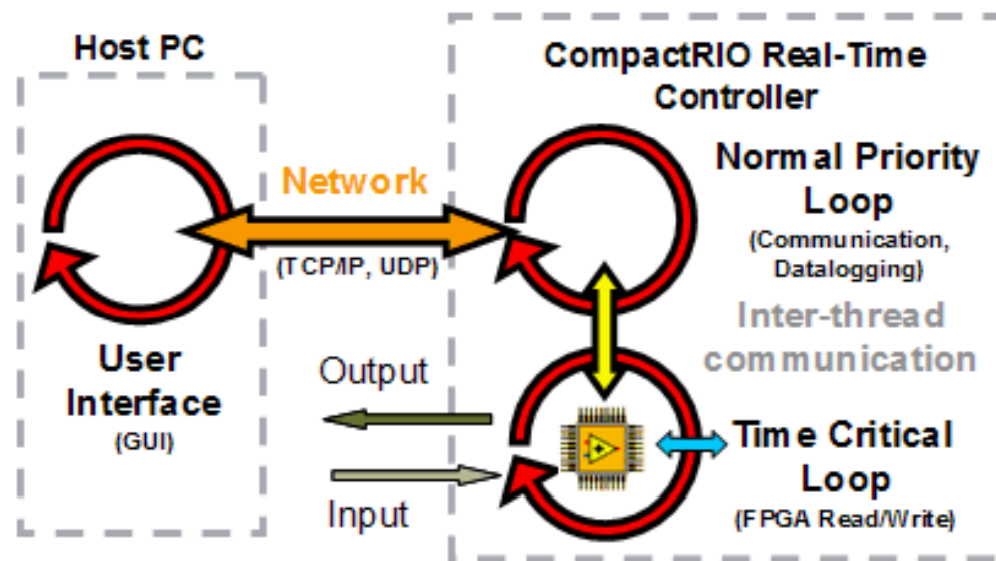
ATLAS-BIS SET-UP (2)

- Hardware interlock based on RIO technology
 - Custom hardware circuitry using reconfigurable FPGA chip
 - RIO core including FPGA chip + surrounding circuitry (I/O modules)
 - RIO core connected to a real-time controller



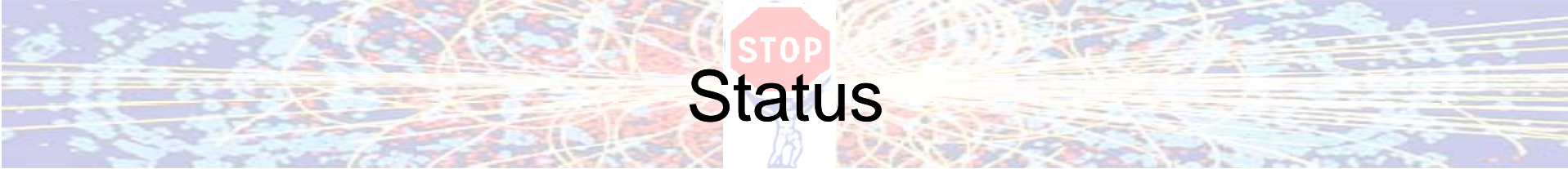
ATLAS-BIS SET-UP (3)

- Complete stand-alone embedded system
 - Critical logic and interlocks in silicon hardware circuitry: stand-alone, highest priority, non-interruptible loop
 - Data logging and ethernet communication performed by real-time controller: software loop to communicate with the FPGA
- External links and system monitoring
 - Link to DSS/DCS system via a dedicated output
 - Link to sub-systems via some specific channels if required
 - User interface on host PC via programmatic communication (TCP/IP)



Requirements of LHC-BIS for Experiments

- ✓ Send **hardware signal** (User_Permit) to CIBU
 - User-Permit = True → Beam_Permit = True
 - User-Permit = False → Beam dump request
 - User-Permit = False and no beam → Injection inhibit
- ✓ Redundancy
 - 2 independent systems
 - 2 independent hardware signals
- ✓ Post-Mortem Analysis
 - Reason(s) for beam dump request will be available (for all ?)
- ✓ System will be operational and fully reliable well before first injection
 - Un-maskable on LHC side
- ✓ System will be on UPS
 - Even stand-alone UPS (as rack is shared)



Status

- Participating Sub-systems identified
 - BCM
 - LUCID
- Hardware solution found
- Hardware purchased and delivered
- Programming course taken
- Setting up and programming started
- Aim at
 - Having first test loop operational end of August
 - Having system fully operational end of 2007
 - Assuring possibility for extension and maintenance