

Status report on the 3D sensor development @FBK

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Outline

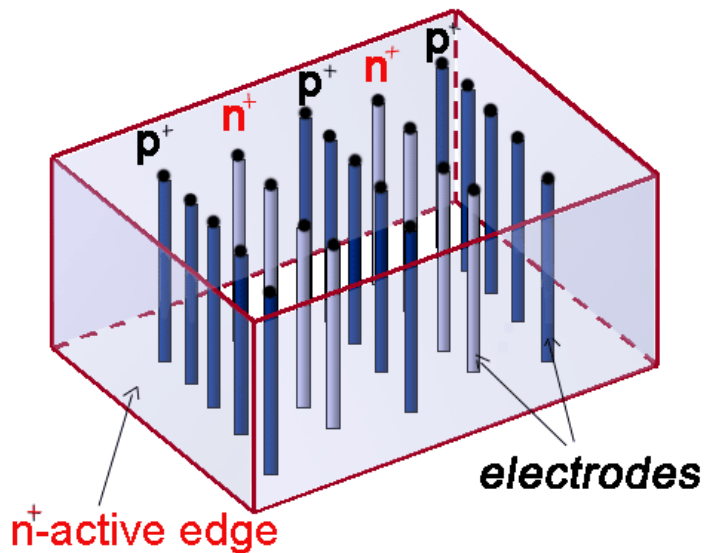
- Process development @ FBK
 - Main technological steps
- Layout
 - Temporary metal
- ATLAS pixel IV characteristics

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3D detectors

First proposed by S. Parker et. al.
in NIMA 395 (1997), 328



Best result:
66% of the original signal after
 $8.8 \times 10^{15} \text{ cm}^{-2}$ 1-MeV n_{eq} fluence

C. Da Via et. al.
 NIMA 604 (2009) 504

ADVANTAGES:

- Electrode distance and substrate thickness decoupled:
 - low depletion voltage
 - high speed
 - good charge collection efficiency
 → **High radiation hardness**
- Active edges:
 - Dead area reduced up to few microns from the edge

DISADVANTAGES:

- Non uniform response due to electrodes
- **Complicated technology**
- Higher capacitance with respect to planar

3D Technology Developments @FBK

NON Passing through columns tech.

A. Zoboli et al., IEEE TNS 55-5, 2008

Hole Depth

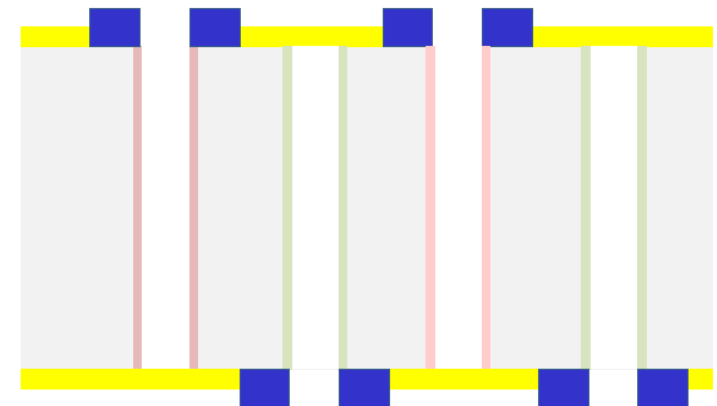
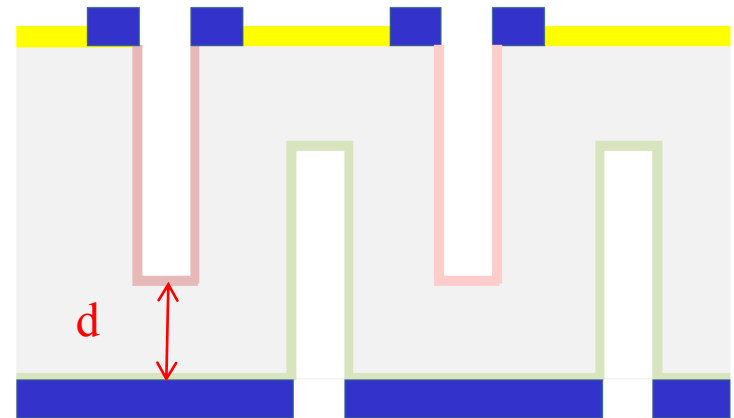
It's a critical parameter on 3D devices
d much smaller than wafer thickness

It's not easy to control, it depends on:

- ✓ Wafers thickness
- ✓ Etch rate
 - ✓ equipment status
 - ✓ uniformity on wafers
 - ✓ uniformity w to w
- ✓ Hole diameter (lithography)

Solution

Passing through columns



3D-DTC with passing through columns

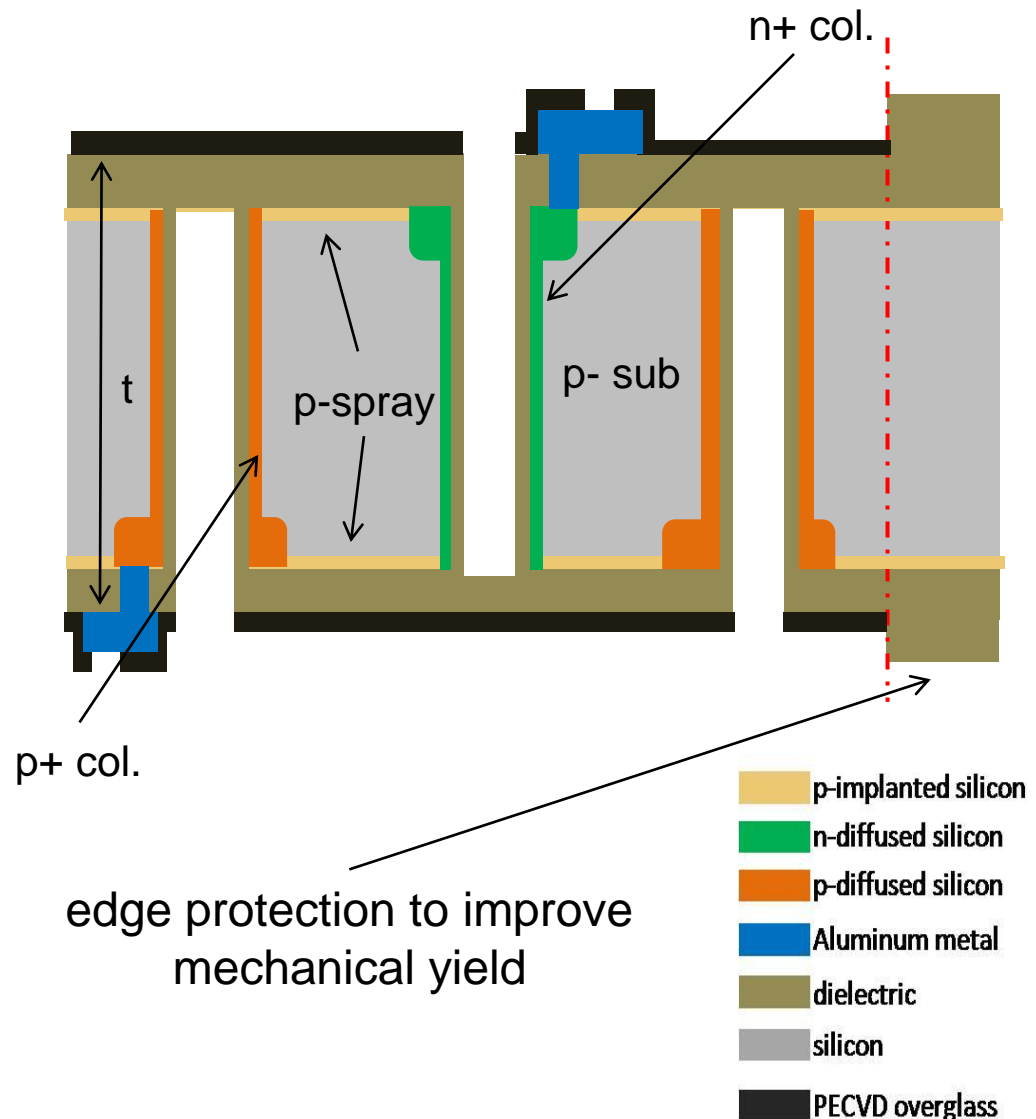
FABRICATION PROCESS

- holes (~11 μm diam.) are “empty” (no poly-Si)
- column depth equal to the wafer thickness
- no support wafer



full double side process

- isolation by p-spray
- Edge protection



Outline

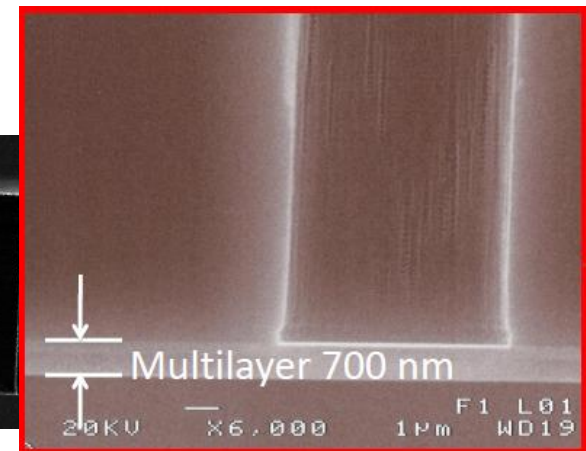
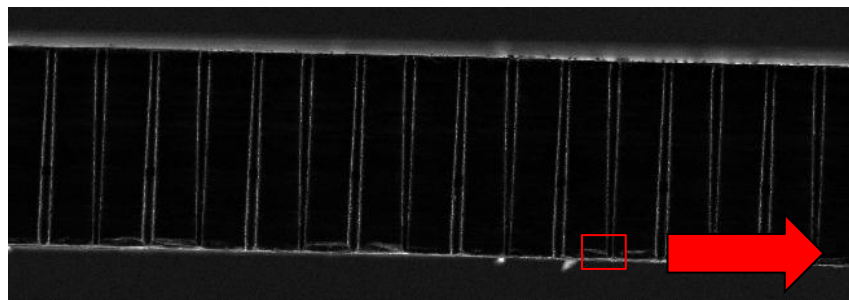
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Optimize DRIE recipes for holes with higher aspect ratio



Optimization of DRIE recipes in order to

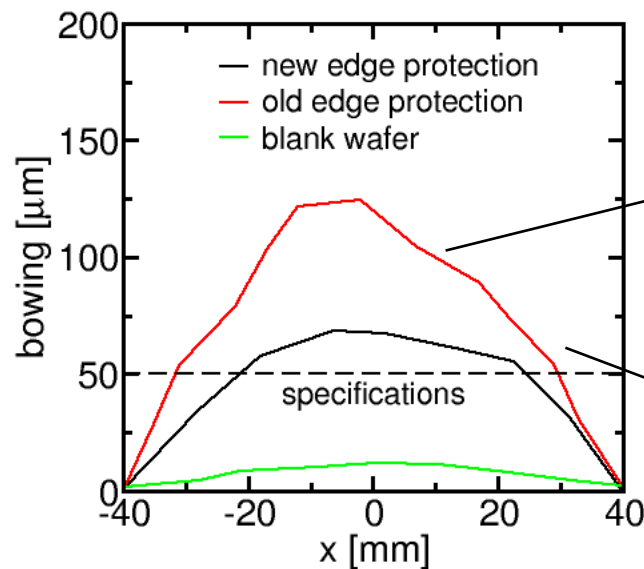
- increase the uniformity of the etch rate
- decrease the overall etching time
- Increase the aspect ratio
- Avoid notching



We use a DRIE with **electrostatic clamping** better thermal contact but we need an **edge protection** in order to improve the mechanical yield

Wafer bowing: leakage current

the wafer bowing is mainly influenced by the edge protection

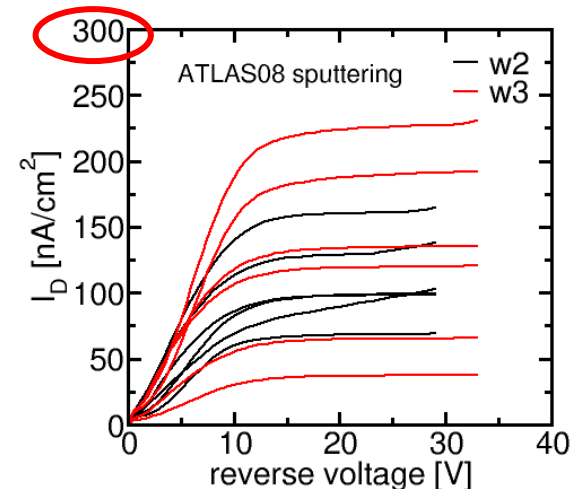
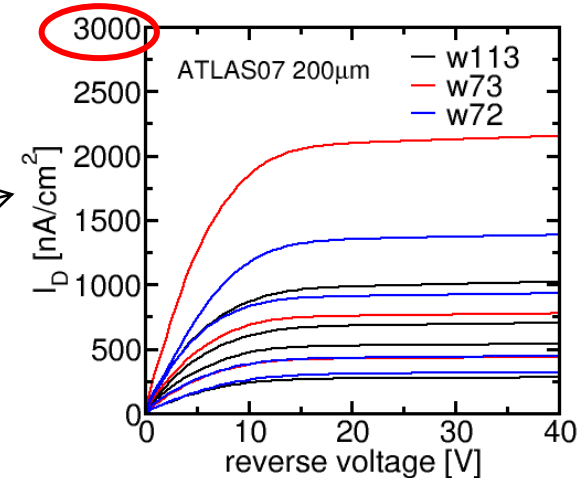


old

new

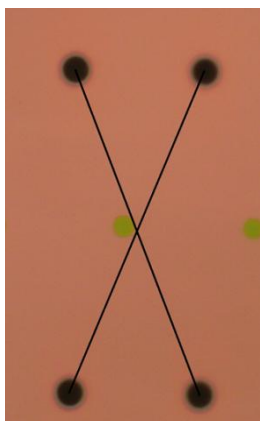
wafer bowing strongly influences the leakage current, in the new process it is reduced by one order of magnitude

Leakage current:
planar test diodes (4mm^2)

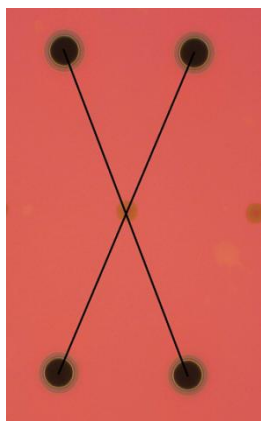


Wafer bowing: Column alignment

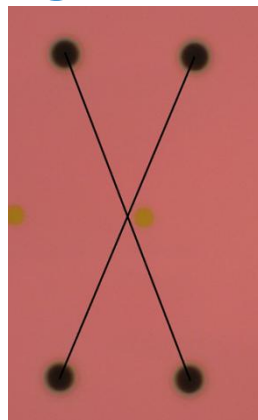
left side



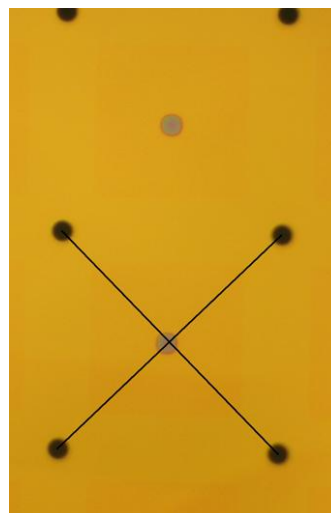
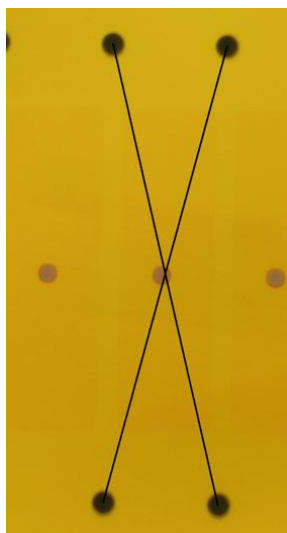
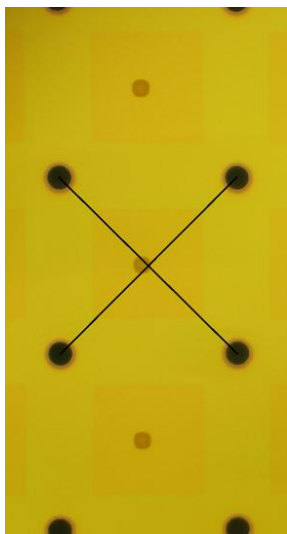
center



right side



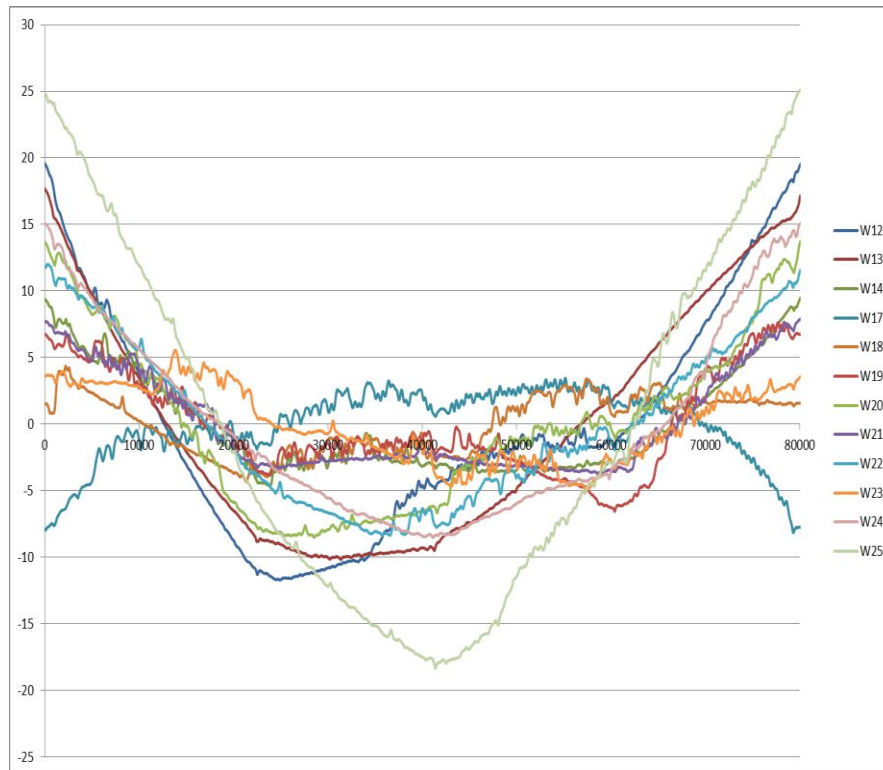
old process
misalignment of a
several μm



new process
(optimized
protection layer)
misalignment $< 5\mu\text{m}$

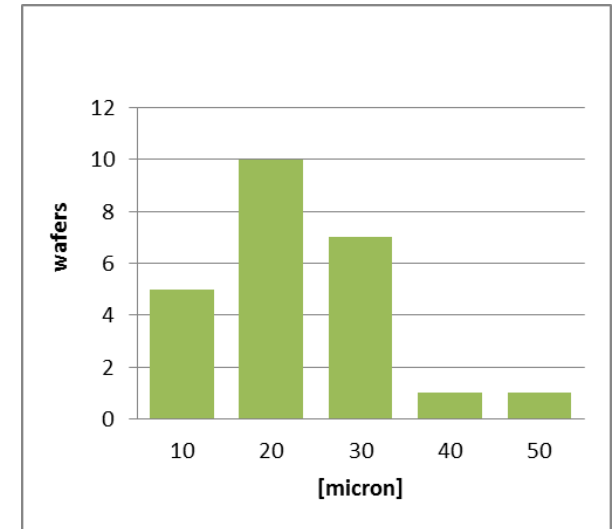
Optimized process technology

- «new» process wafers warp less than 30 micron



← →

8cm



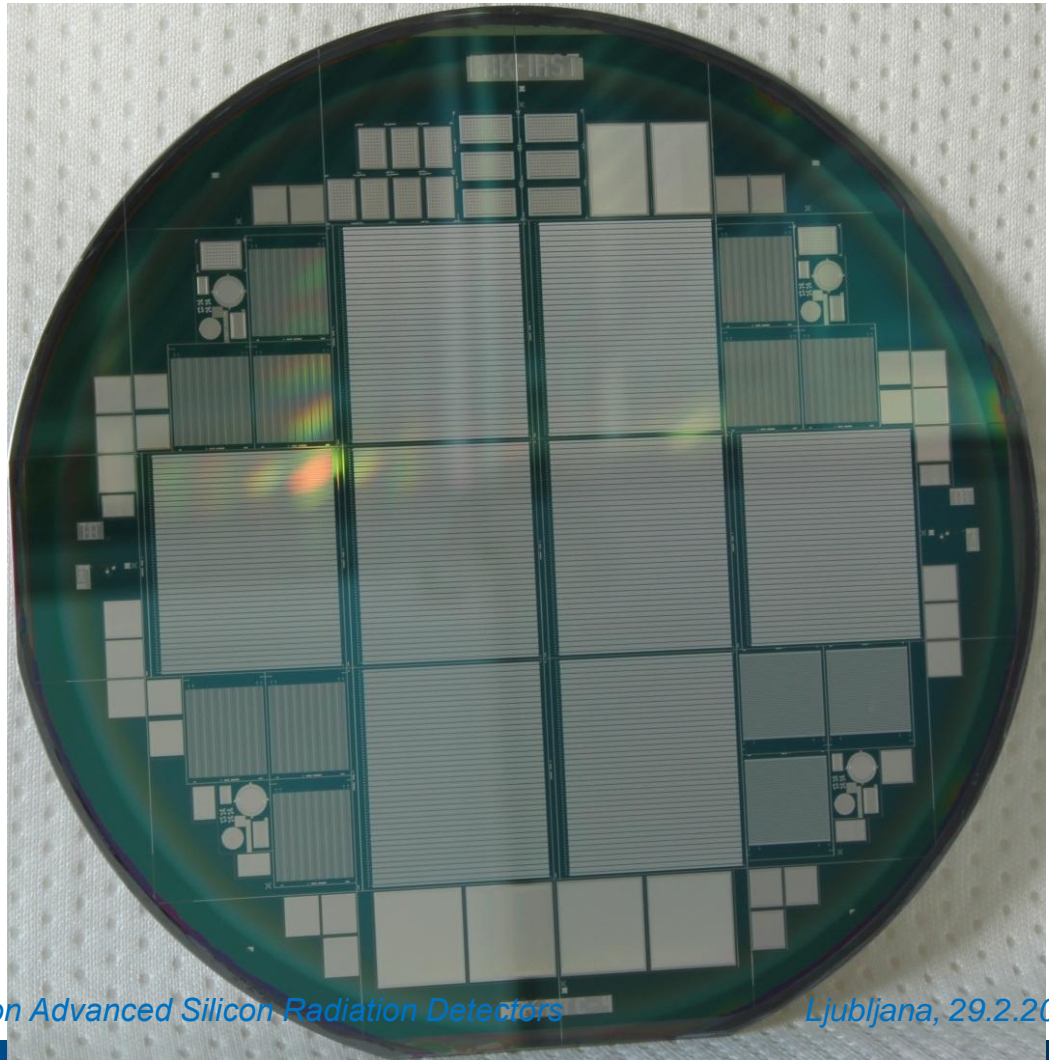
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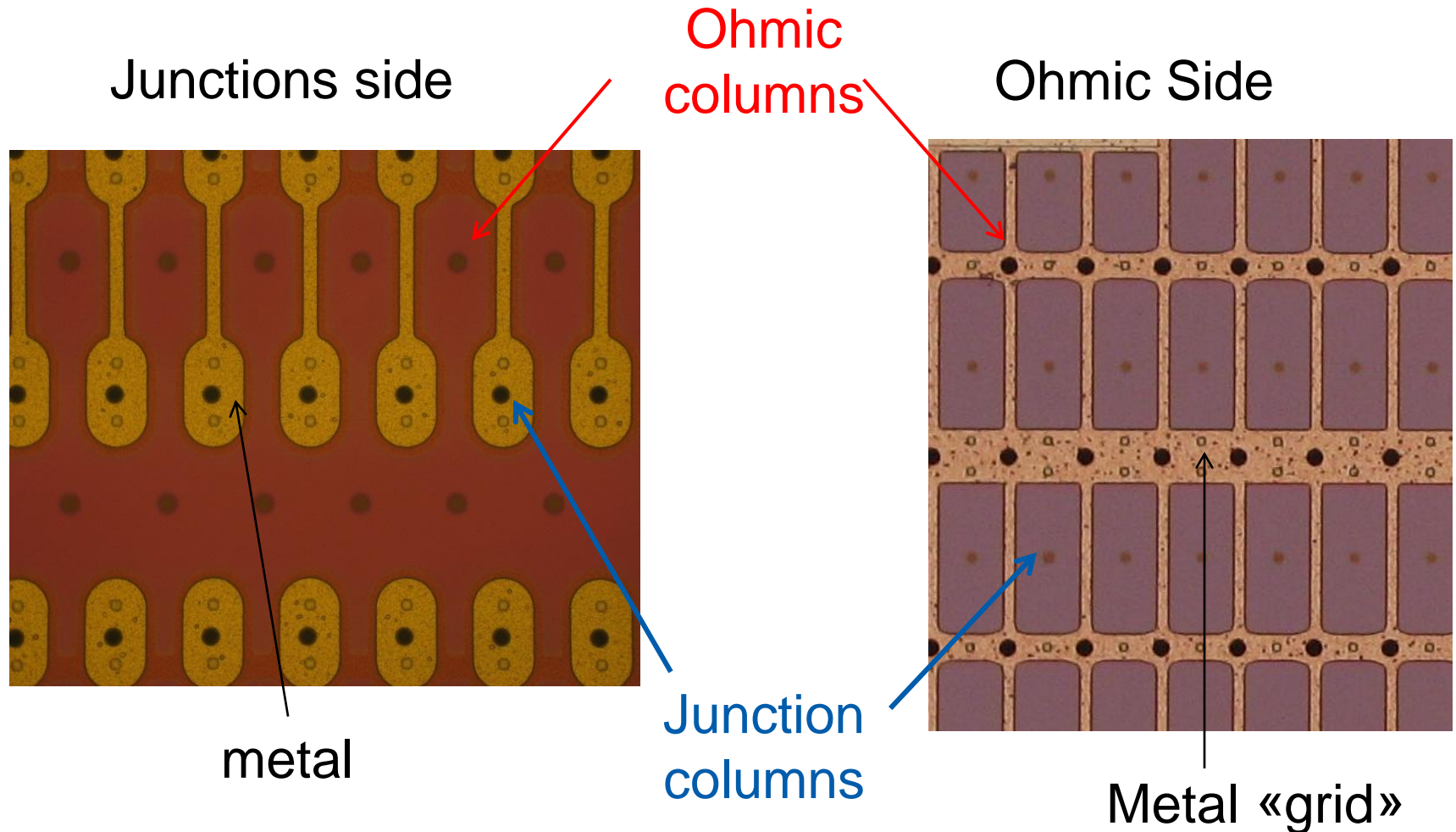
Wafer layout

The layout has been developed in the framework of the ATLAS 3D Sensor Collaboration

- FE-I4 (8x)
- FE-I3 (9x)
- CMS (3x)
- test structures

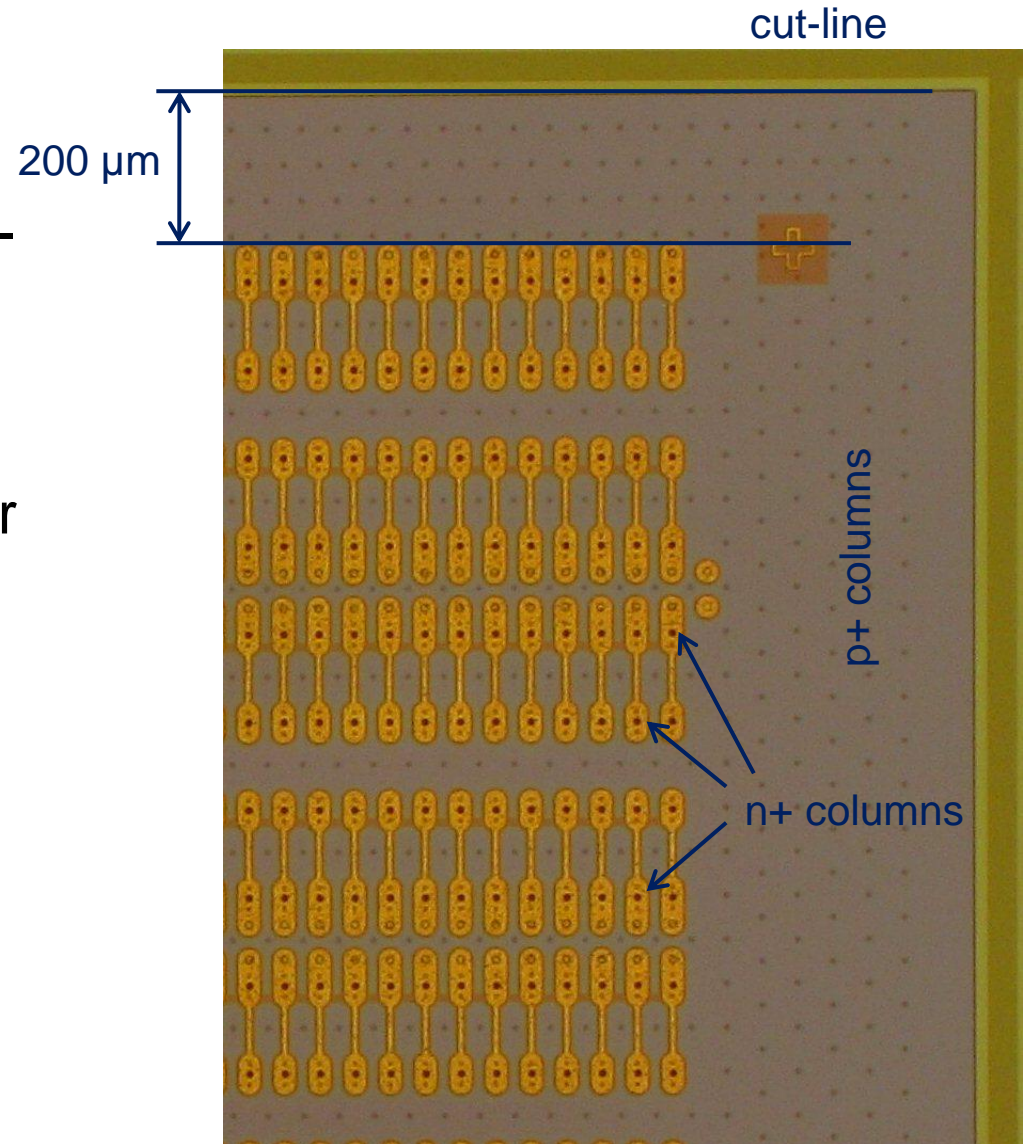


Pixel detector



Detectors Edge

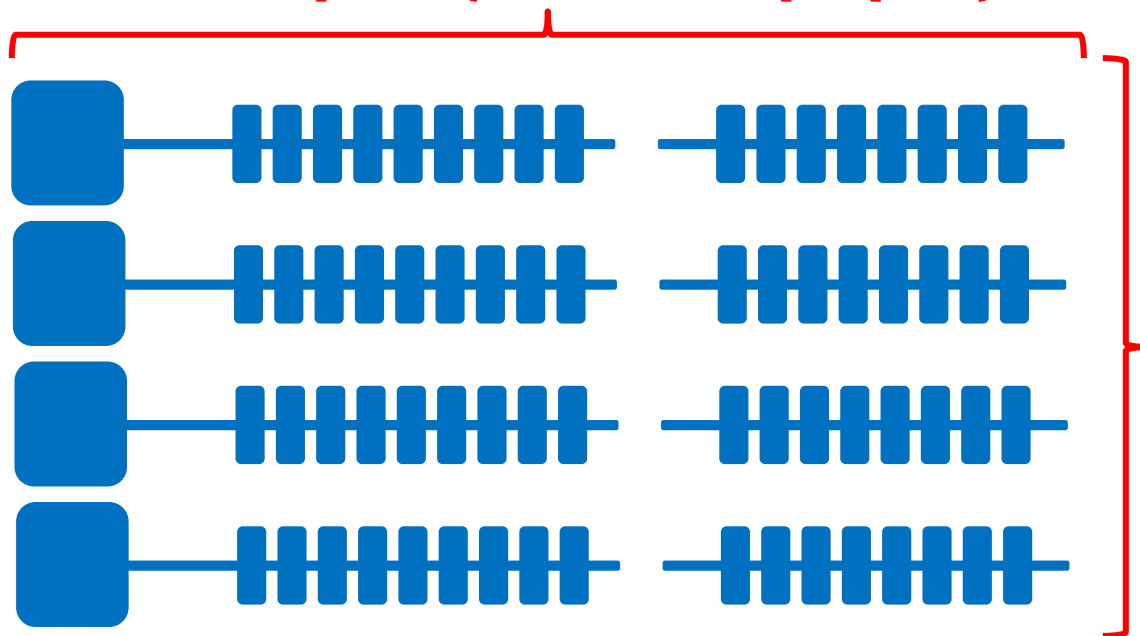
- Substrate bias from the back-side (also suitable for dual-readout pixel/strip detectors)
- No active edge, but allows for “slim-edge” detectors
- But It's not possible to characterize the detectors before bonding



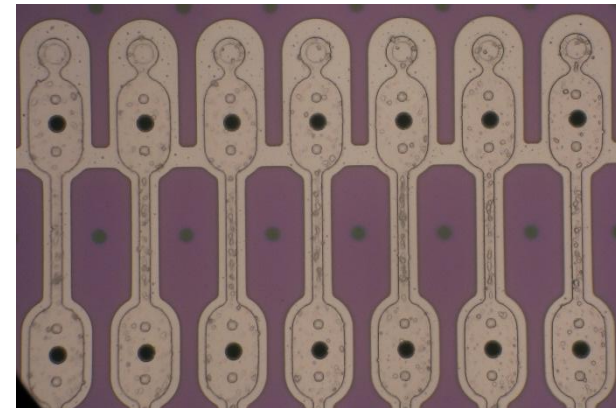
Temporary metal

- The temporary metal shorts 336 pixels together in a strip
- Allows to perform electrical tests on the FE-I4 pixel sensors before bump-bonding
- The IV characteristics of 80 strips form a FE-I4 pixel sensor

336 pixels (2 electrodes per pixel)



80 columns



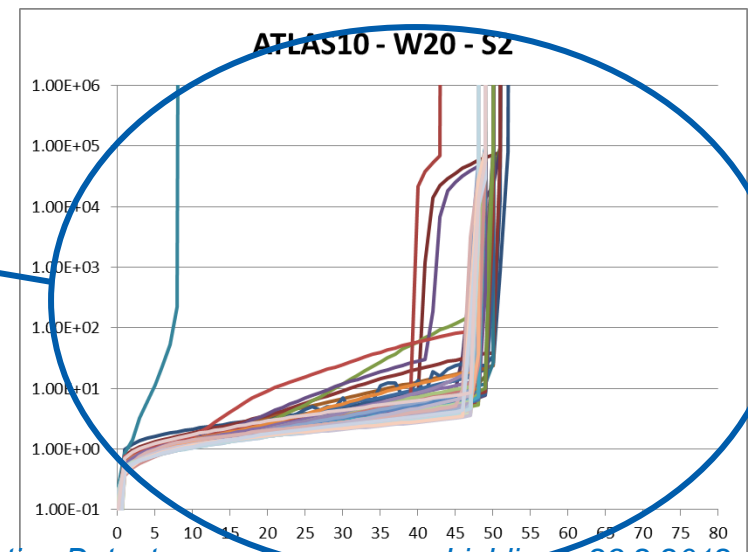
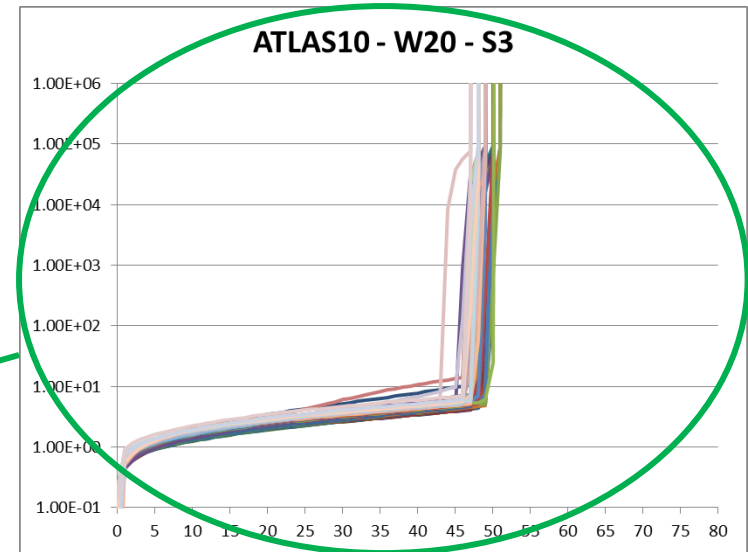
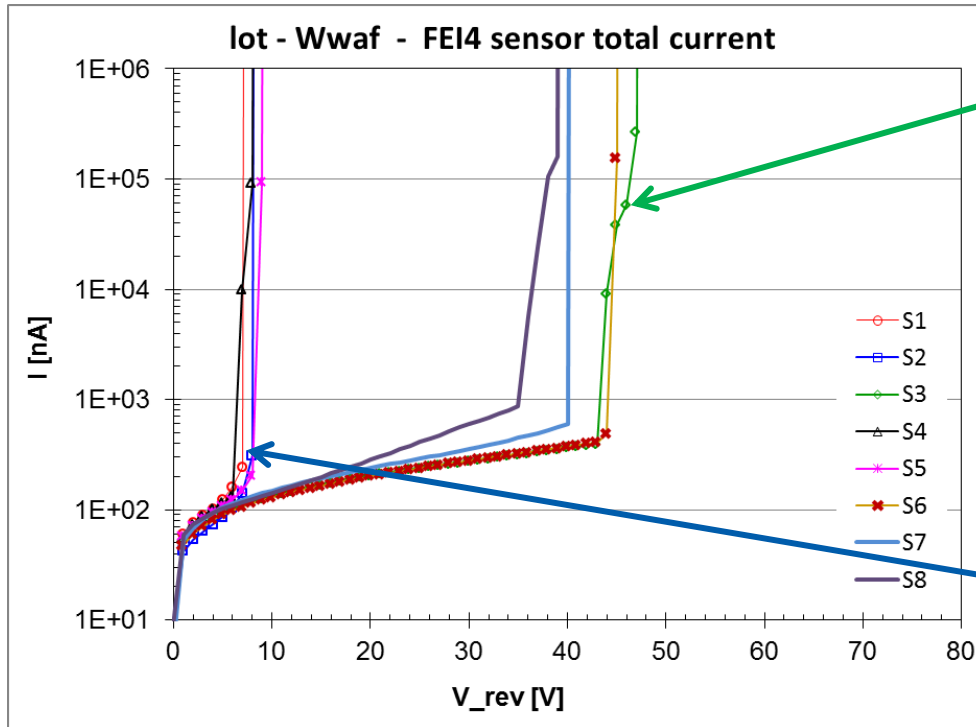
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Electrical characterization

- In the next slides we report some results (IV curves) obtained on the first batch produced for ATLAS IBL 3D pixel
- The IV curves have been obtained using temporary metal realized on detectors compatible with FE I4
- Others two batches are under processing in FBK lab.

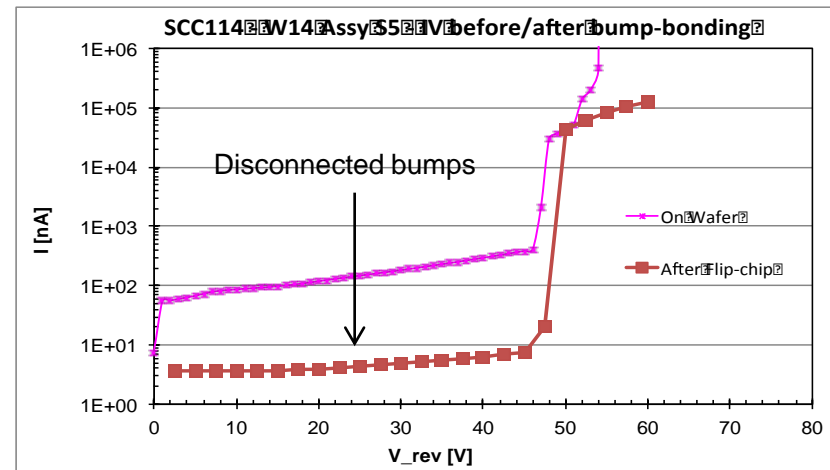
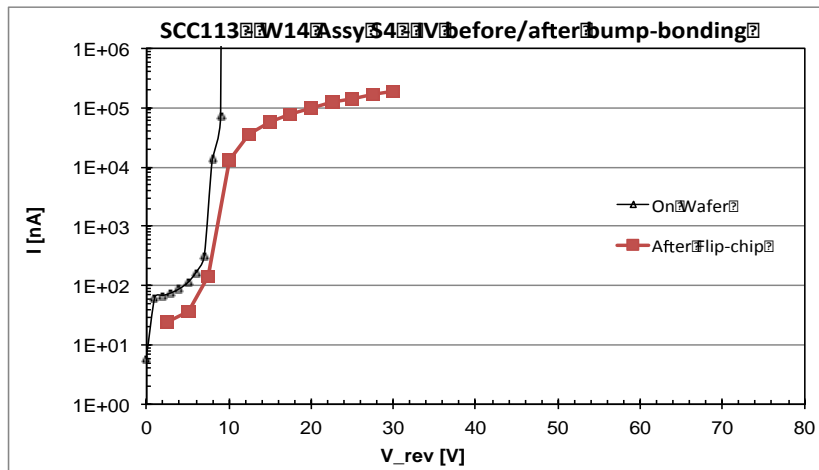
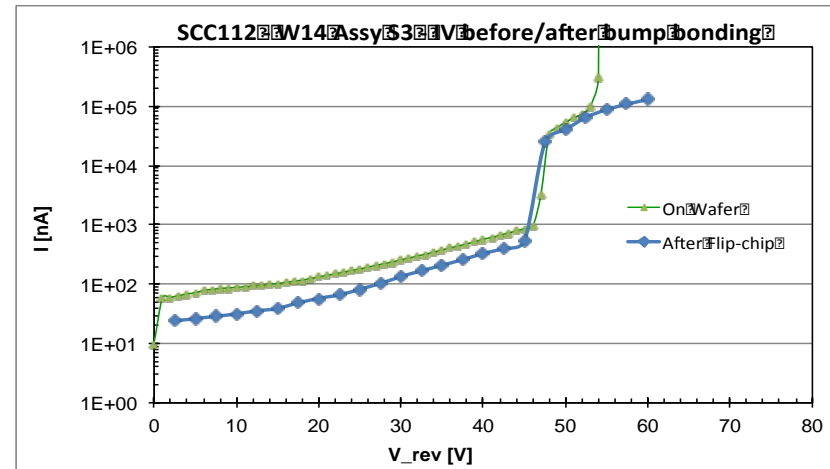
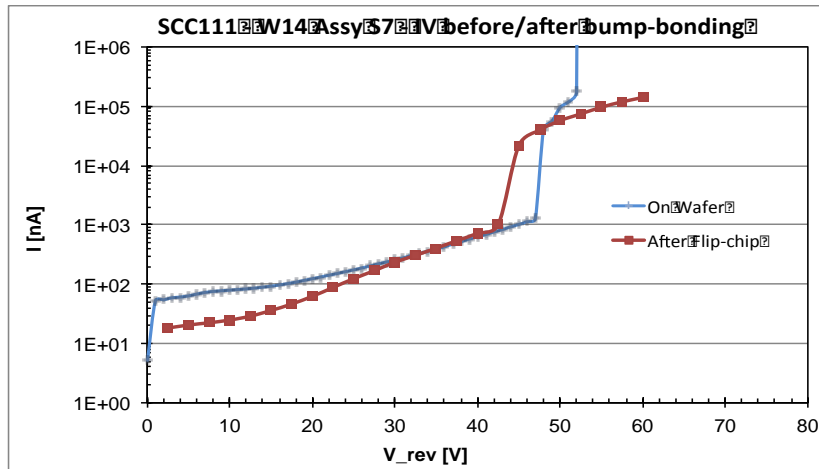
Temporary Metal: IV characteristics



The IV characteristics of FE-I4 pixel sensor as
a sum of 80 IV curves

before and after bump-bonding

D-L. Pohl, C. Gemme, G. Darbo



The bump bonding has been performed at IZM (Berlin)

Yield: a preliminary estimation

The following specifications are required by ATLAS to qualify a device as functioning correctly before bump-bonding:

- $V_{\text{depl}} \leq 15\text{V}$ and
- $V_{\text{op}} \geq V_{\text{depl}} + 10\text{V}$
- $I(V_{\text{op}}) < 2\mu\text{A}$ per tile
- $V_{\text{bd}} > 25\text{V}$
- $[I(V_{\text{op}}) / I(V_{\text{op}} - 5\text{V})] < 2$

yield (on first production batch)

On 21 wafers (2 broken = mechanical yield)

42% in spec

58% not in spec (but 8% are in at limit condition)

Ongoing Activity

	Total good Wafers *	Total sensors	Good sensors	Yield (%)
A10	12	96	58	60.4
A11**	4	32	14	43.7

FBK is producing two more batches of 3D for ATLAS IBL that will be completed by middle of march and end of april

* Wafers with at least 3 good sensors

** Unfortunately, due to a major problem in the clean-room, a large number of wafers from the FBK2 batch could not be properly completed.

Summary

- FBK has developed and optimized Si 3D technology based on pass through columns without the use of support wafers
- A temporary metal has been developed to allow a characterization of Si 3D pixel sensors before bump bonding
- FBK is producing two more batches of 3D for ATLAS IBL