Development of novel KEK/HPK n^+-in-p silicon sensors and evaluation of performance after irradiation

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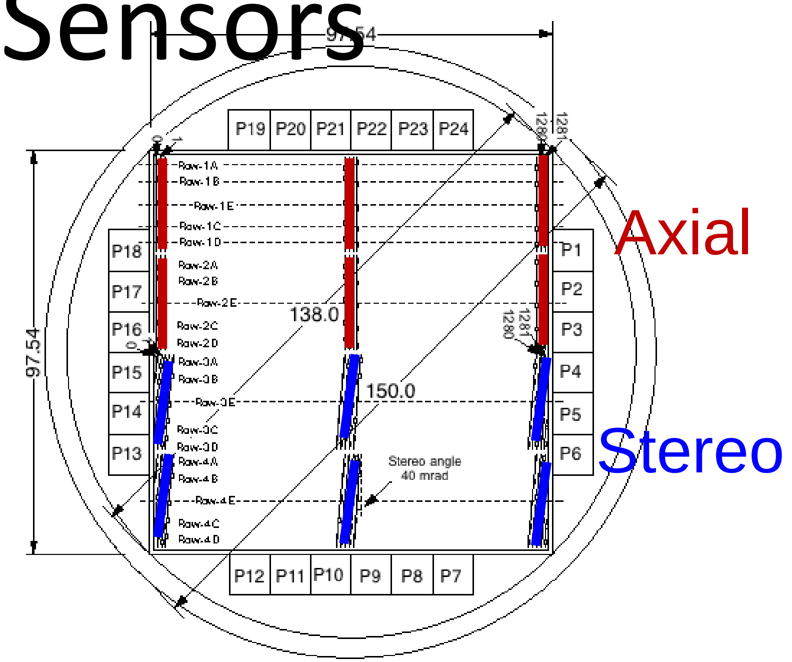
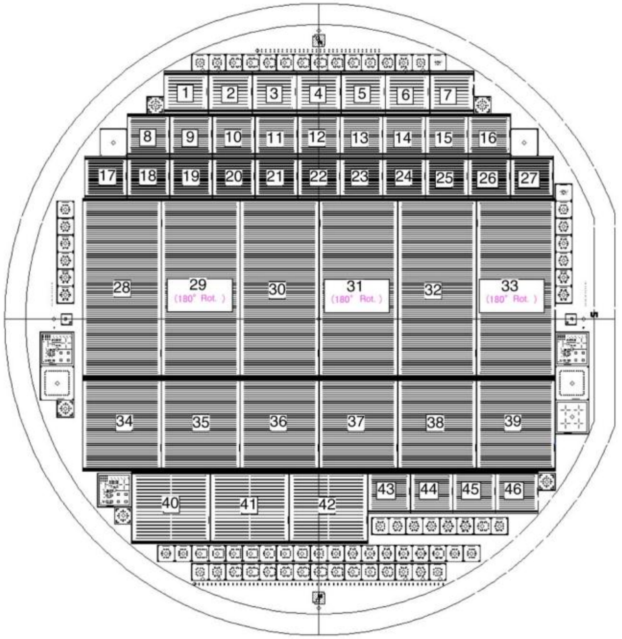
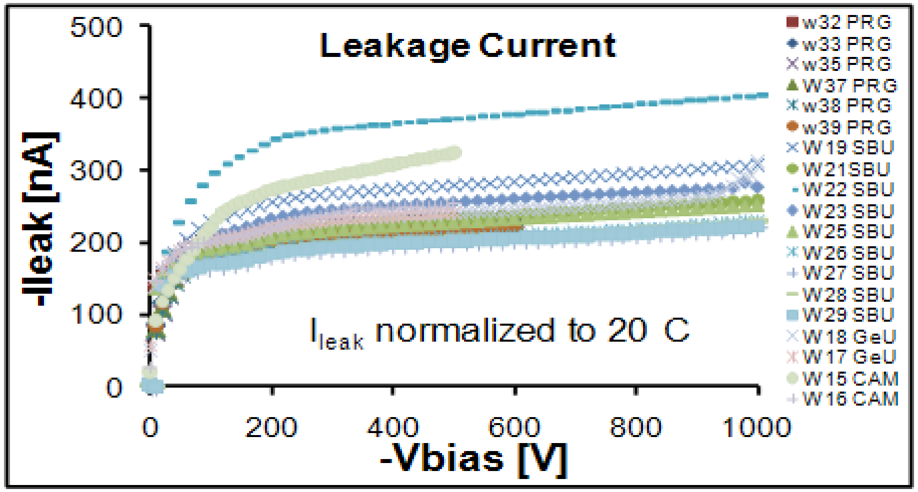
n^+-in-p Silicon Sensors

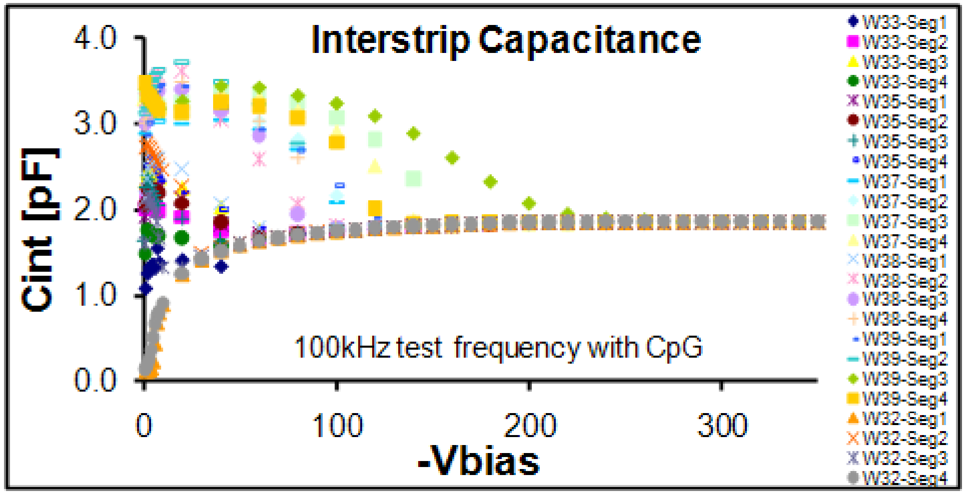
- Collaboration of ATLAS with Hamamatsu Photonics K.K. (HPK)
- Strip sensors
  - 9.75x9.75 cm^2 sensors (6 inch wafers)
  - 4 segments (2 axial, 2 stereo), 1280 strip each, 74.5 mm pitch
  - FZ <100>, 320 µm thick material
  - Miniature sensors (1x1 cm2) for irradiation studies
  - E.g., Y. Unno, et. al., Nucl. Inst. Meth. A636 (2011) S24-S30
- Pixel sensors
  - ATLAS FE-I3 and FE-I4 pixel sensors
  - Biasing: Punch-thru (PT) dot at the four-corner or PolySi resister
  - Isolation: p-stop (common, individual) or p-spray
  - Miniature sensors with test structures
  - E.g., Y. Unno et al., Nucl. Instr. Meth. A650 (2011) 129–135

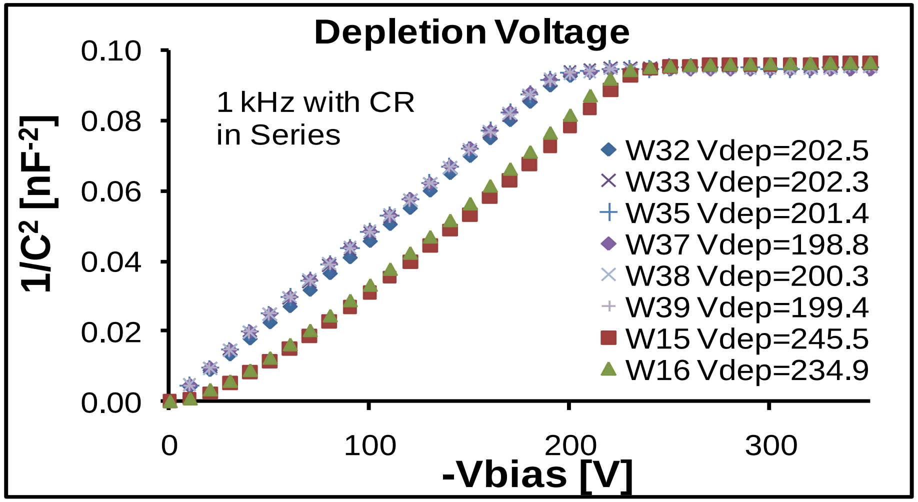




Full-size Sensor Evaluation







	Specification	Measurement
Leakage Current	<200 µA at 600 V	200– 370nA
Full Depletion Voltage	<500 V	190 – 245V
Coupling Capacitance (1kHz)	>20 pF/cm	24 – 30pF
Polysilicon Resistance	1.5+/-0.5MΩ	1.3 -1.6MΩ
Current through dielectric	I_{diel} < 10 nA	< 5nA
Strip Current	No explicit limit	< 2nA
Interstrip Capacitance (100kHz)	<1.1pF/cm (3 probe)	0.7 – 0.8pF
Interstrip Resistance	> 10x R_{bias}~15 MΩ	>19 GΩ

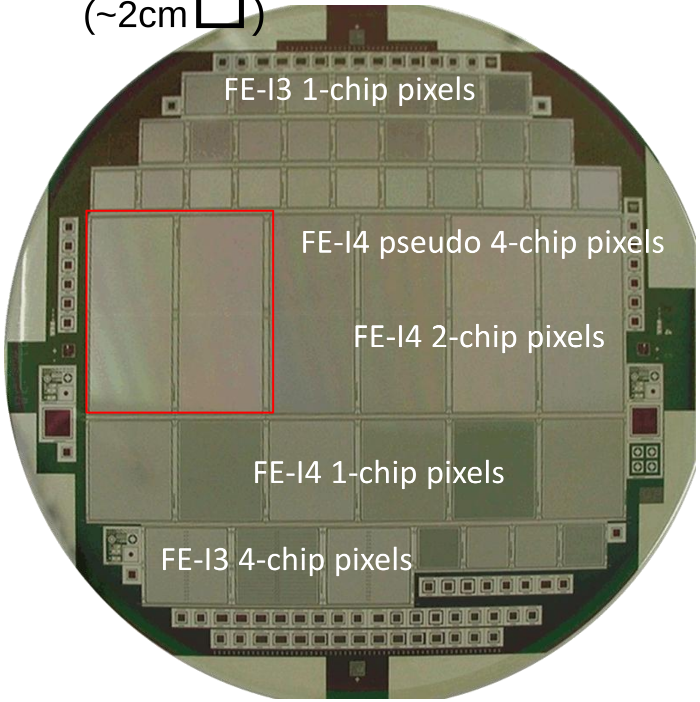
See J. Bohm, et. al., Nucl. Inst. Meth. A, Vol. 636 (2011) S104-S110 for details

- <u>All specifications already met!!</u>

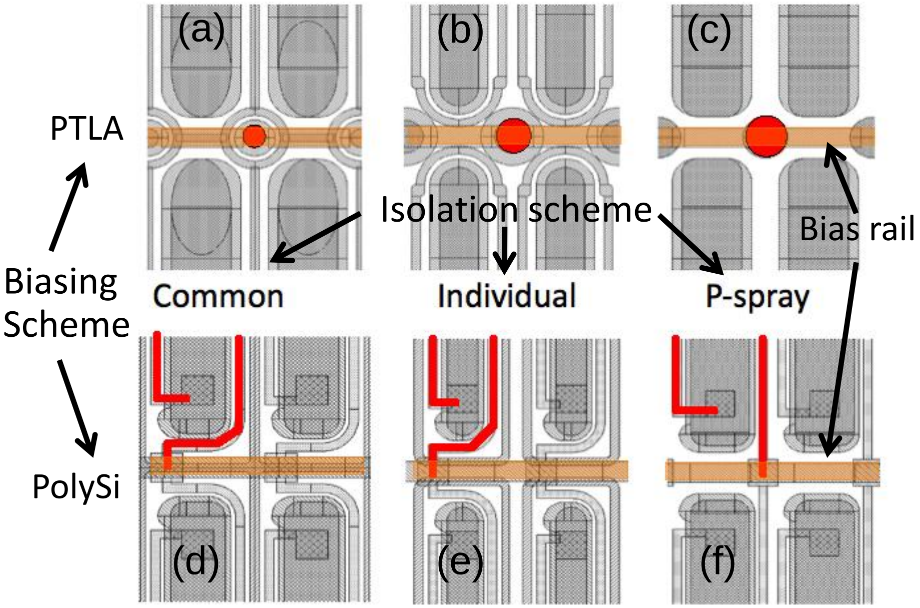
Novel n-in-p HPK Pixel Sensors

- n-in-p 6-in. wafer process in HPK
  - ATLAS FE-I3 and FE-I4 pixel sensors
  - Biasing: Punth-thru (PT) dot at 4-corner or PolySi resister
  - Isolation: p-stop (common, individual) or p-spray
  - “Bias rail” is a metal over insulator, no implant underneath. No electrode in the silicon, other than the bias “dot”

FE-I3 (~1cm□) FE-I4 (~2cm□)



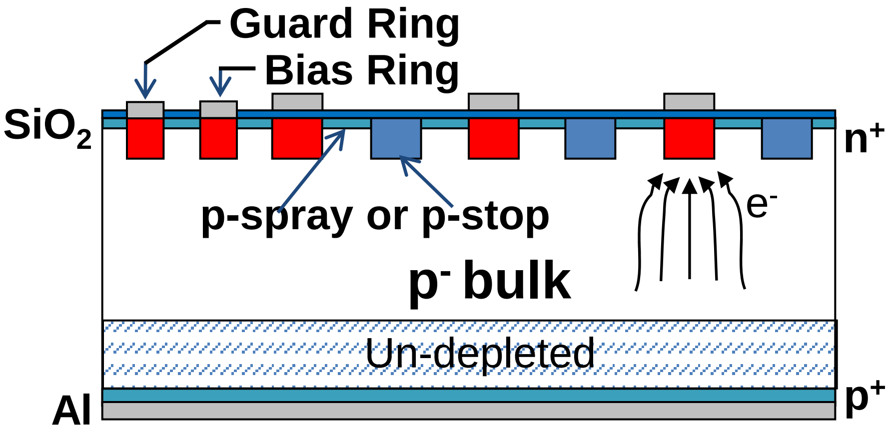
HPK n-in-p 6-in. wafer

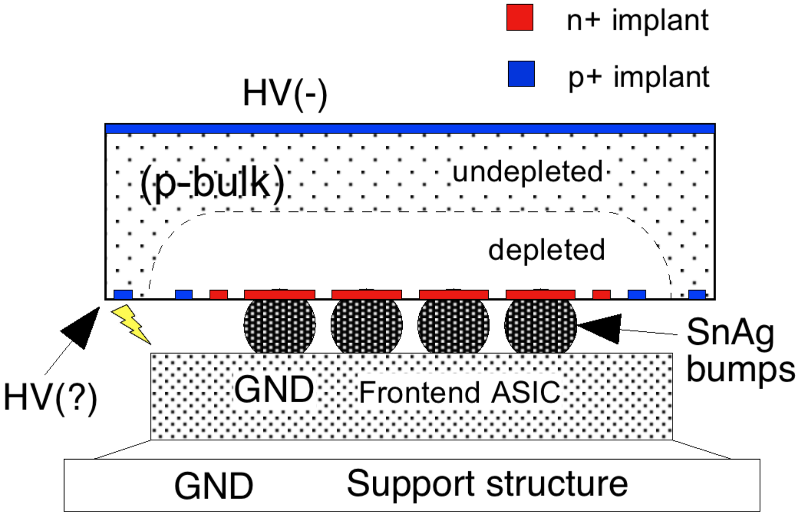


- Thinning
  - Finishing 320 µm wafer process first
  - Thinning the wafers to 150 µm
  - Completing the backside

n^+-in-p Benefits and Issues

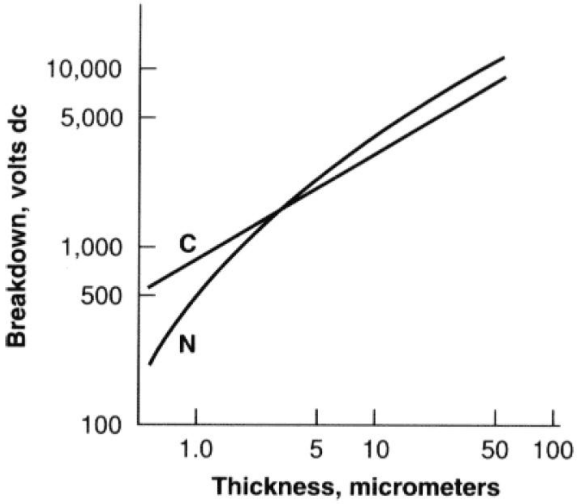
- n^+-readout in p-type substrate (n-in-p)
  - Collects electrons
    - like current n-in-n pixels
    - Faster signal, reduced charge trapping
  - Depletes from the segmented side
    - Good signal even under-depleted
  - Single-sided process
    - 30-40% cheaper than n-in-n
    - More foundries and available capacity world-wide
  - Easier handling/testing
    - due to lack of patterned back-side implant
- Specific structures
  - Bias structure
  - Isolation structure
  - Issues
    - inefficient area
    - HV breakdown = prevention of microdischarge
- HV protection
  - between the front edge and the ASIC

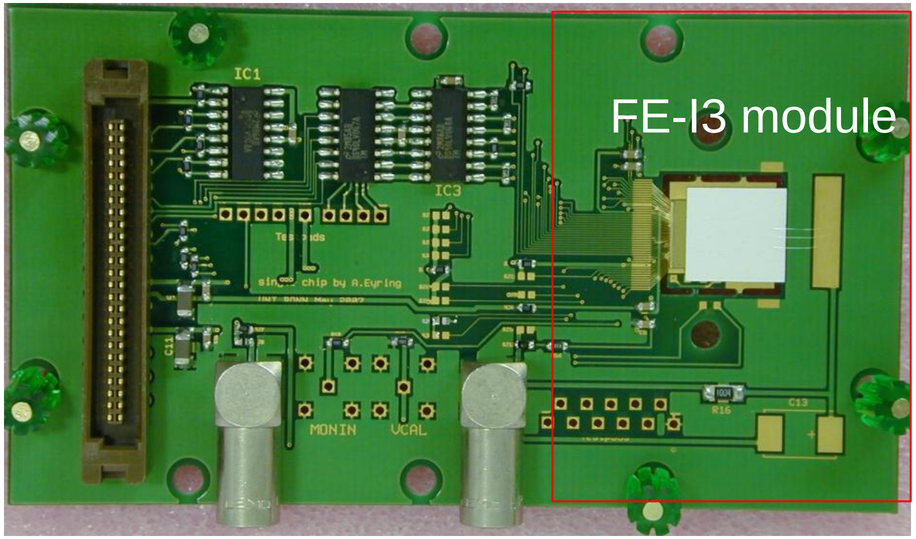




HV protection – Parylene coating

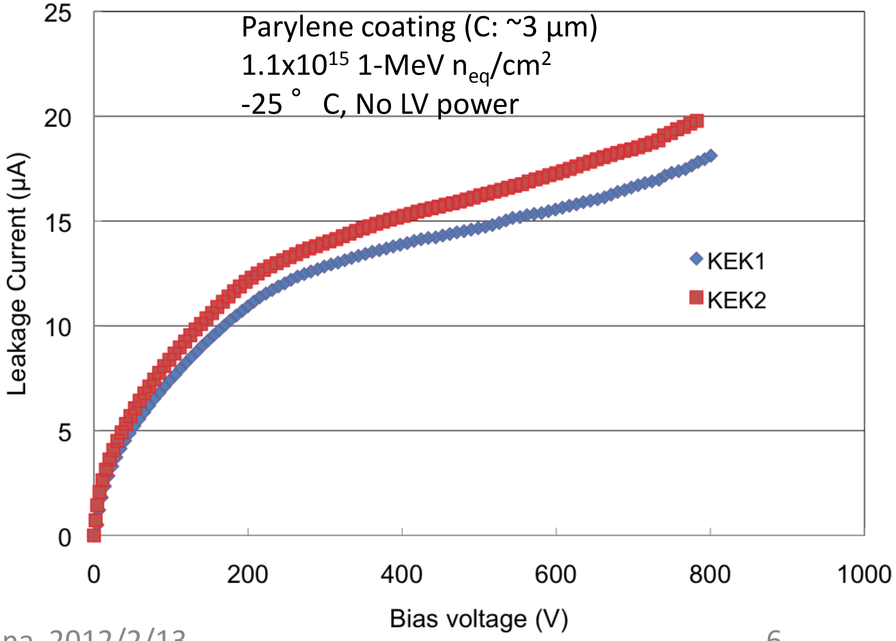
- Parylene coating
  - Two FE-I3 SCMs
    - After wire-bonding
    - Covering all over
    - Parylene C, ~3 µm
      - Softer Parylene-N might be better (?)
  - I-V measurement
    - Shorted ~700 V
    - Consistent with known shorts in the single chip card



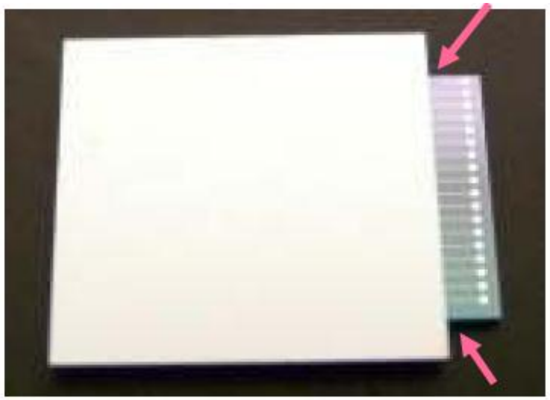


FE-I4 single chip card

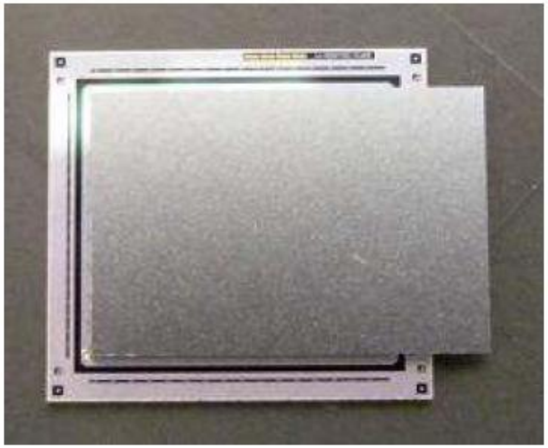
Coated area



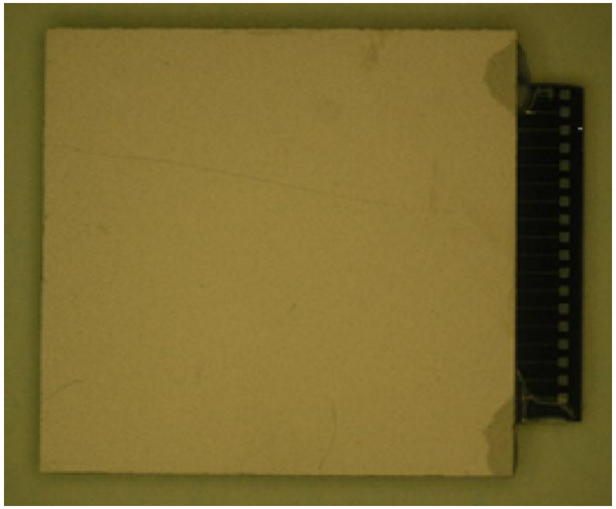
HV protection – Encapsulation



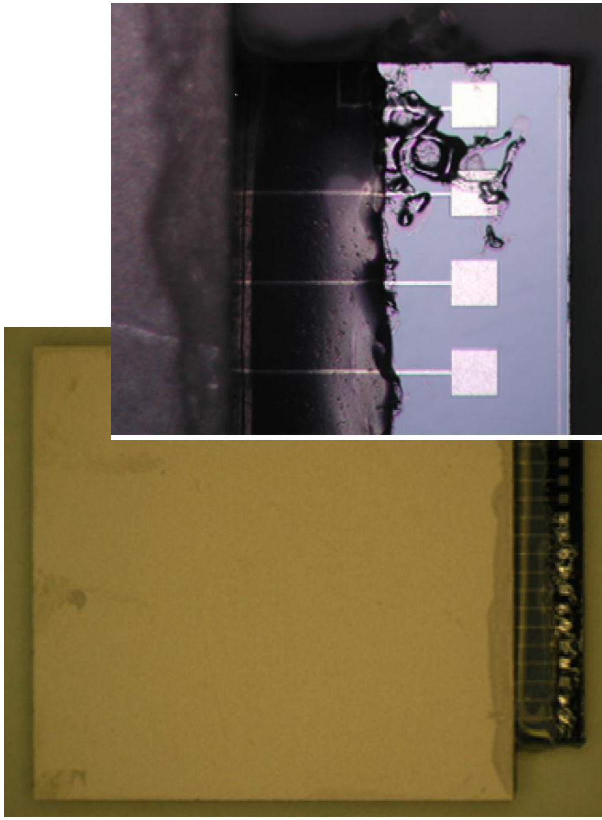
Weak cross points



#1: No encapsulation



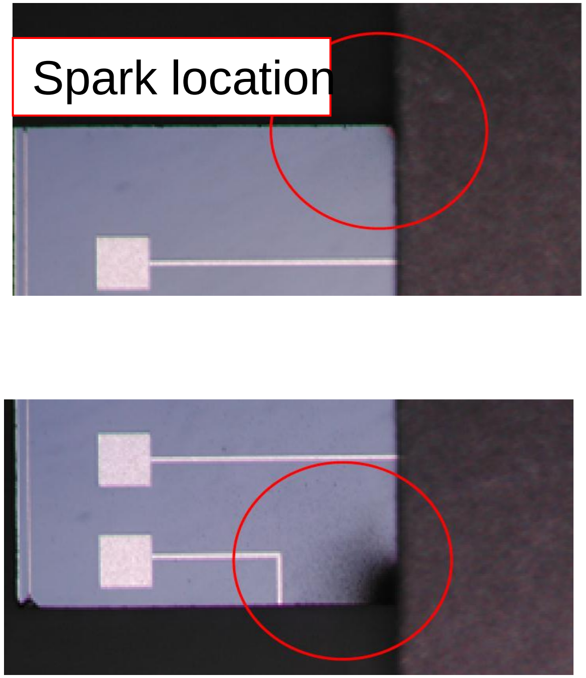
#2: Encapsulation of x-points



#3: Full line encapsulation

- Real pixel sensor (FE-I3) + dummy chip (Al traces)
  - bump-bonded
- Three types of encapsulation
  - Encapsulation material – Silicone adhesive (soft)
  - No encapsulation (#1), X-points (#2), full line (#3)

Encapsulation – Spark test



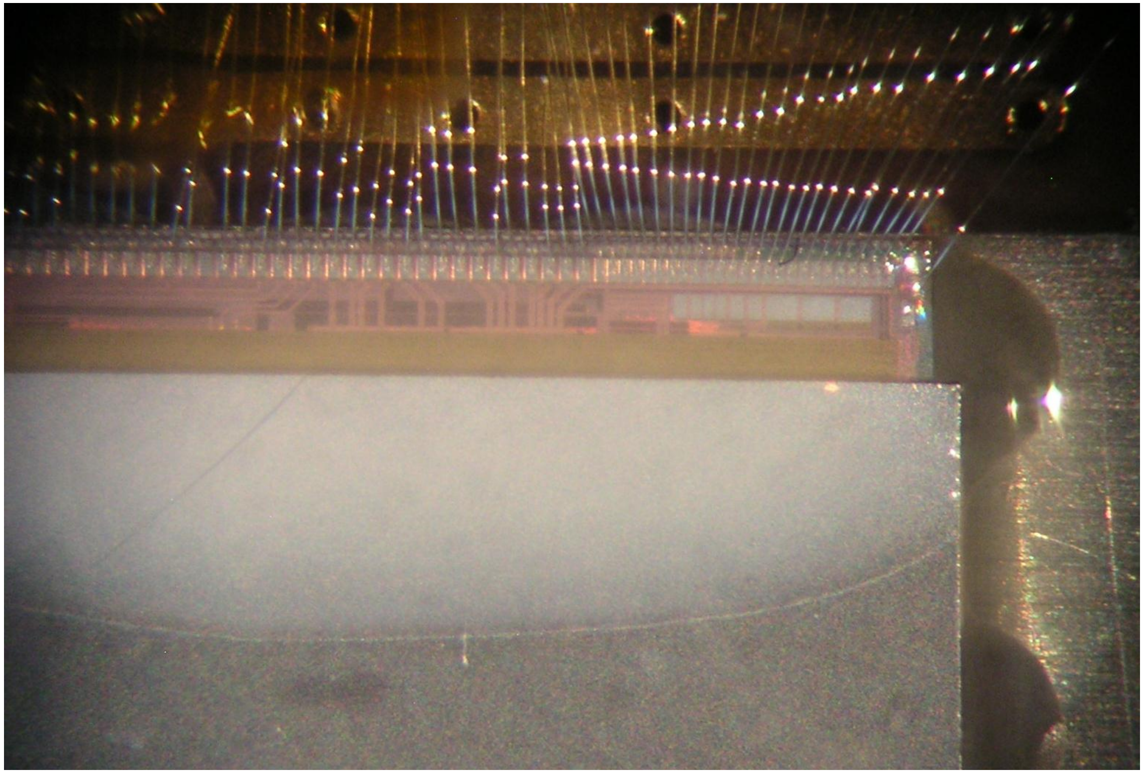
#1: Spark location – X-points ~500 V

#2: Spark location – Al trace ~690 V

#3: No spark up to 1000 V

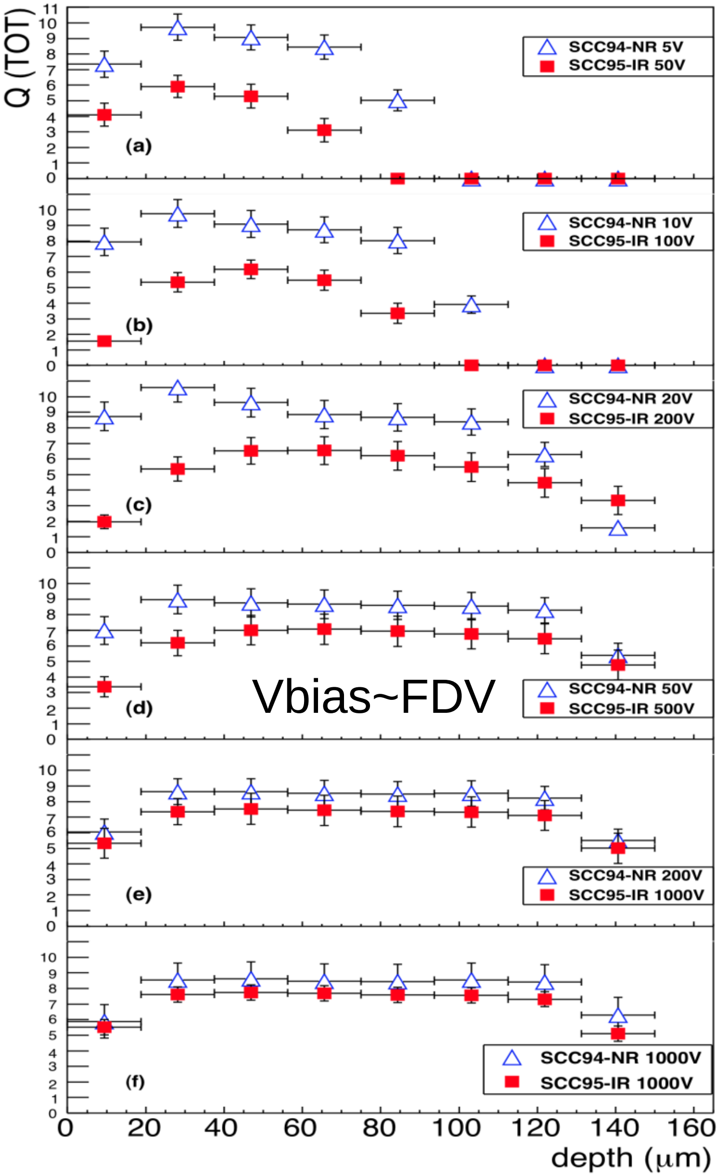
- Spark occurs
  - ~500 V at X-points without protection
    - good info.
  - ~700 V at Al-traces facing to the sensor edge
    - No open/no passivated trace in the real FE-I4 chips (?)
  - No spark up to 1000 V with full encapsulation
- We have at least a candidate to protect the edge.

Encapsulation – FE-I4's testbeam

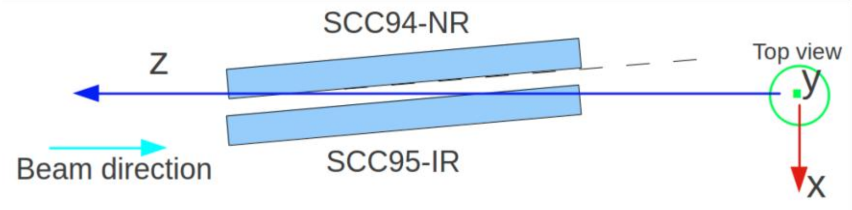


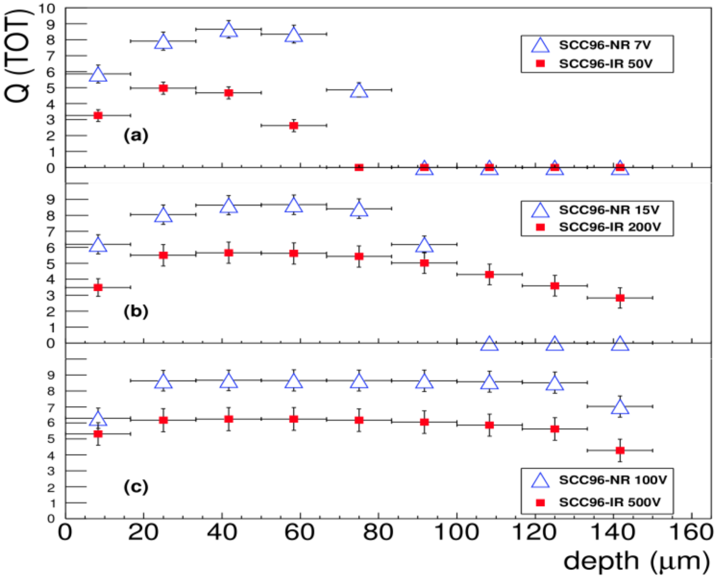
- Post-process application
  - Silicon adhesive
  - Both non-irradiated and irradiated single chip modules (SCM)
  - successfully operated up to 1000 V in the testbeam

Charge Collection in Depth of Sensor



Vbias~FDV





- 150 μm, n-in-p pixel sensors
- Open: non-irradiated (NR)
  - FDV ~45 V
- Solid: $2\text{x}10^{15}$ n_{eq}/cm^2 irradiated (IR)
  - FDV ~ 400 V
- Left: #94-NR, #95-IR, Right: #96-NR and IR

Aftermath of Irradiation

Interstrip Resistance

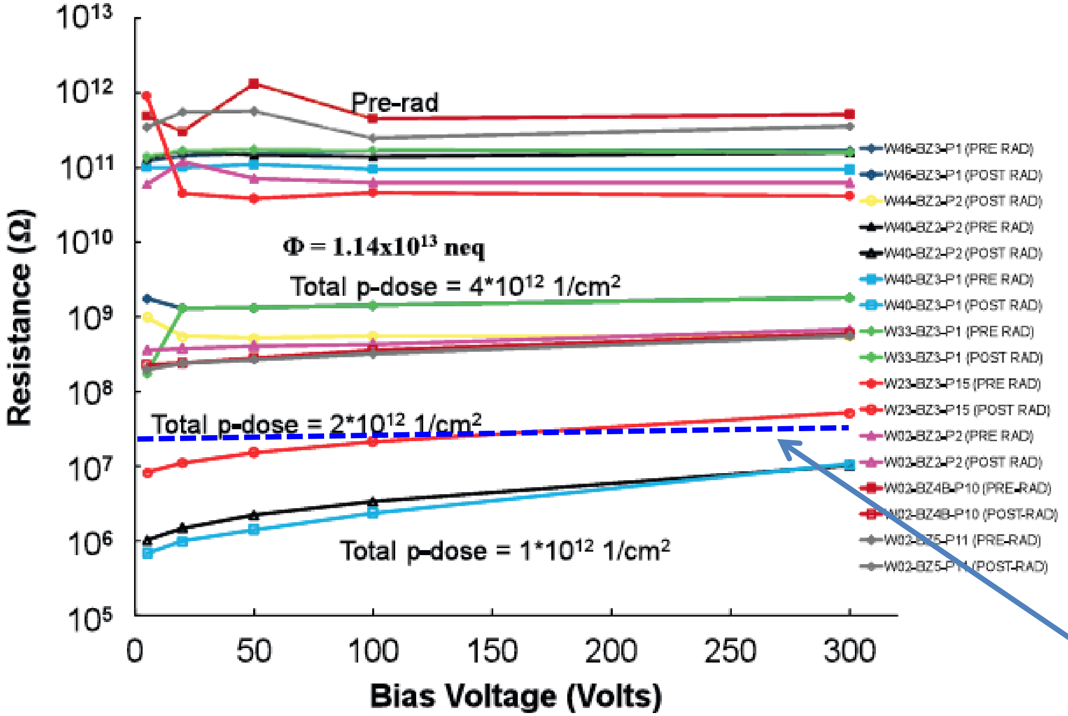
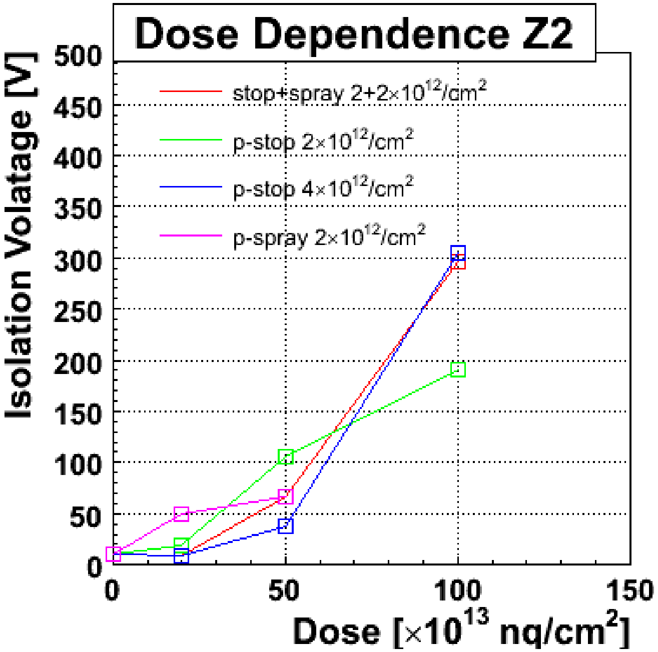


Fig. 6. Interstrip resistance for irradiated series 3 detectors. There is a clear dependence on the total p-dose applied after irradiation.

S. Lingren et al., Nucl. Instr. Meth. A636 (2011) S111–S117

Thesis: M. Yamada

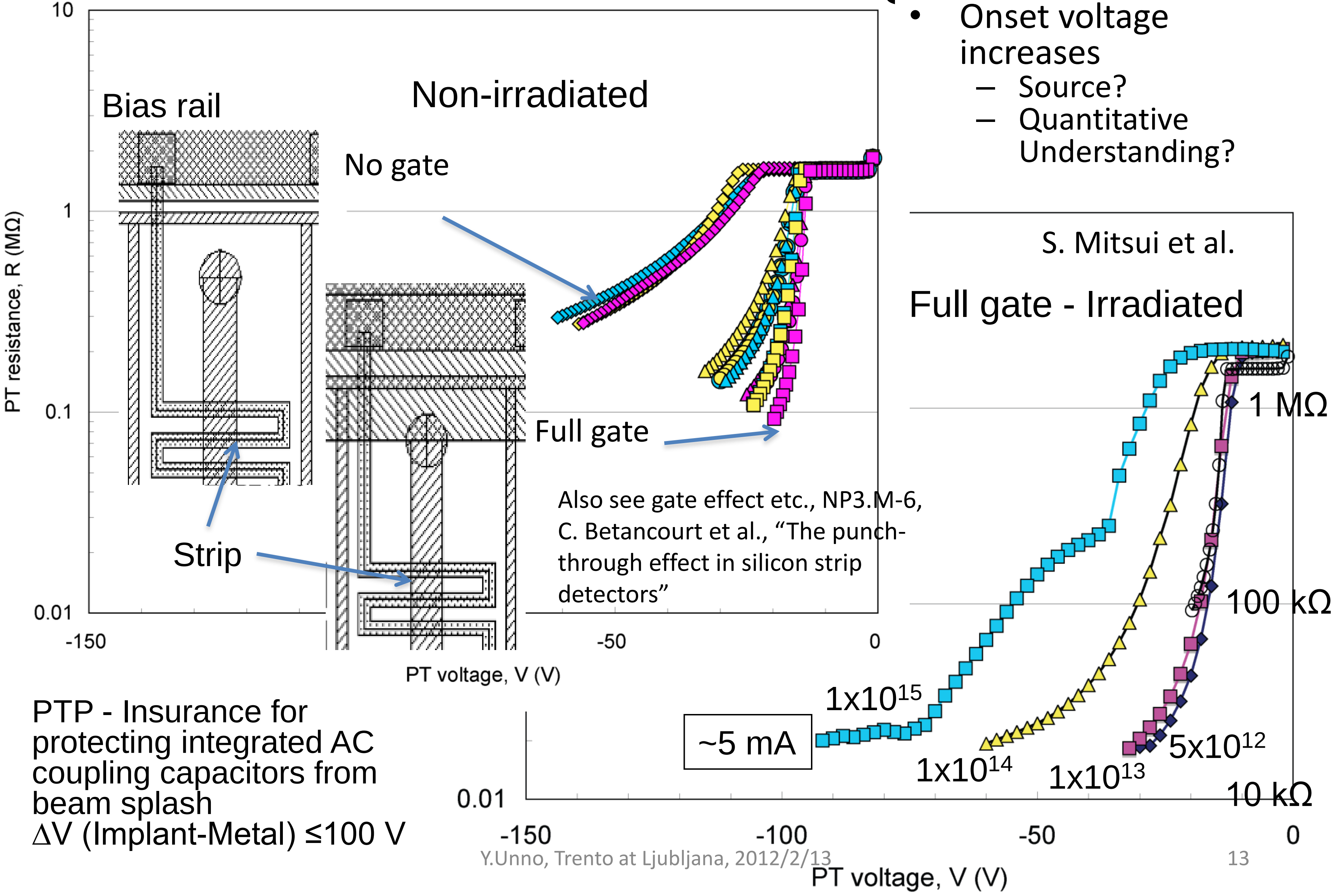


Isolation voltage = Bias voltage to make R_{int}=30 MΩ

- Interstrip resistance decreases with fluence
  - What causes the effect?
  - Do we have a quantitative understanding of the source?

PTP Onset Voltage

- Onset voltage increases
  - Source?
  - Quantitative Understanding?



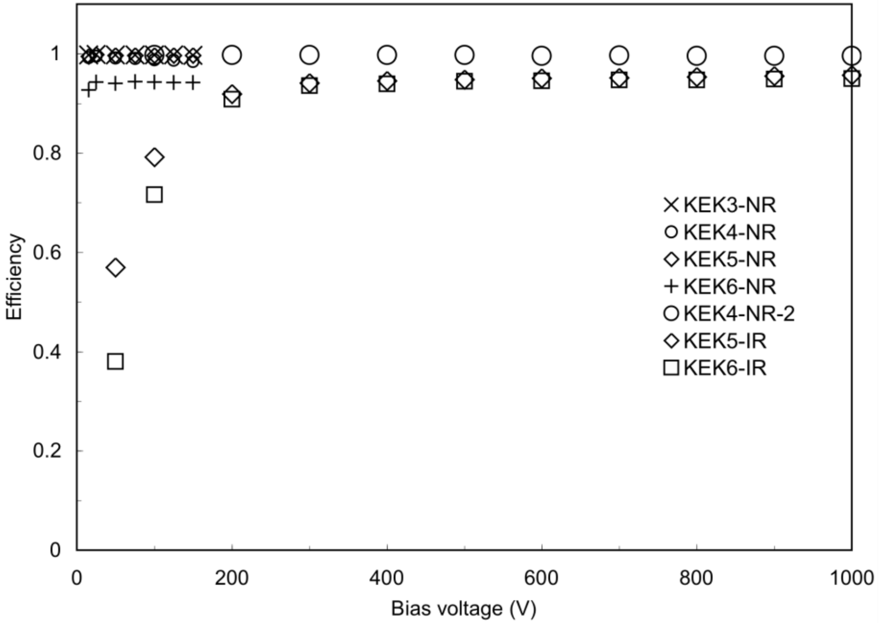
S. Mitsui et al.

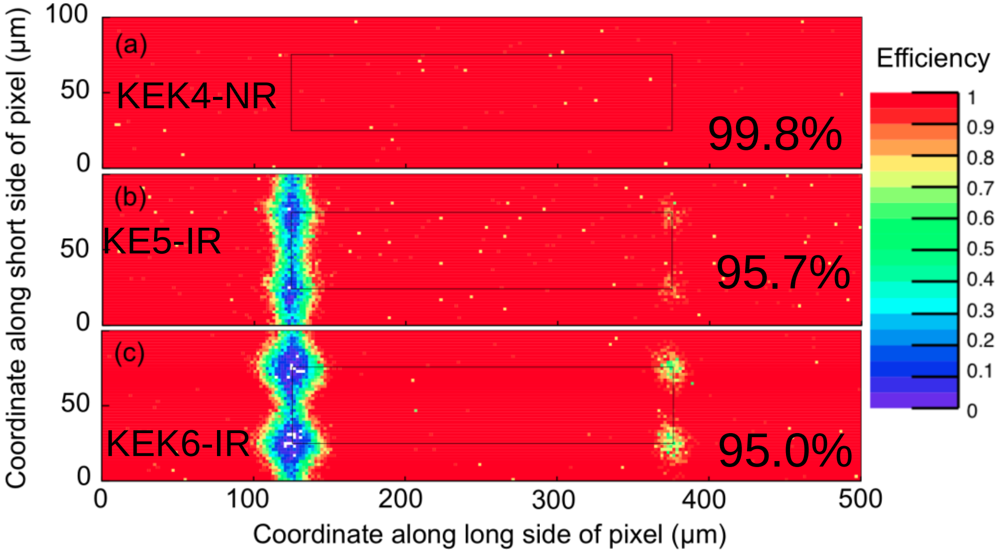
Also see gate effect etc., NP3.M-6, C. Betancourt et al., "The punch-through effect in silicon strip detectors"

PTP - Insurance for protecting integrated AC coupling capacitors from beam splash

ΔV (Implant-Metal) ≤100 V

Bias Rail Effect – Inefficient area





	1st beamtest	2nd beamtest
SCC93	^{a}99.7±0.005% (NR)	N/A
SCC94	^{a}98.7±0.01% (NR)	^{b}99.6±0.01% (NR)
SCC95	^{a}99.7±0.01% (NR)	^{c}95.6±0.02% (IR)
SCC96	^{a}94.2±0.02% (NR)	^{c}94.9±0.02% (IR)

Weighted averages and errors of: ^{a}(100, 125, 150 V), ^{b}(100, 200, 300 V), ^{c}(800, 900, 1000 V)

- Thin (150 µm) FE-I4 pixel sensors
- Irradiation (2x10^{15} n_{eq}/cm^{2})
- Successful operation up to 1000 V
- Issue
  - Reduction of efficiency specially underneath the bias rail

Insensitive Area after Irradiation

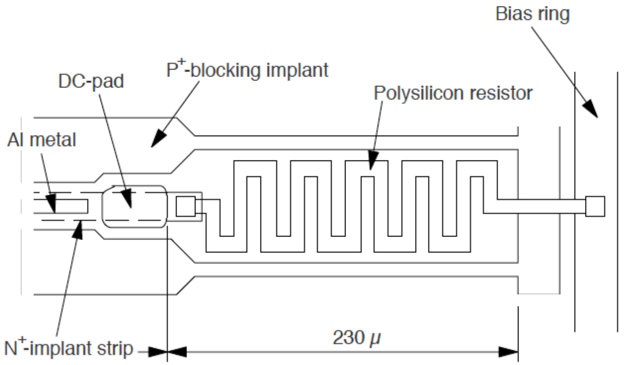


Fig. 9 Structure around the polysilicon bias resistor of the n-side. The n$^+$-implant strip ends at the DC-pad; no n$^+$-implant strip was designed under the bias resistor in this detector.

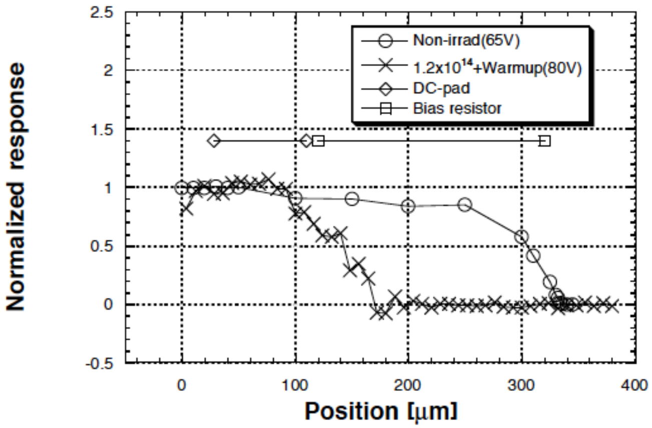
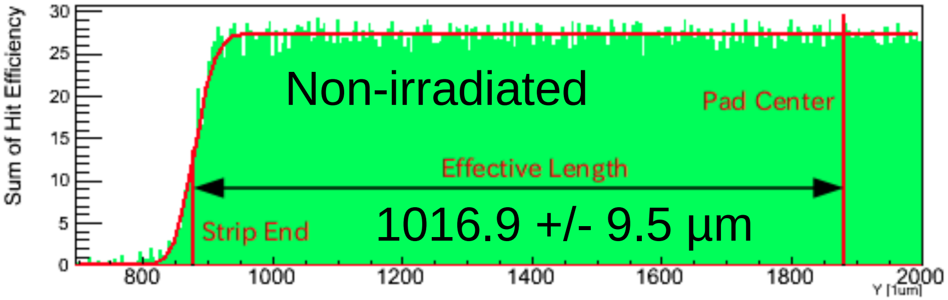


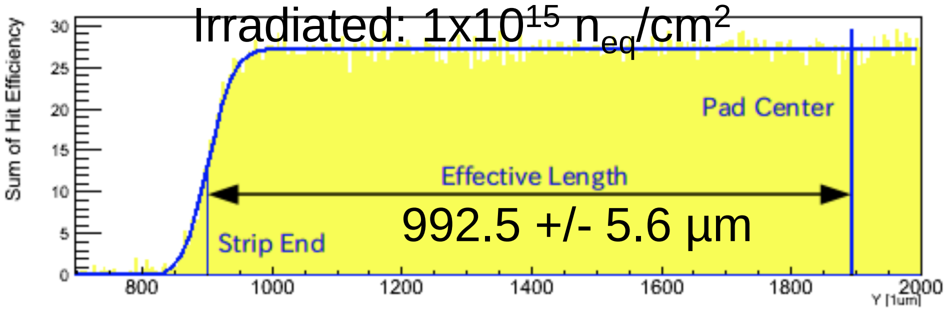
Fig. 10 The charge collection under the bias resistor where no n$^+$-implant strip was fabricated has been measured by using a laser light (1064 nm). The laser response was obtained for non-irradiated (circle) and the irradiated (cross) detectors. The areas of the bias resistance (square) and the DC-pad (diamond) are shown together.

Y. Unno et al., IEEE TNS 44 (1997) 736-742



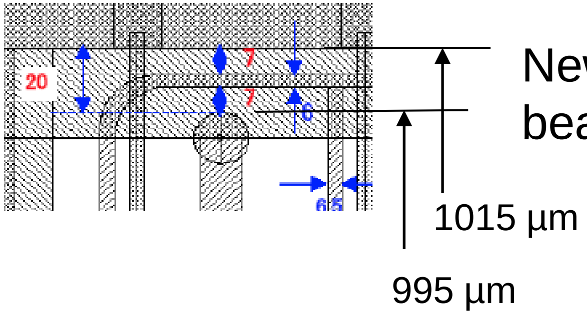
Non-irradiated

1016.9 +/- 9.5 µm



Irradiated: 1×10^{15} n_{eq}/cm^2

992.5 +/- 5.6 µm



New result from a beamtest (Kishida et al.)

- Underneath the gate (metal) seems insensitive after irradiation
  - 20 µm width

Sensor Edge – Field Width

S. Mitsui

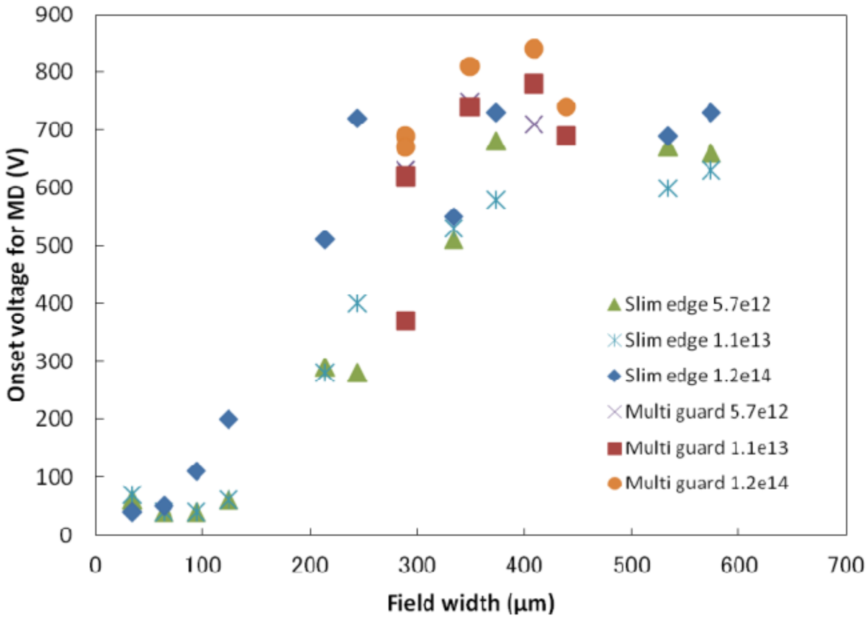


Figure 4: Field width dependence of the onset voltage for MD.

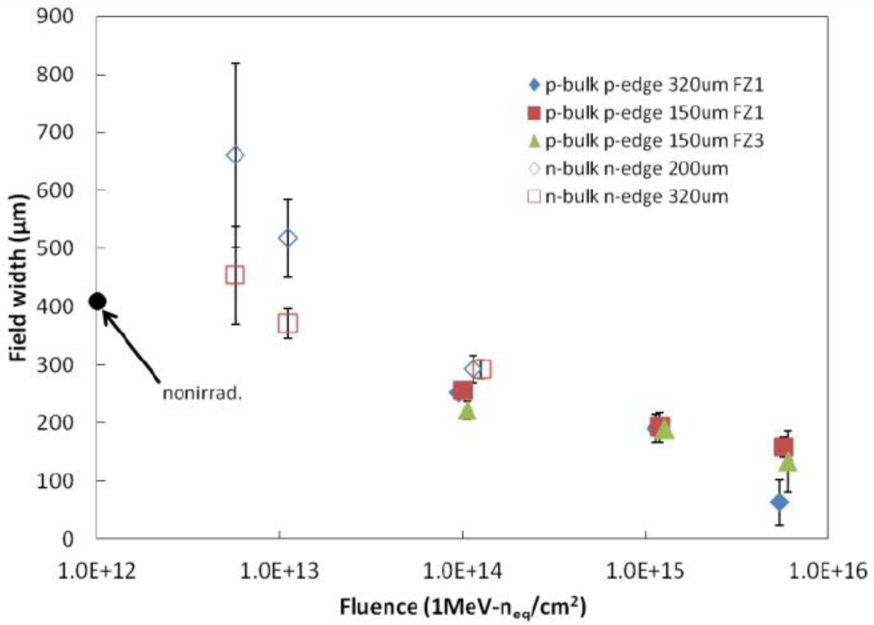
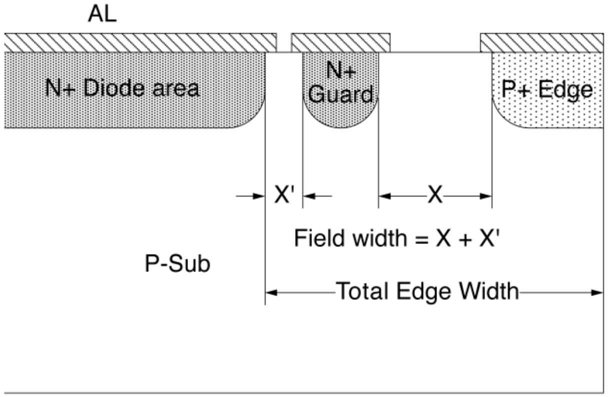
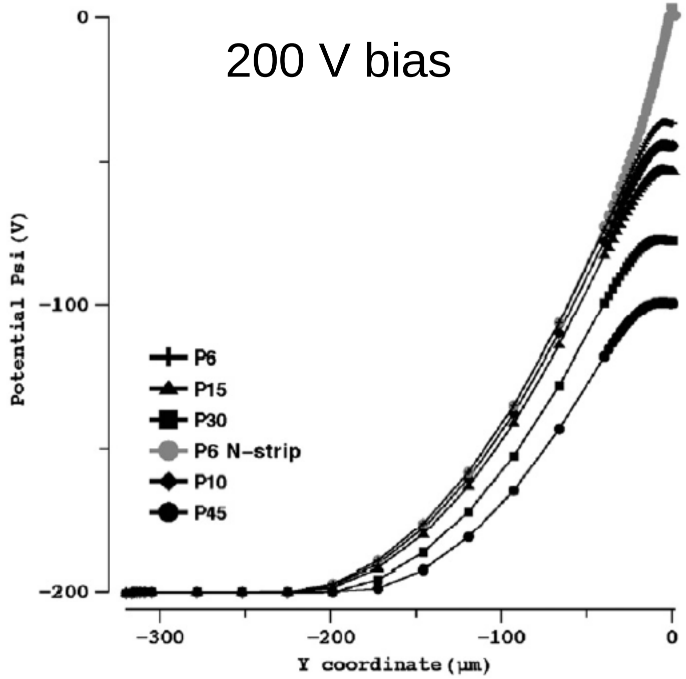


Figure 5: Fluence dependence of field width hold up to 1000 V.



- Field width
  - Area with no implantation
- Top-left fig.
  - Need for a width to hold a bias voltage
- Top-right fig.
  - Required field width decreases as fluence is accumulated
  - How does this correlate with the surface resistivity?

P-stop Potential - TCAD



200 V bias

Fig. 7. Electric potential Psi charted vertically through silicon in common p-stop structures with p-stop widths of 6–45 µm at the centre between the n$^+$-strips (P6–P45), and at the n$^+$-strip (P6 N-strip).

75 µm ptich

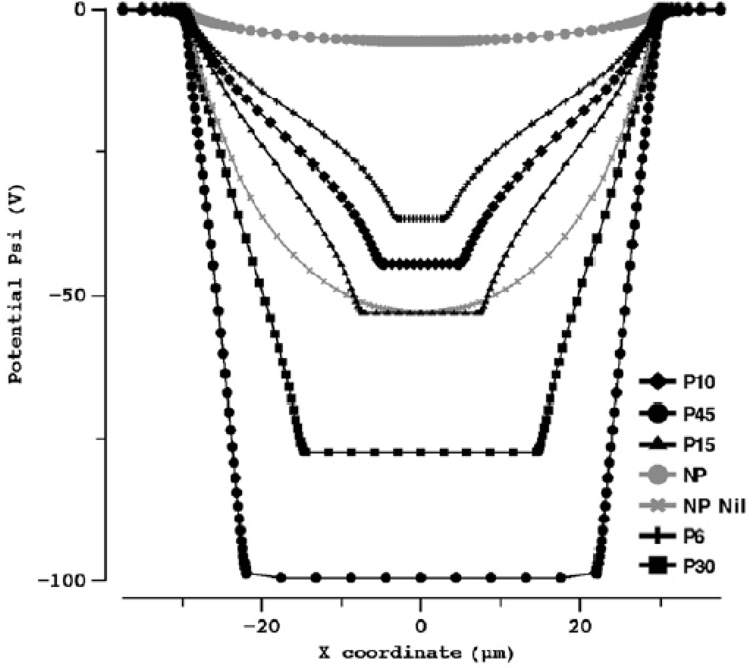
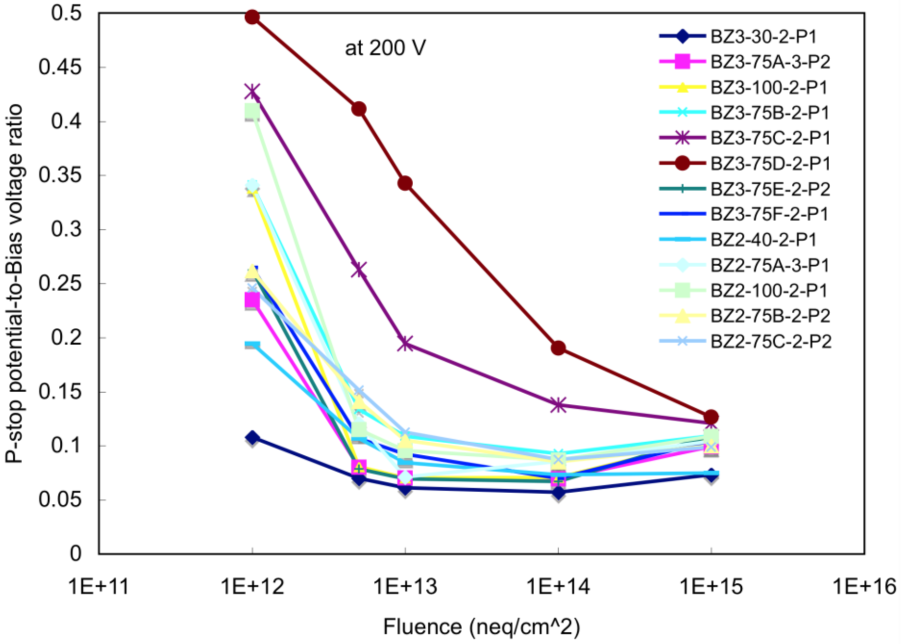


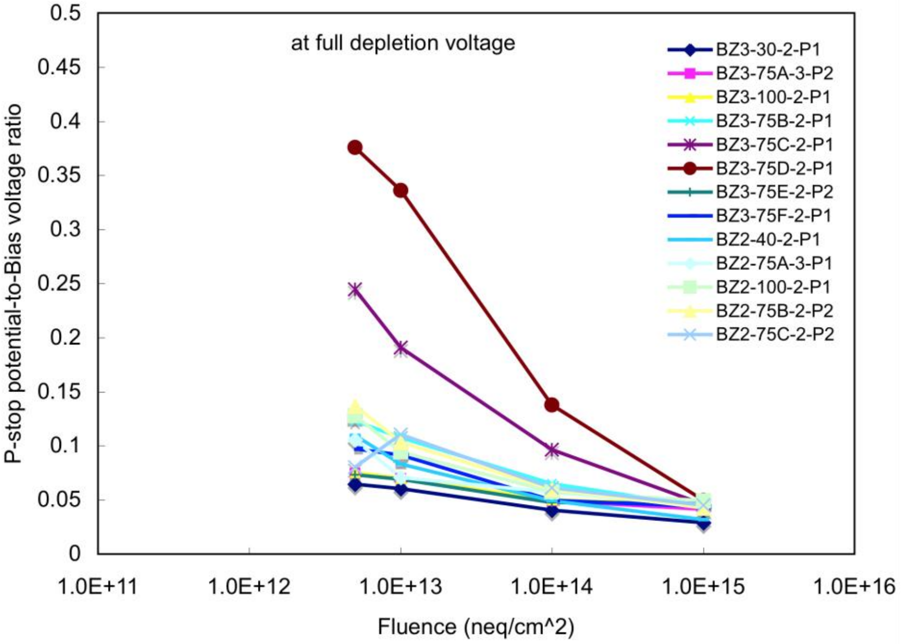
Fig. 6. Electric potential Psi near the silicon surface between n$^+$-strips in common p-stop structures with p-stop widths of 6–45 µm (P6–P45), together with references without p-stop and with interface trap charges of 1×10^{11} cm^{-2} (NP) and nil (NP Nil).

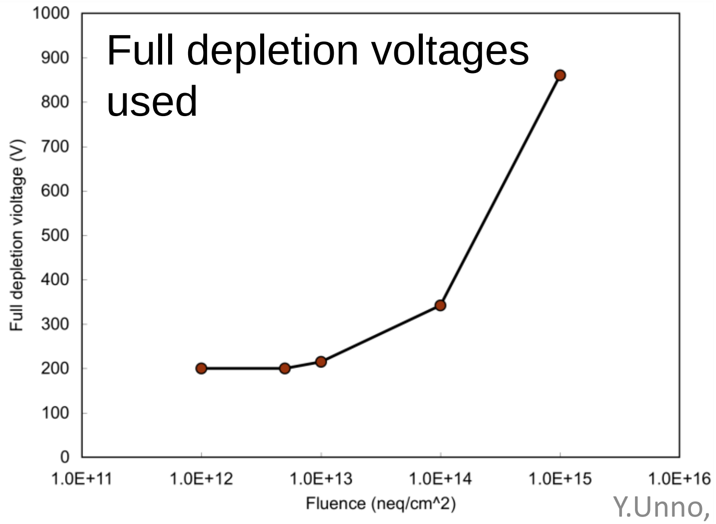
- Silicon wafer
  - 320 µm, 3 kΩ cm (=4.7x10^{12} cm^{-3})
- Condition: Non-irradiated
- Ratio of p-stop potential-to-bias voltage seems stable for the change of the bulk resistivity
- Y. Unno et al., Nucl. Instr. Meth. A636 (2011) S118–S124

P-stop Potential

S. Mitsui







- 75A, B, C, D, E, F
  - 75 µm pitch
  - P-stop width: 6, 15, 30, 45, 6 (Asym), 6 (Asym) µm
  - Asym: asymmetric location of p-stop
- Reduction of p-stop potential as a function of fluence
  - Interface charge explains this?
  - What else is the source of the change?

Discussion

- After irradiation,
  - Decrease of the interstrip resistance
  - Decrease of efficiency underneath the bias rail
  - Decrease of the sensitive area underneath the ground potential
  - Decrease of the p-stop potential between the n^+ strips
  - Decrease of the field width to hold 1000 V
  - Increase of the onset voltage in the PTP structure
- What is the common source that may have caused the above observations?
  - Change of the surface resistivity by radiation damage?
  - Trapping of the electron carriers in the surface?
  - Are these effects already identified in our and/or in the semiconductor community (i.e., TCAD program)?
    - If not, how can they be implemented?

Summary

- Nobel n^+-in-p silicon strip and pixel sensors have been fabricated at HPK successfully.
- Issues specifically associated with the n^+-in-p sensors were addressed.
  - Isolation structures that are robust against the bias voltage up to 1000 V.
    - Issue: Inefficient area underneath the bias rail
  - HV protection at the edges
    - Low tech. solutions (Parylene coating, Encapsulation), but works
      - Issue: Radiation hardness up to a few x 10^{16} n_{eq}/cm^2
- Performance before and after irradiation has been accumulated.
  - We have had a number of evidence that require a fundamental explanation.
    - The explanation must be simple if understood (my guess).
  - If you have already had the explanation, let's have a dinner together.
  - We hope to have a quantitative explanation by the next workshop.