Development of *n*-in-*p* planar pixel sensors with active edge for the ATLAS High-Luminosity Upgrade

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Project leader

- Simulations
- Test

FBK
(Trento)

- Design
- Process

Outline

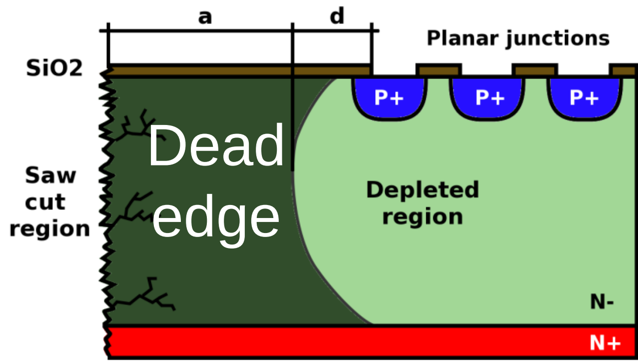
- What is this sensor for?
- Trench Tech @ FBK
- Layout
- Simulations
- Test Plans

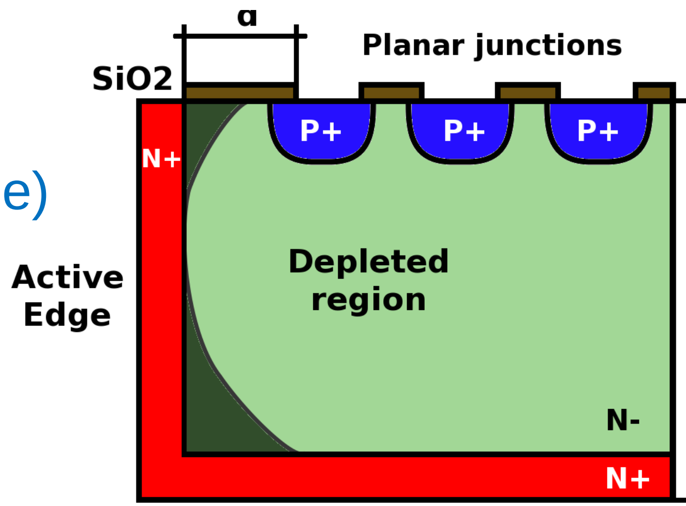
ATLAS Pixel Sensor

R&D for ATLAS upgrade

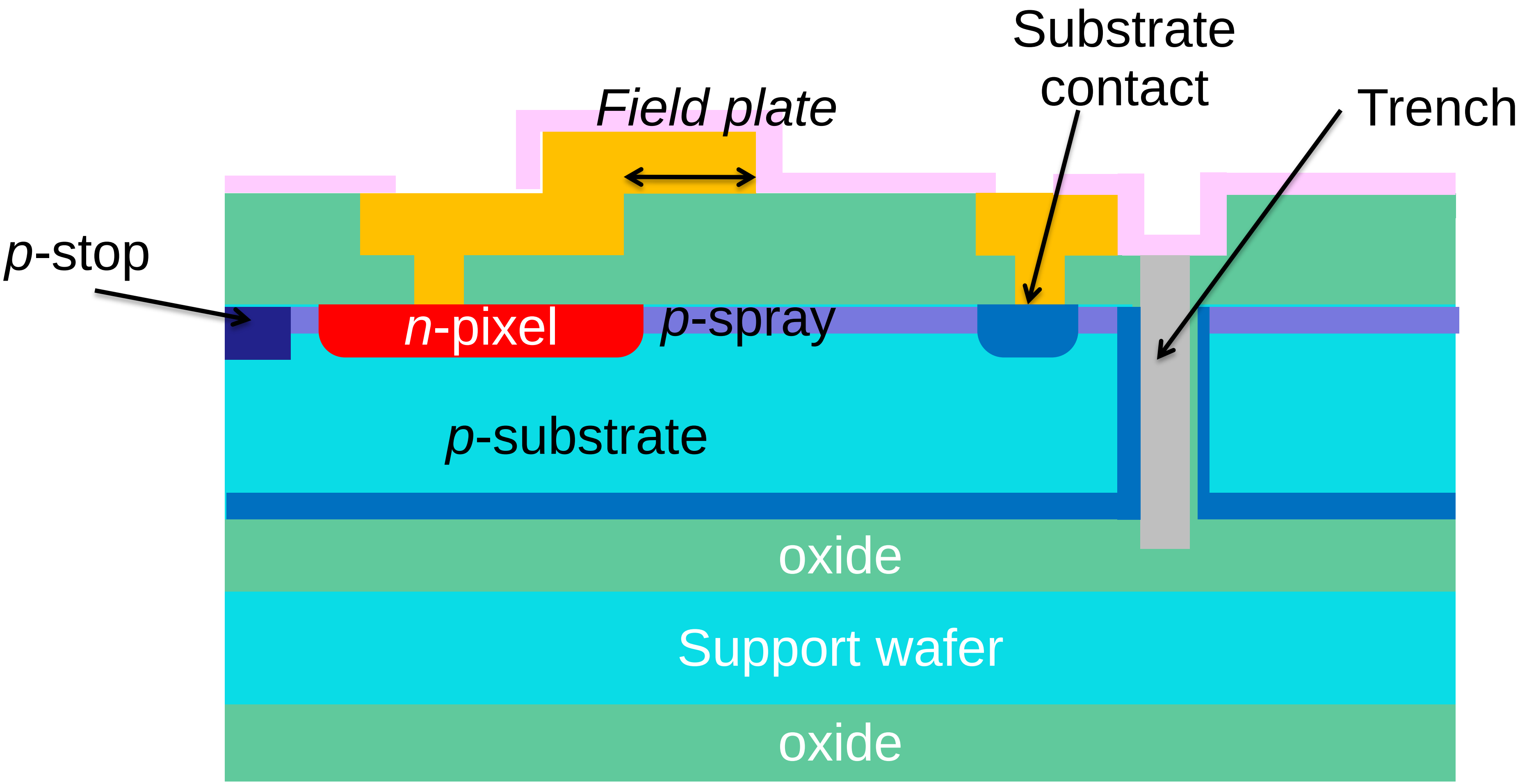
- a) Rad-hard for ~ 1e16 n_{eq}/cm^2 (high luminosity LHC)
- b) Highly segmented to cope with high-event rate
  - → pixel sensor
- c) Minimize dead area (no *z*-overlap)
  - → Active Edge
- d) Low material budget
  - → Thin substrates (200 μm)
- e) Signal mainly due to electrons
  - → *n*-on-*p* technology
  - (*n*-on-*n* is double-side, not compatible with Active Edge)

→ Active edge pixel sensor can be a choice





Active Edge Sensor Structure



n-on-*p* needs pixel insulation

We will use both *p*-spray and *p*-stop.
Process splittings concern the dose of such implants: e.g.

Splitting #	*p*-spray dose (cm^{-2})	*p*-stop dose (cm^{-2})
1	0	3e12
2	1e12	5e12
3	3e12	3e12
4	2e12	5e12

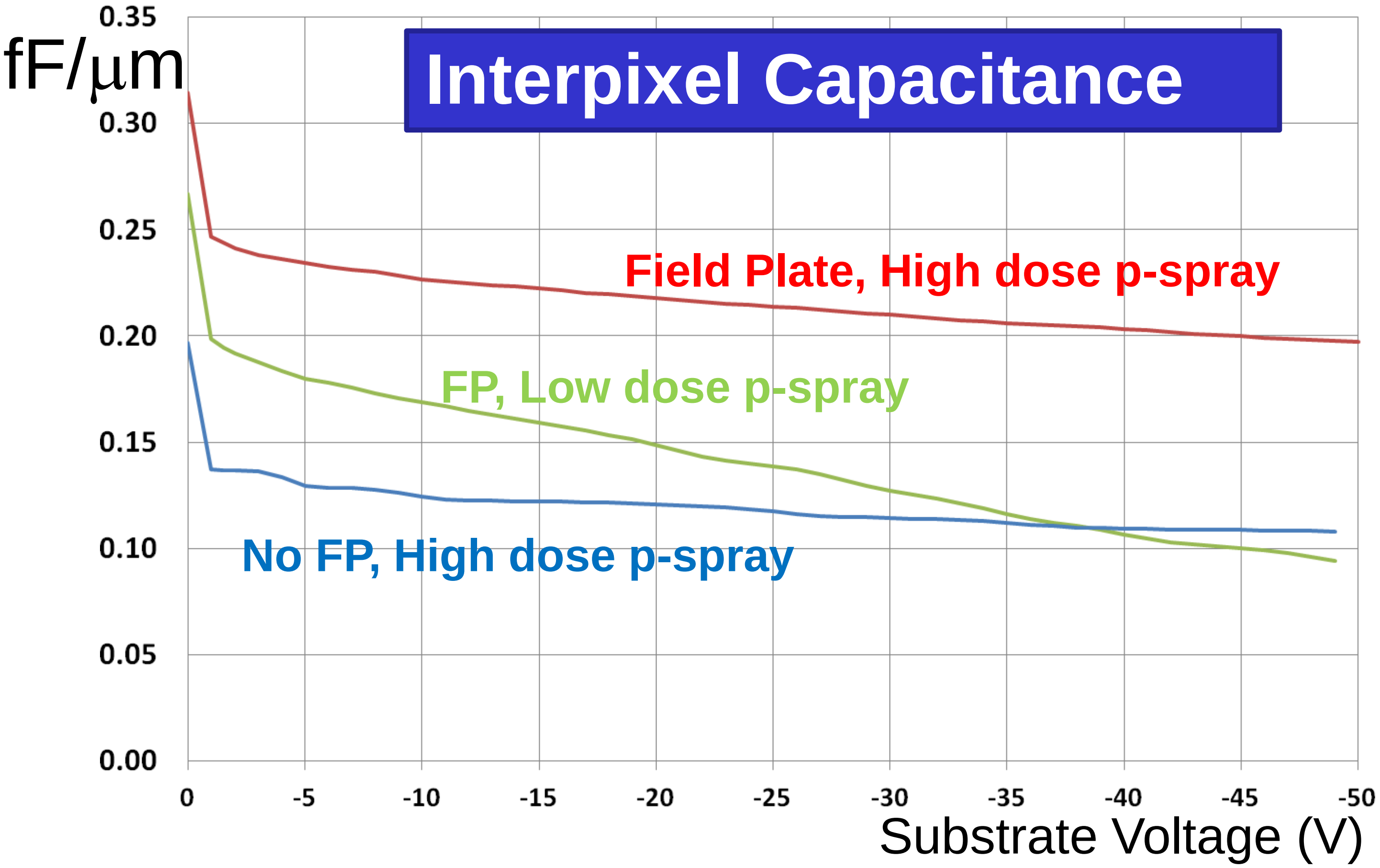
- FBK has experience on planar *n*-on-*p*
- the edgeless technology is different due to the presence of high temperature steps required for trench doping

InterPixel Capacitance vs *p*-spray dose

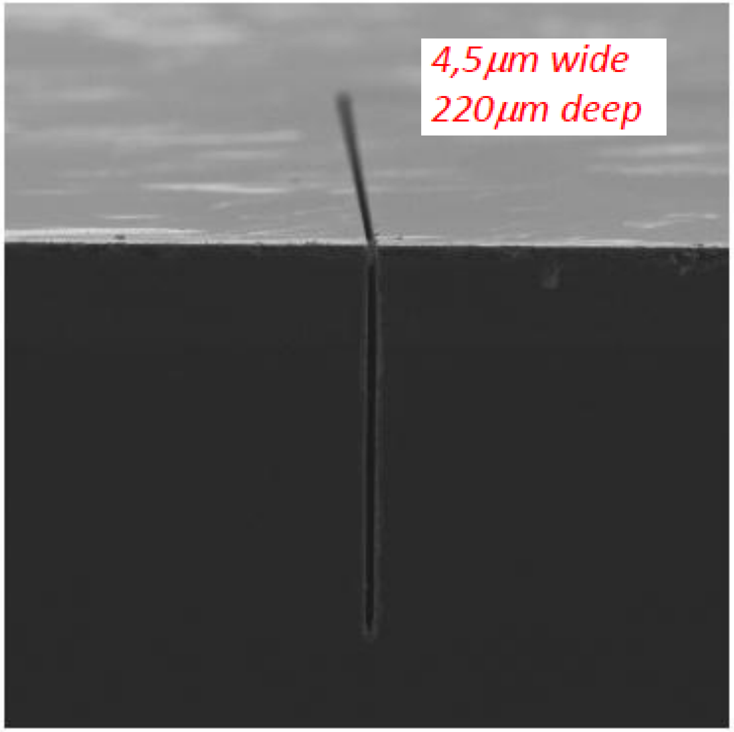
1. Pixel capacitance should be minimized.
2. We want Field Plate (FP) for higher BD Voltage

p-spray must deplete under the FP or there'll be a large interpixel capacitance

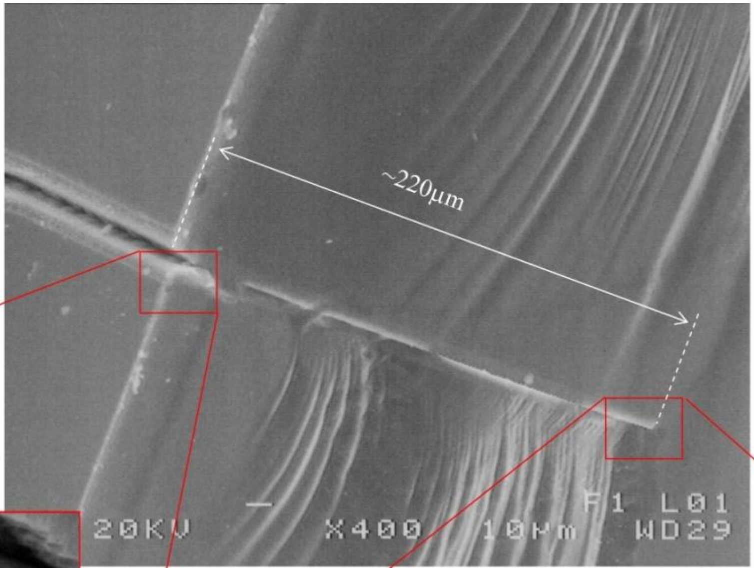
→ Low *p*-spray dose

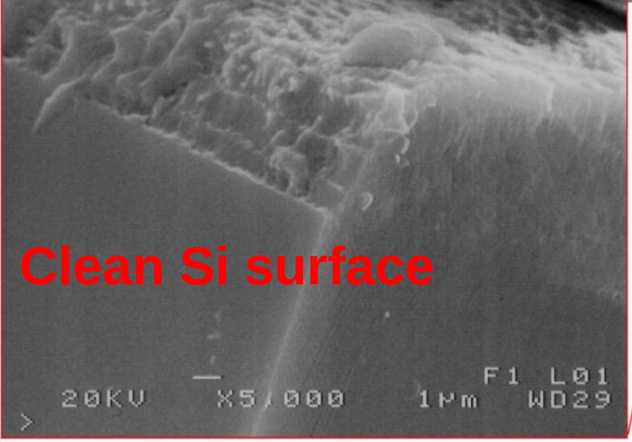


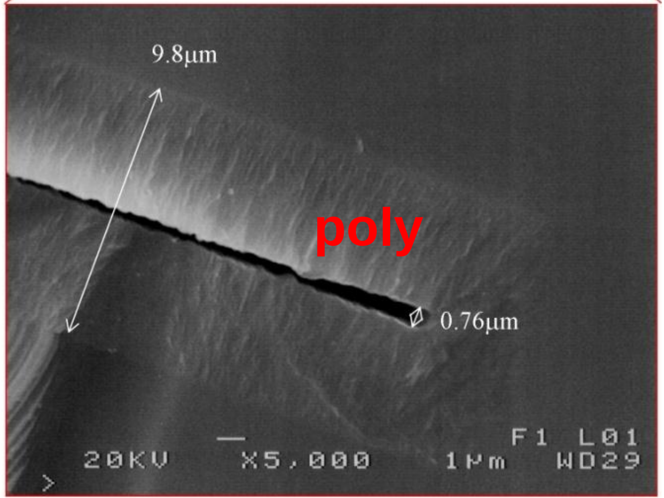
Trench experience @ FBK (1)



- 10µm wide
- 220µm deep
- polysilicon filled



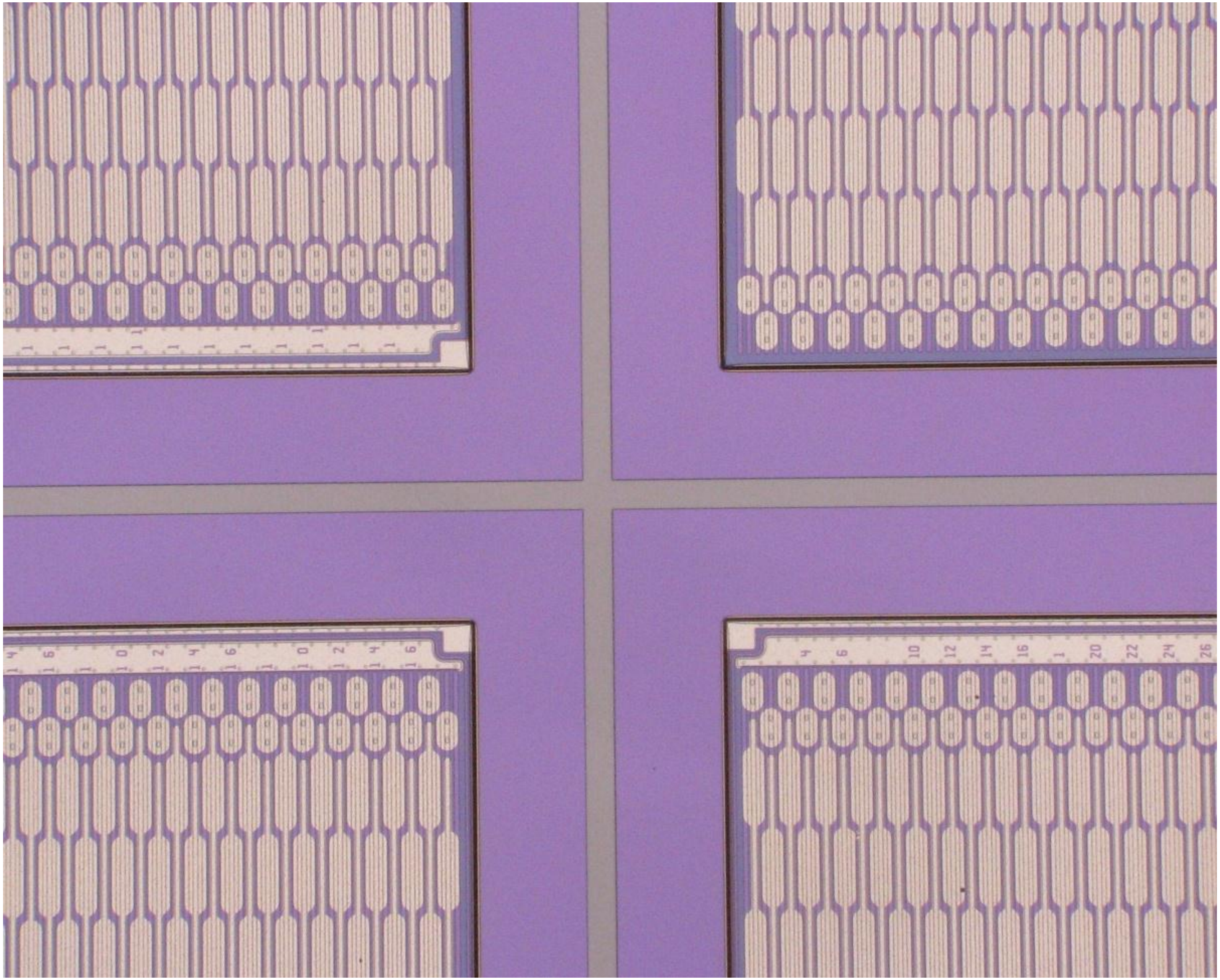




A.Bagolini, “Development of planar active-edge technology at FBK”, 6th Trento workshop 2011

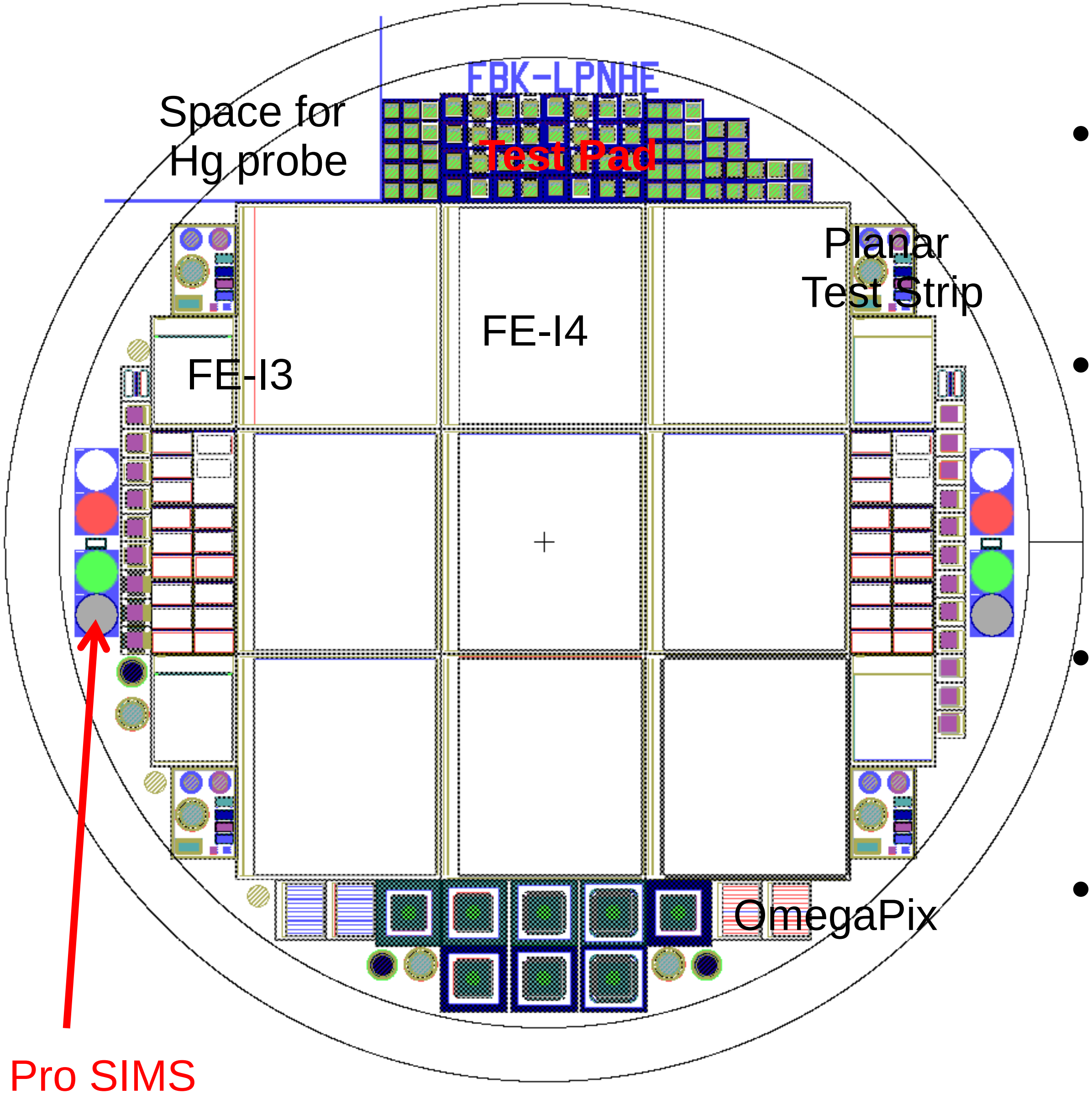
Trench experience @ FBK (2)

Planar strip sensor (p-on-n)



Povoli et al., "Development of planar detectors with active edge" NIM A658 (2011) p. 103

Wafer Layout

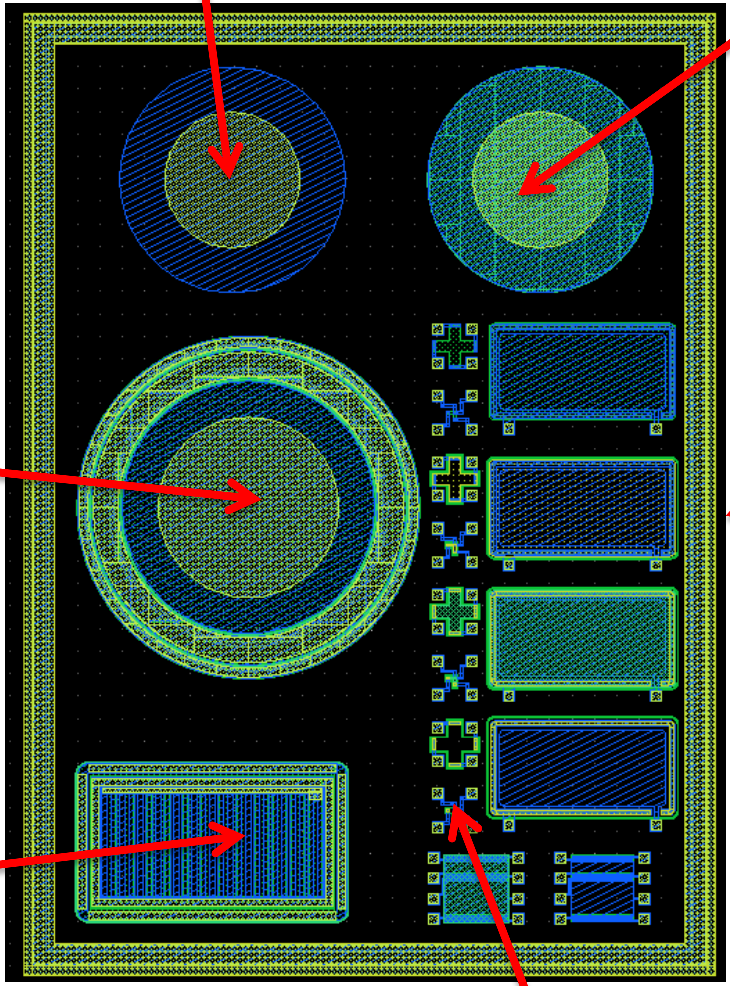


Pro SIMS
n+, p+, *p*-spray, *p*-stop

- 9 FE-I4
  - 0, 1, 2, 3, 5, 10 GRs
  - Different n^+→trench distances
- 4 FE-I3
  - 1 or 2 GRs
  - 2/4 are PT biased
- DC Strip Sensors
  - 0, 1, 2 GRs
  - Different n^+→ trench distances
- OmegaPix
  - 1 or 2 GRs
  - 2/4 are PT biased
- TestPixels/Pad
  - 0, 1, 2, 3, 5, 10 GRs
  - Different n^+→trench distances

Planar Test Structures

2 MOS (one over *p*-spray and one over *p*-spray + *p*-stop)



1-D Diode

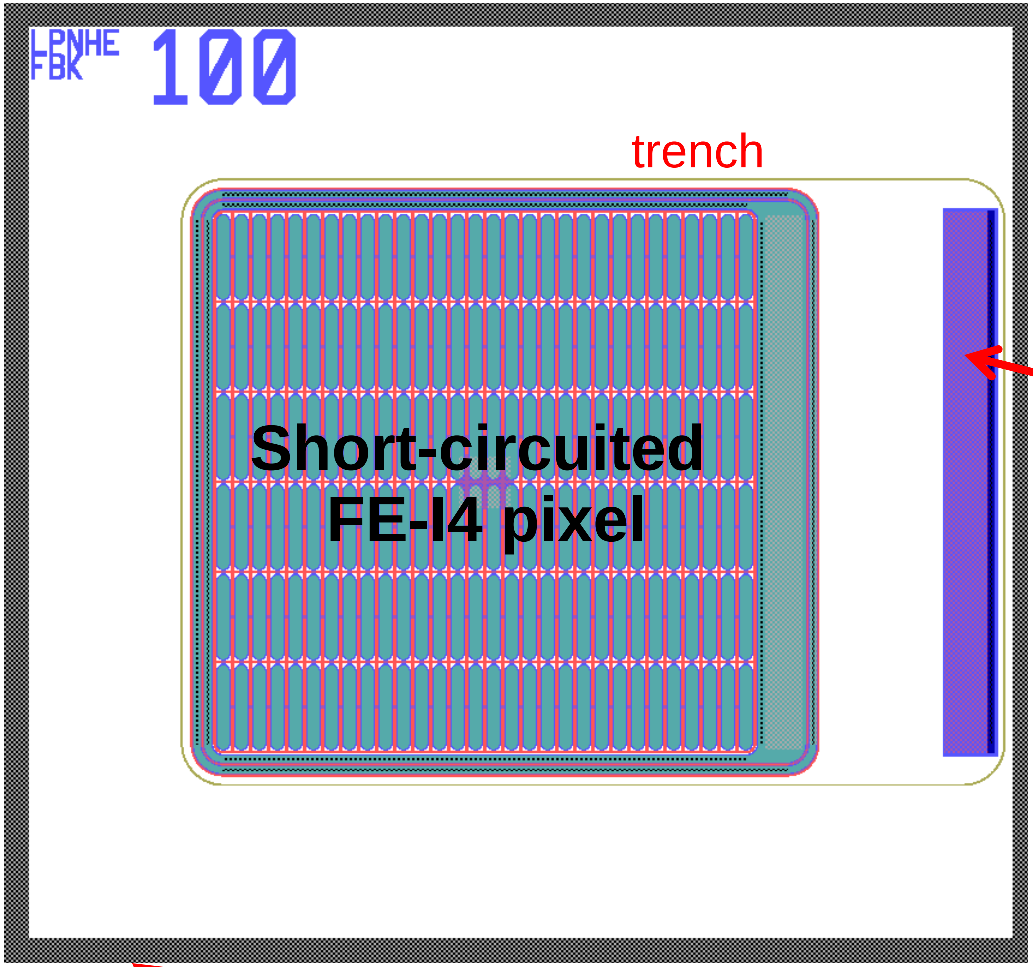
Capacitors

Gated diode

Van der Pauw and contact resistance of every implant

Test Pixel Sensors

IV Measurement: Break-down Voltage vs *n*⁺→ trench distance



Layout splittings

- 0, 1, 2, 3, 5, 10 GRs
- Different *n*⁺→trench distances

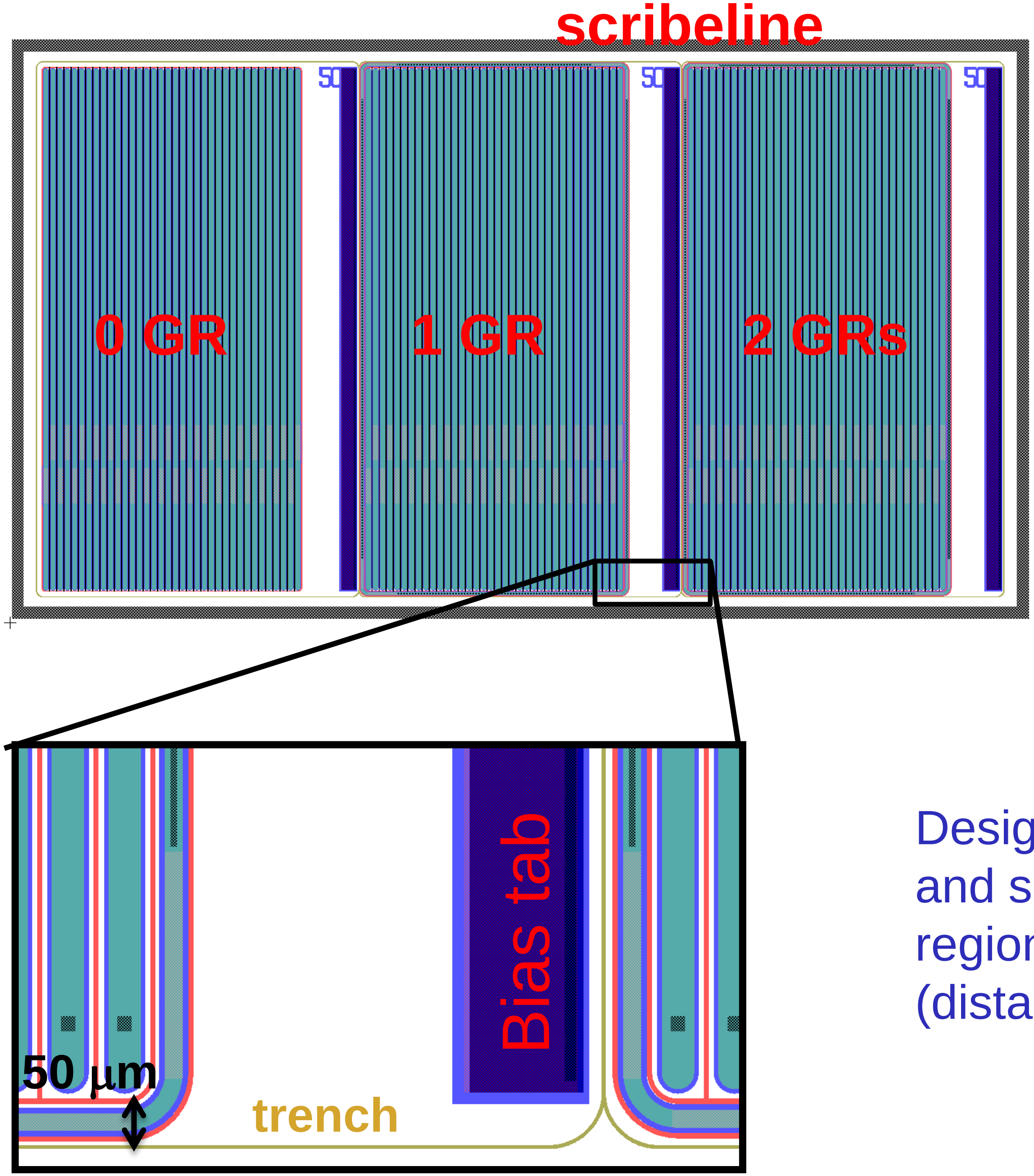
Bias Tab:
back-side in not accessible until support wafer is removed
→ ohmic (*p*) contact from front-side

Full-size FE-I4 sensors should behave exactly as these baby sensors

Scribeline:

- useful if support wafer is not removed
- its position does not affect the electrical characteristics

DC-strip sensor



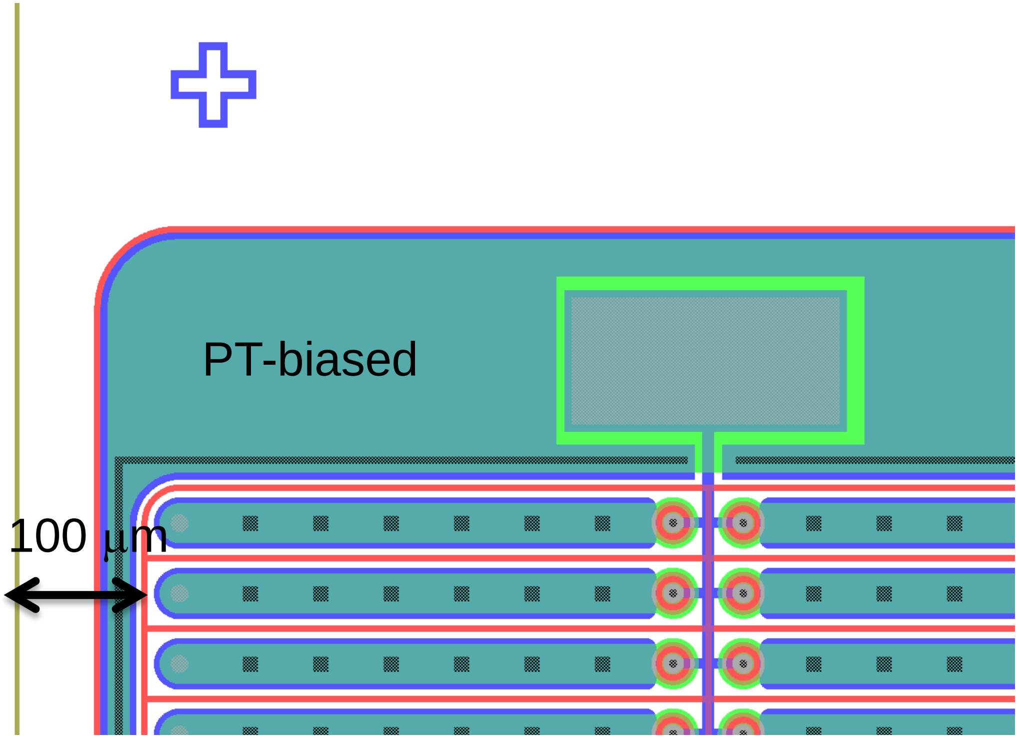
- 3-mm long strips
- Same design as pixels, only length is changed
- In a group, 3 design variants (36 strips each) (0 GR, 1 GR, 2 GRs) wire-bondable to a 128 ch ASIC
- Many groups, differing by strip → trench distance (50, 75, 100, 150 µm)

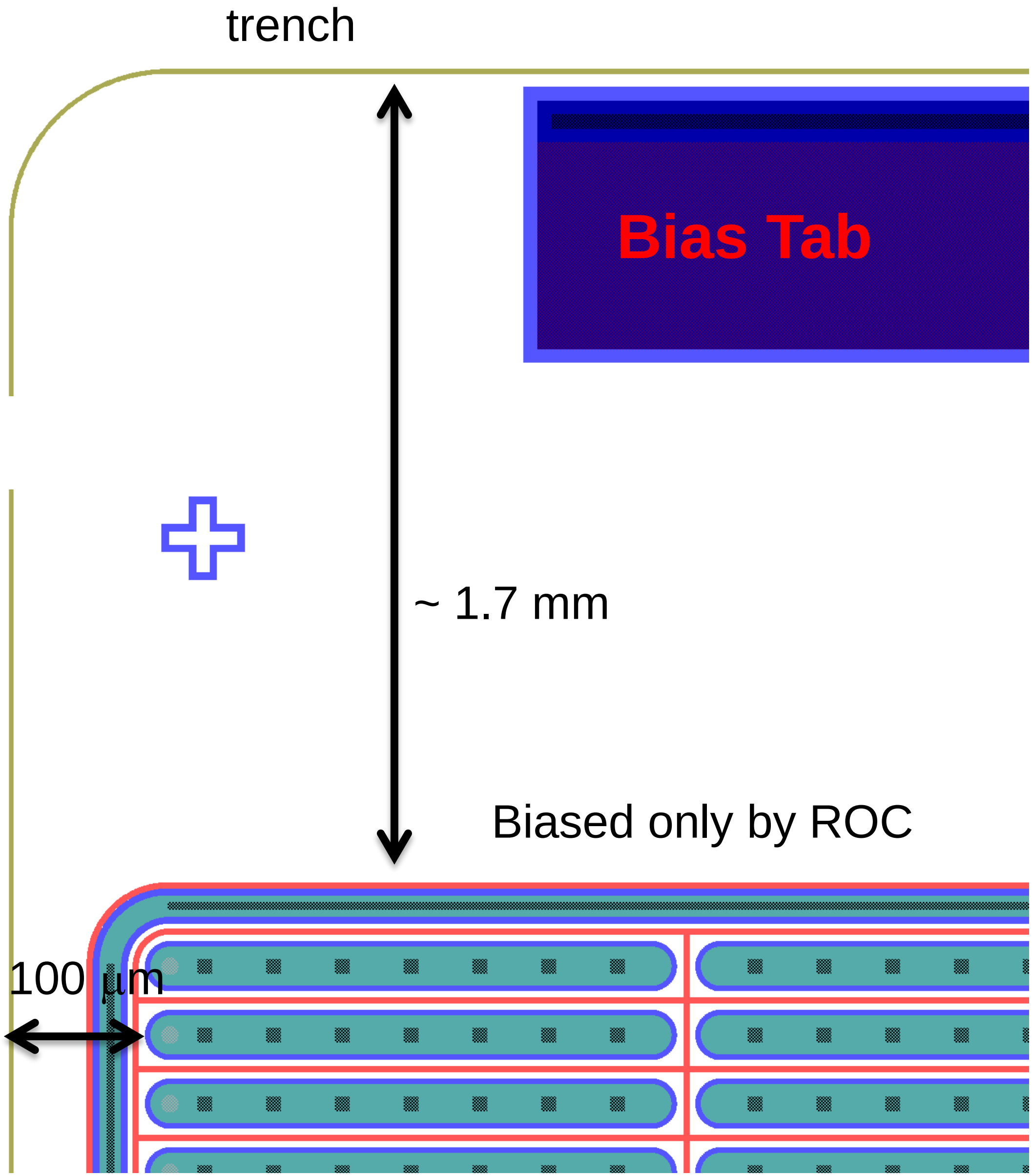
Designed for measuring efficiency and signal collection in the edge region vs. design parameters (distance to trench, # of GRs)

FE-I3 and Omega-Pix

n+ → trench distance = 100 µm

	PT biased	ROC biased
1 GR	OK	OK
2 GRs	OK	OK

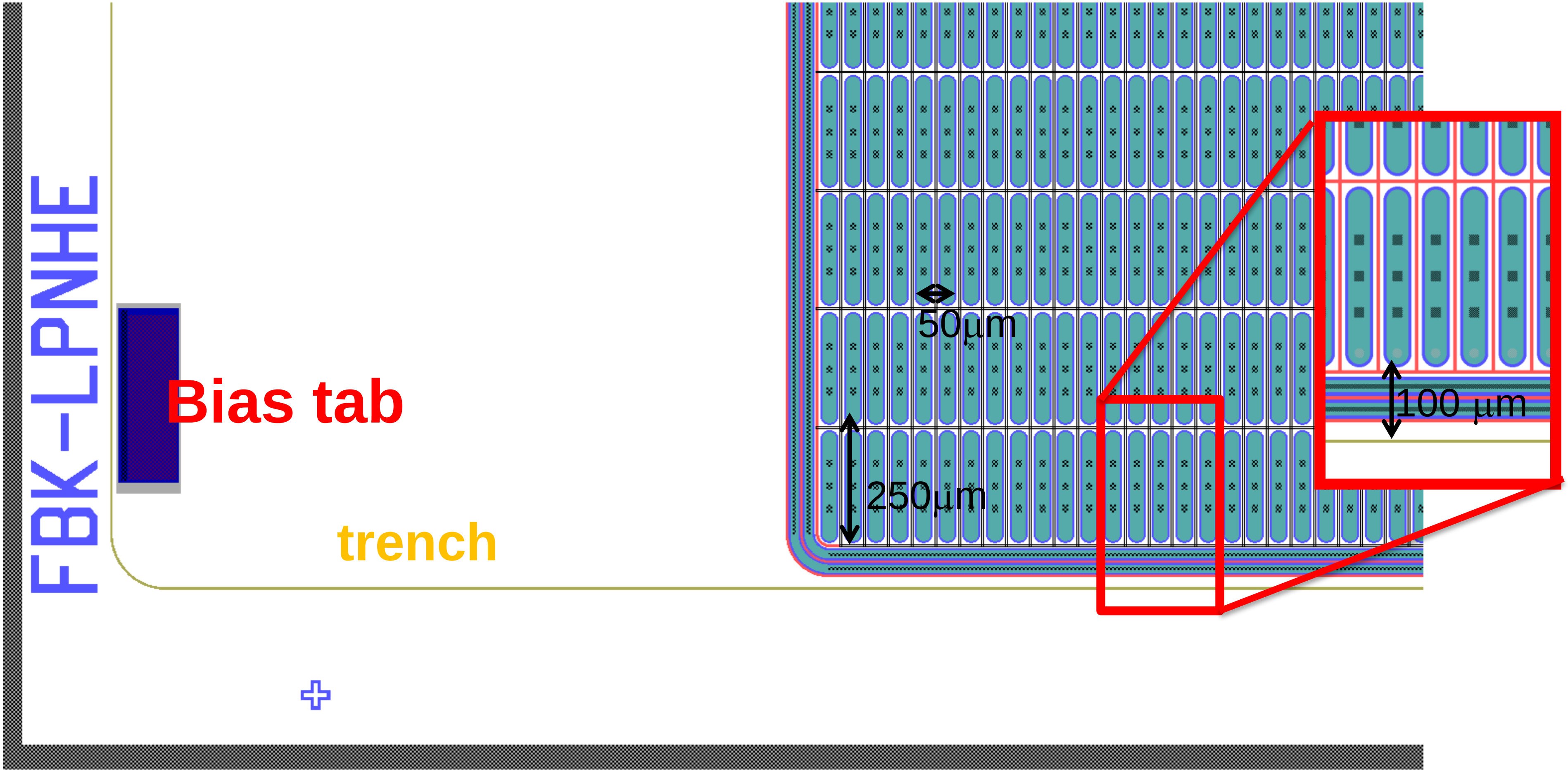




Sensors with FE-I4 Layout

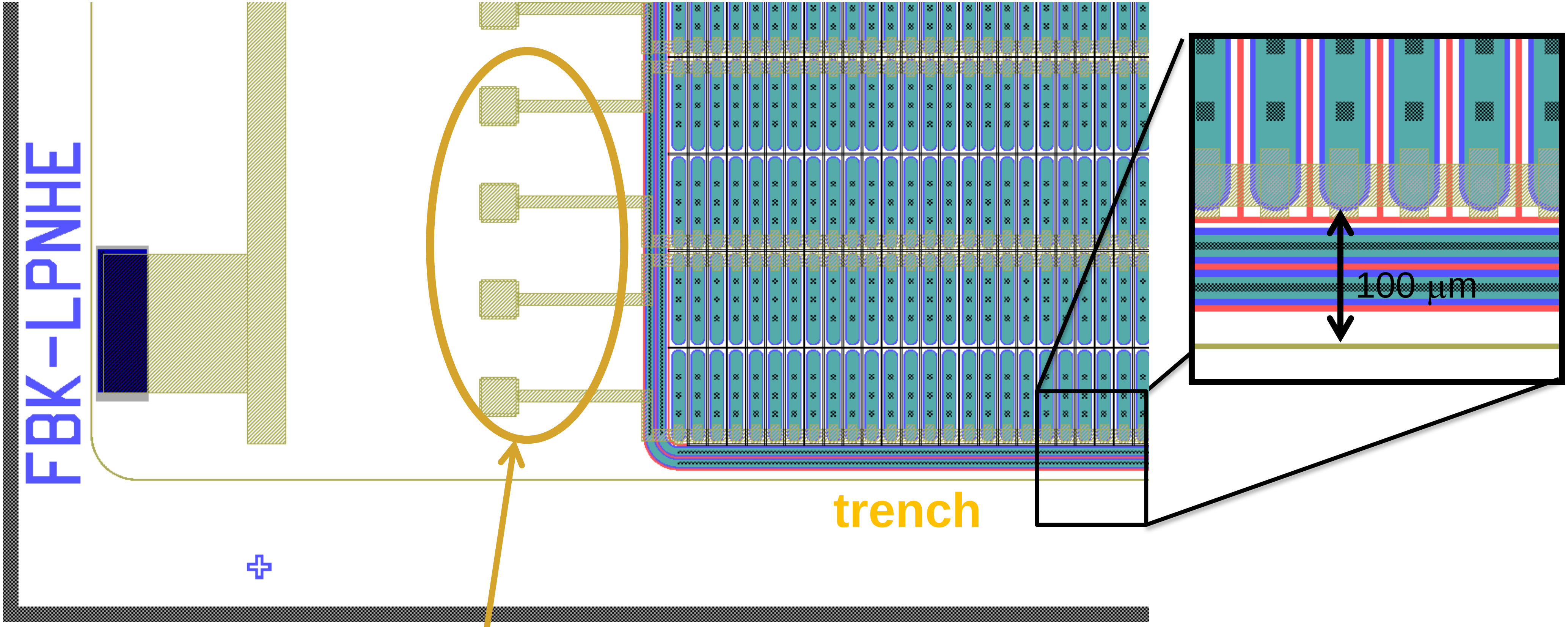
FE-I4 ROC is the newest of ATLAS and is available.
We can profit from the large experience on 3D and *n*-on-*n* read-out by FE-I4.

- **1 X 0 GR (100 μm)**
- **1 X 1 GR (100 μm)**
- **1 X 2 GR (100 μm)**
- **2 X 3 GR (200 μm)**
- **2 X 3 GR (bis) (200 μm)**
- **1 X 5 GR (300 μm)**
- **1 X 10 GR (400 μm)**



FE-I4 sensors: temporary metal

An additional metal contacts the pixel in the regions of passivation openings.
Automatic measurements on pixel sensors are possible.
Temporary metal is removed after measurements.



Temporary metal stripes (over the passivation), connecting all pixels in one row

Simulations

Mainly dedicated to BreakDown Voltage (BDV) analysis.
Varied parameters are:

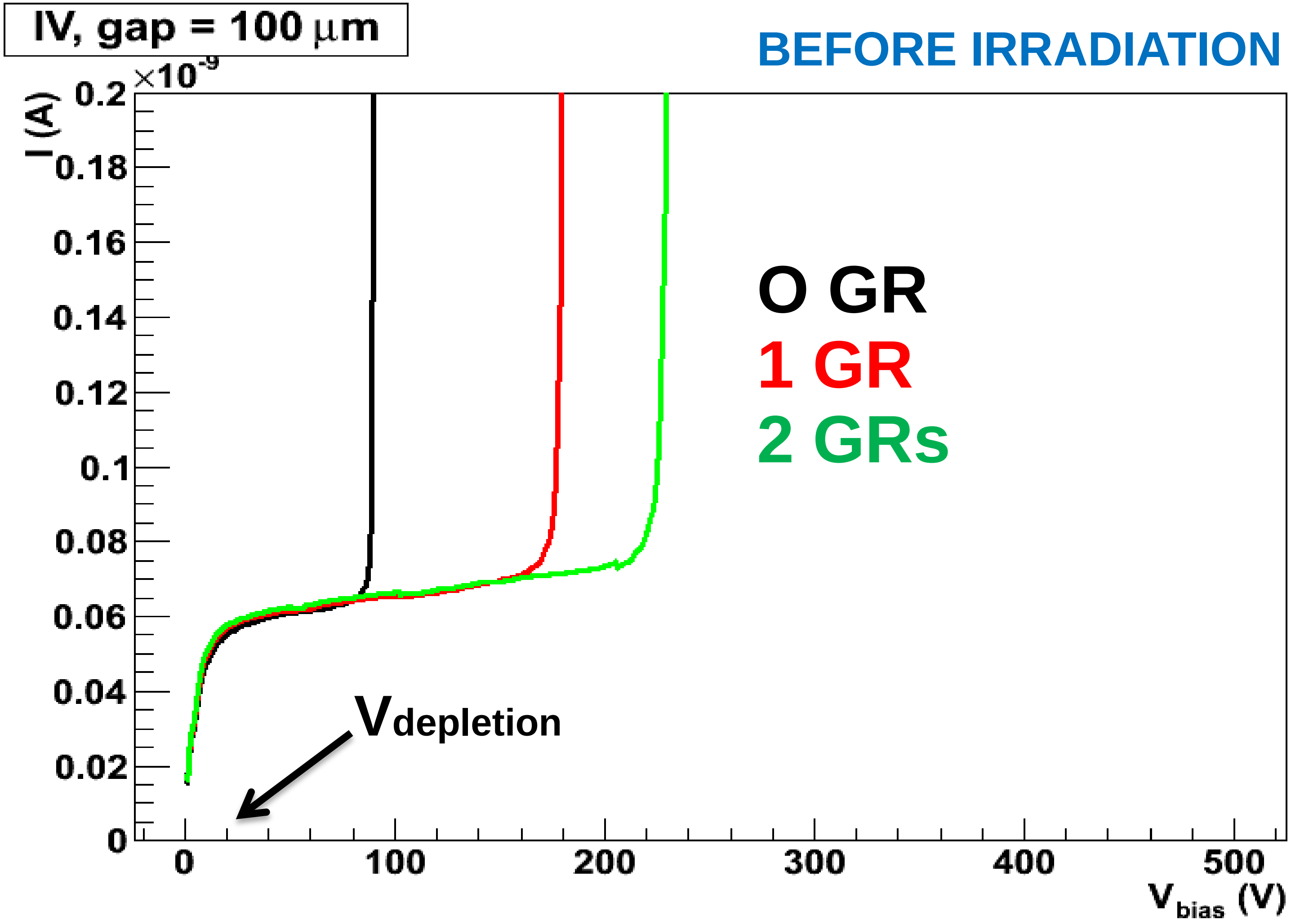
- # of GRs
- distance n+ → trench

Design covers many layout options
→ BDV can be measured on test diodes and compared with simulations
After validation with measured data, simulations can be used to improve the design,

Simulations/measurements done before & after irradiation

Simulation Example (*n*+ → trench distance = 100 µm)

BDV >> V_{depl}, also for short *n*+→ trench distance



Outlook

1) ready to start the fabrication:
   - 4-inch *p*-type 200-μm thick wafers have been bond-annealed at SINTEF
   - Final layout done! masks ready
   - ~ 4 months for processing

2) Electrical characterization
   - pixel sensors, at wafer level, making use of temporary metal (automatic measurements)
   - test structures (diode, strip,..) before and after irradiations (manual measurements)

3) Late 2012: bump bonding

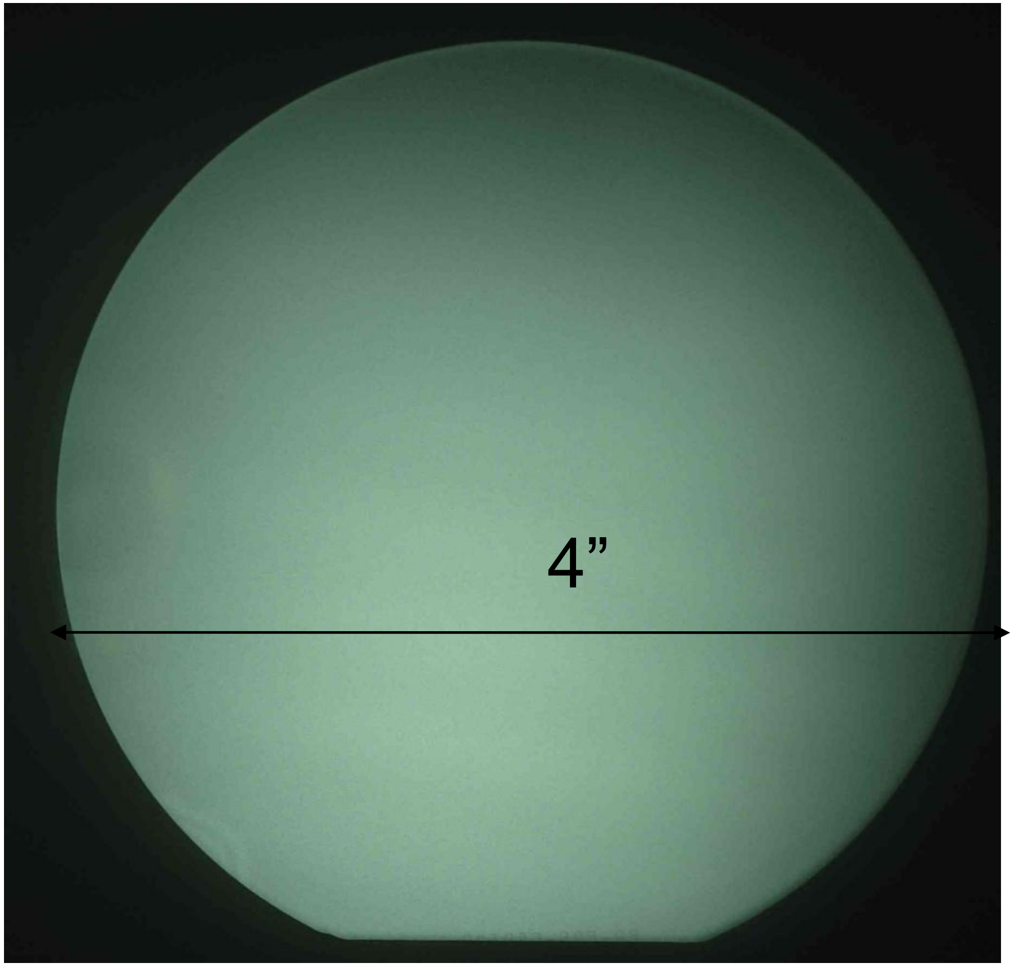
4) 2013: beam tests

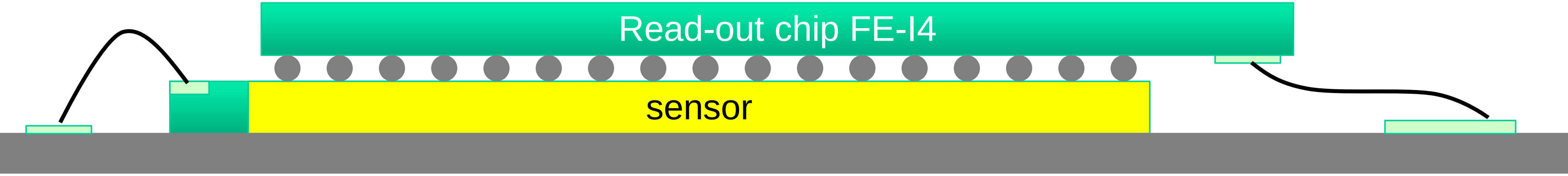
Back-up

Status

- 20 *p*-type 4” 200-μm thick wafers have been bond-annealed at SINTEF

- Microscope inspection and IR images show no particular problems




Read-out chip FE-I4
sensor