

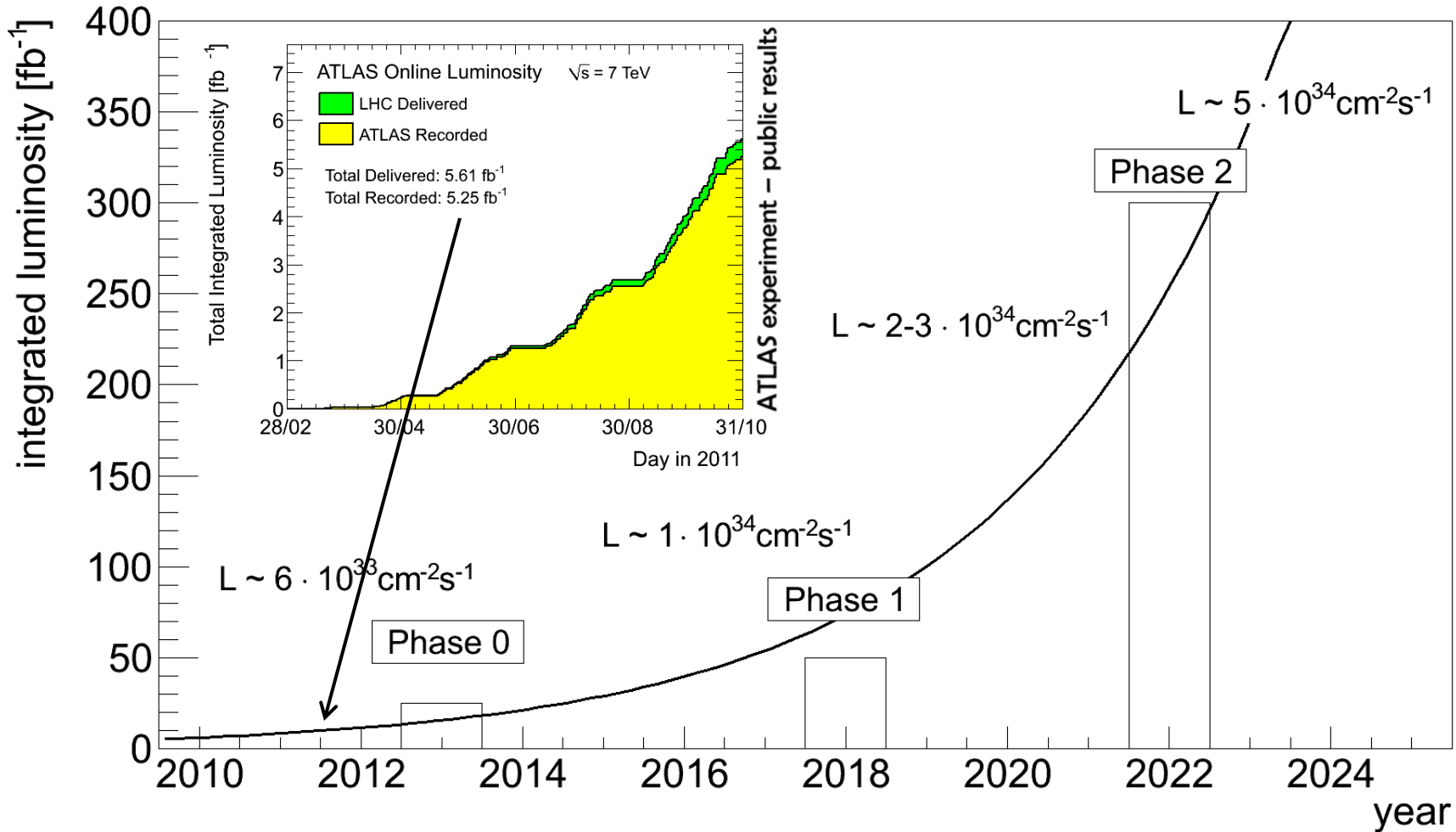
Overview of the ATLAS Insertable B-Layer (IBL) Project

Christian Gallrapp (CERN)
on behalf of the ATLAS collaboration

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LHC UPGRADE PROGRAM

LHC upgrade program

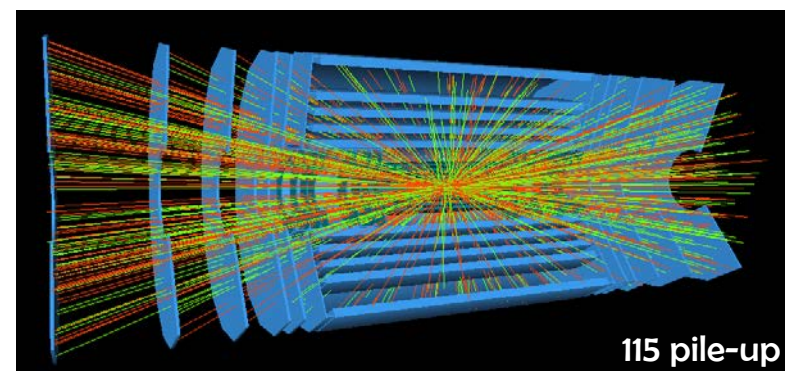
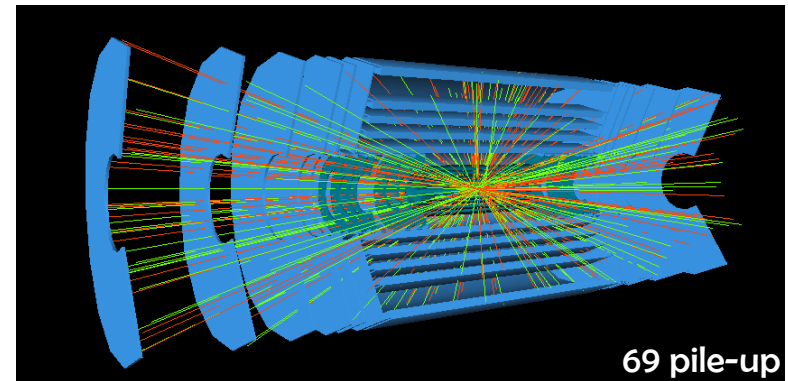
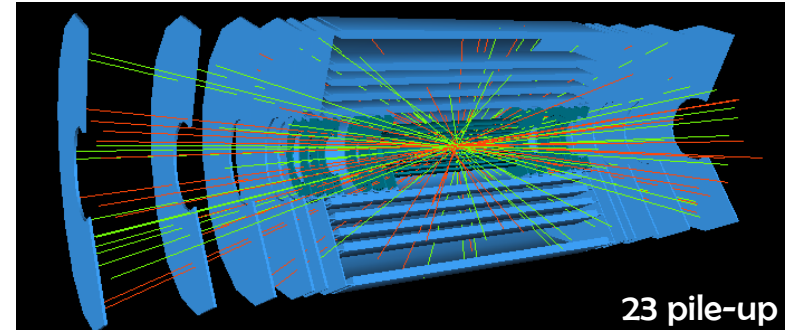


A total integrated luminosity of about 3000 fb^{-1} is expected till 2030

Based on:
Marzio Nesi, Chamonix 2012
8 February 2012

Challenges for the Inner Detector

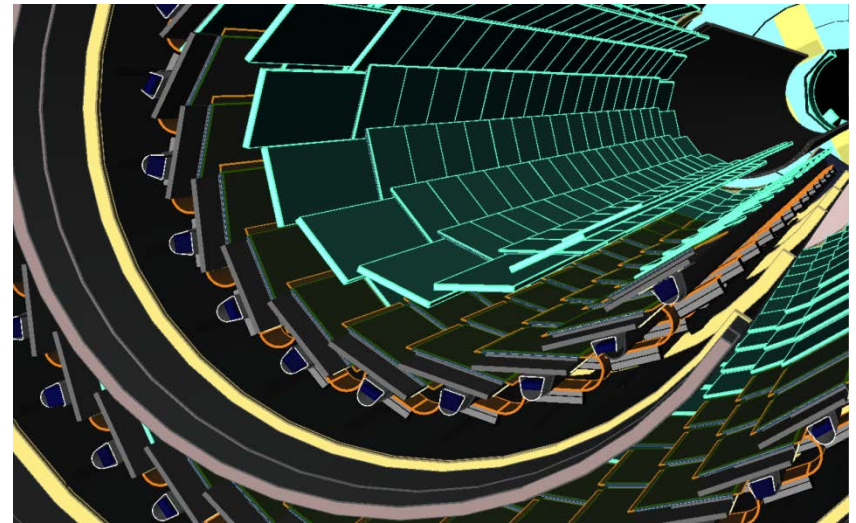
- Increased luminosity
 - Higher hit-rate capability
 - Higher segmentation
 - Higher radiation hardness
 - Lighter detectors
- Radiation hardness for the innermost layer at 3cm to 4cm
 - Phase 1: $1 \cdot 10^{15} n_{eq} cm^{-2}$
 - Phase 2: $5 \cdot 10^{15} n_{eq} cm^{-2}$
 - HL-LHC: $2 \cdot 10^{16} n_{eq} cm^{-2}$



ATLAS Pixel Detector upgrade

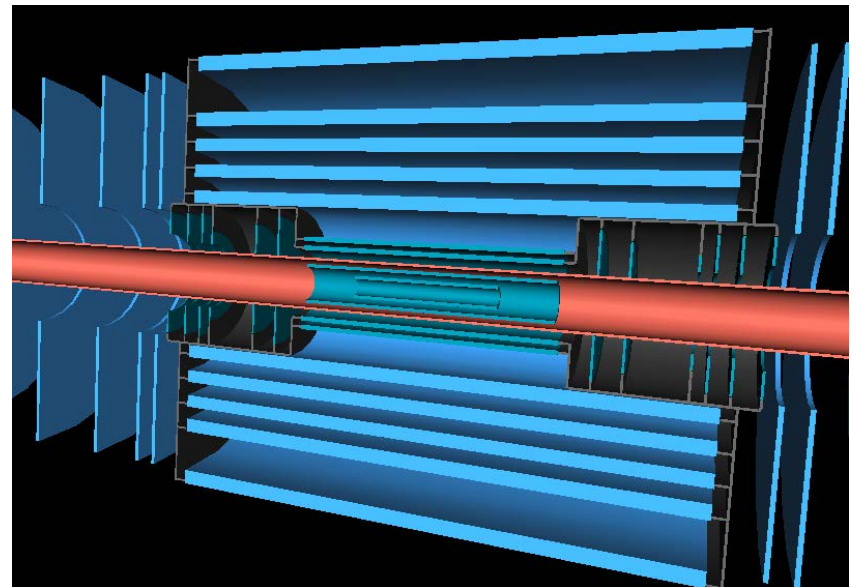
- **Phase 0 Upgrade**

The new IBL will extend the pixel detector system to a 4-layer system with finer segmentation and at a smaller radius



- **Phase 2 Upgrade**

Complete new ATLAS tracker for pixels and strip detectors

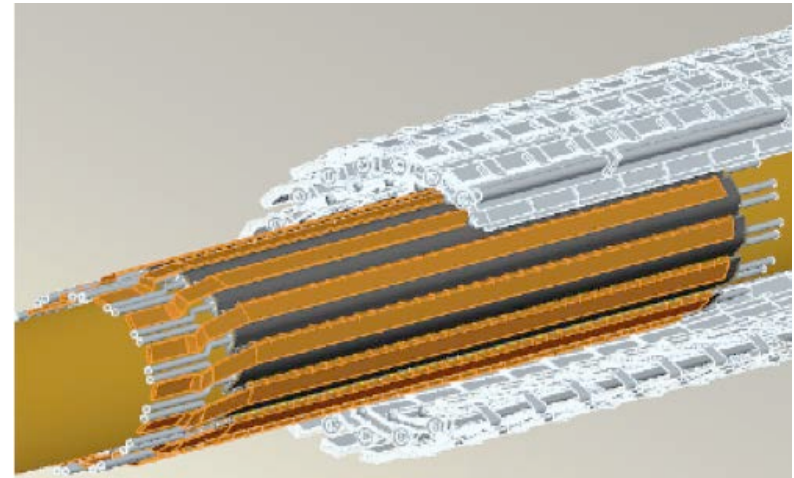
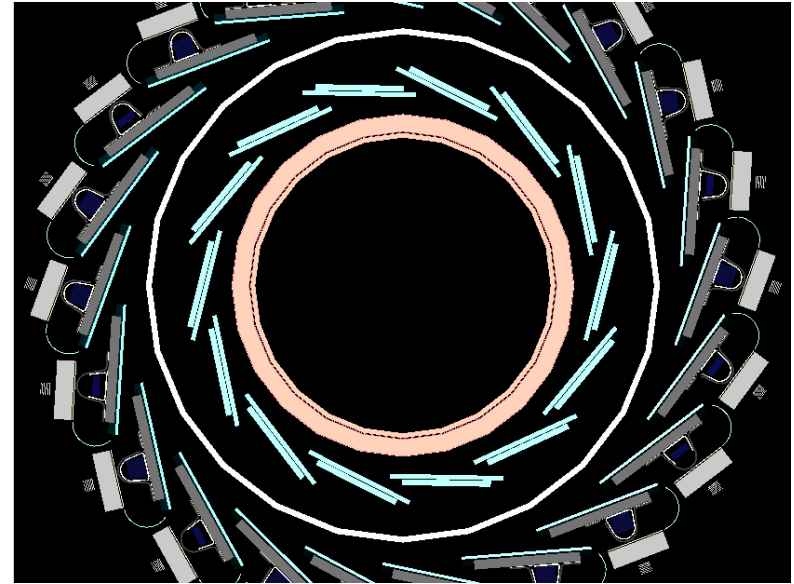


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IBL UPGRADE

IBL upgrade

- IBL Properties
 - Smaller beam pipe ($R_{\min} = 26.5 \text{ mm}$)
 - Smaller z pitch ($250 \mu\text{m}$)
 - Material budget adjusted to 1.5% XO
 - 250 Mrad TID and $5 \cdot 10^{15} \text{ n}_{\text{eq}} \text{cm}^{-2}$ NIEL
- Layout is based on performance studies within the ATLAS Simulation framework and the available space
- Fourth pixel layer for tracking in ATLAS
- Maintain and improve physics performance (b-tagging, light jet rejection) until HL-LHC
- IBL layout
 - 14 staves
 - 32 FE-I4 chips per stave
=> 448 FE-I4 chips in total
 - Available Sensor technologies
 - 3D sensors as single chip modules
 - Planar sensors as double chip modules



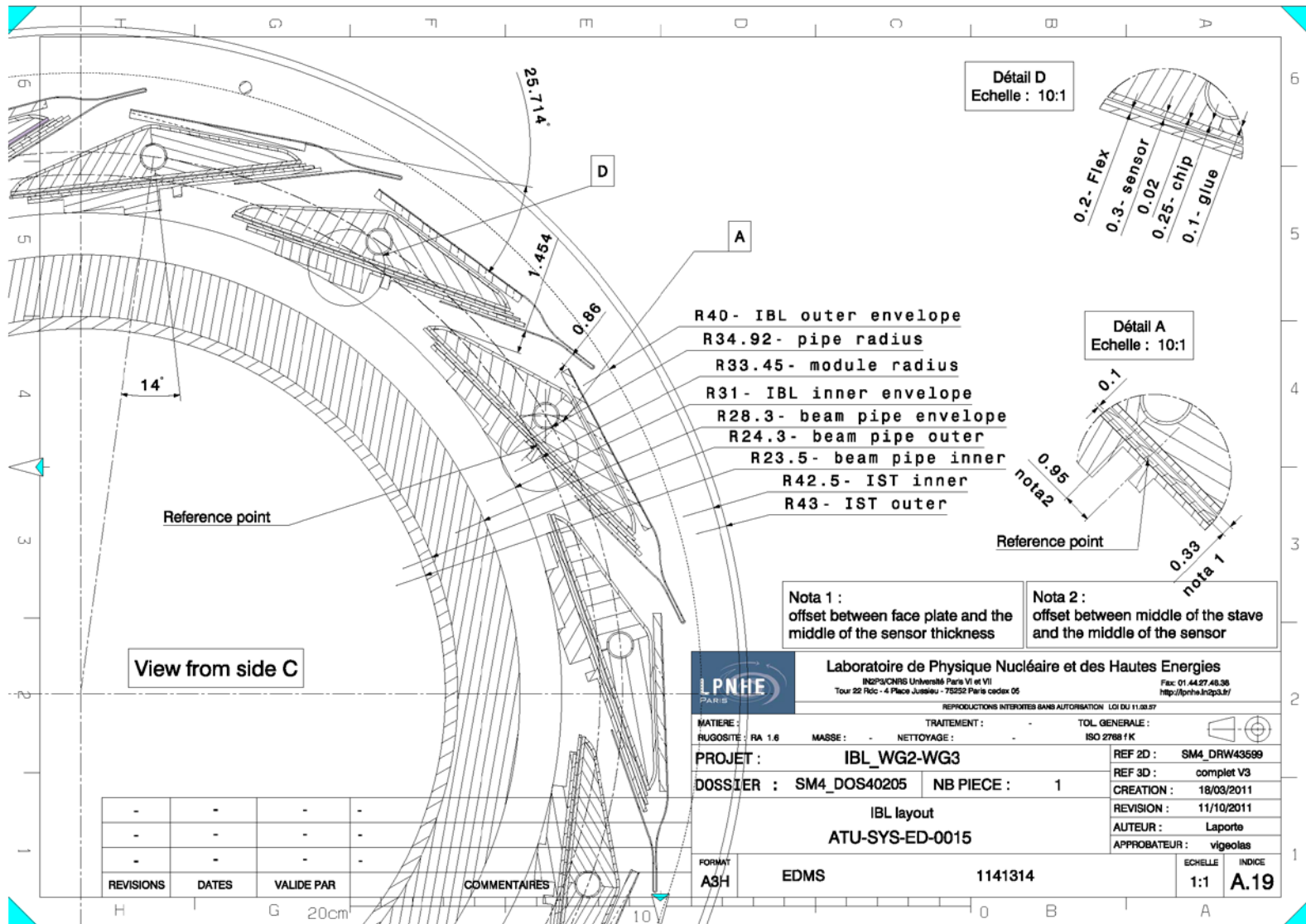
CERN-LHCC-2010-013

ATL-INDET-SLIDE-2011-251

IBL Requirements and Specifications

- **Higher radiation hardness**
 - $5 \cdot 10^{15} \text{ n}_{\text{eq}} \text{ cm}^{-2}$ NIEL (Improve radiation hardness by factor 5)
 - max. power dissipation: 200 mW cm^{-2} at -15°C
 - tracking efficiency $> 97\%$.
- **New readout chip with fine segmentation, more active area and improved hit-rate capability**
 - New readout architecture and smaller cell size $250 \cdot 50 \mu\text{m}^2$
 - Large single-chip ($21 \cdot 19 \text{ mm}^2$)
 - Radiation hardness $> 250 \text{ Mrad TID}$
- **Lighter detector: less radiation length in support and cooling**
 - improve radiation length per layer from 2.7% to $\sim 1.5\%$ to minimize multiple scattering in closest layer
 - Requires lighter and less material for support and cooling
 - High efficiency CO_2 cooling at -40°C coolant temperature
- **New off-detector readout system**
 - Matched to FE-I4 pixel chip
 - Increase readout speed by a factor of two

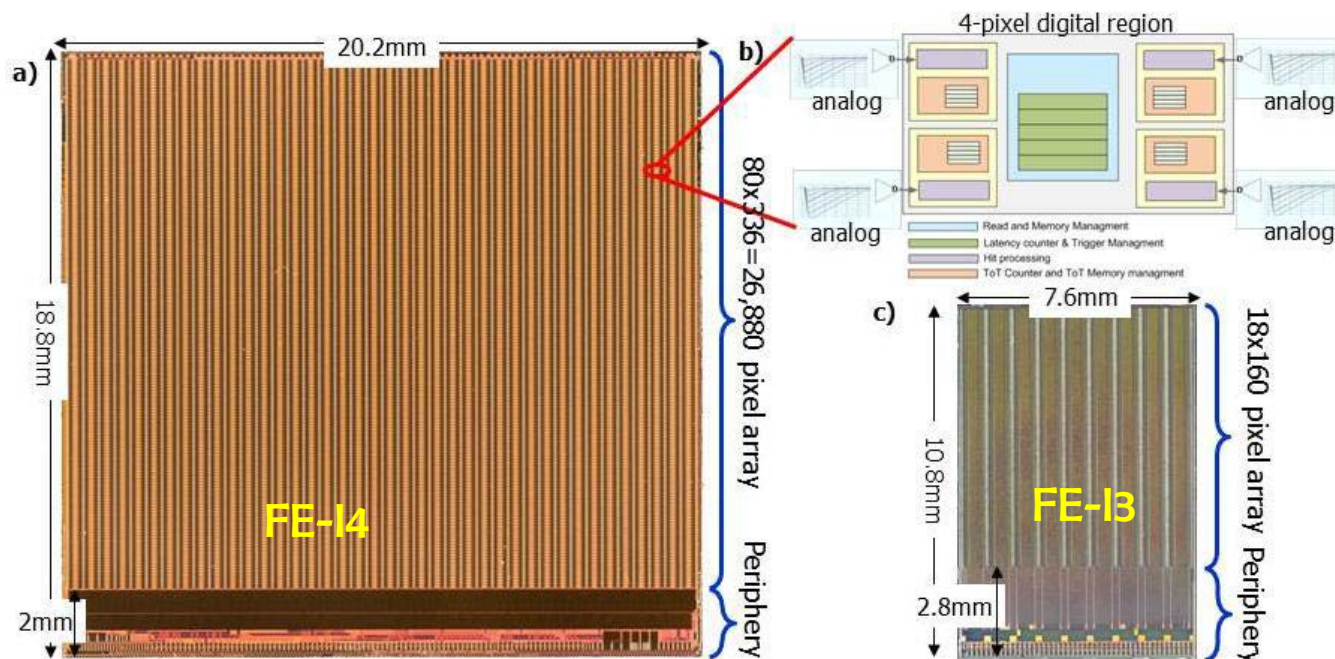
IBL layout



EDMS: 1141314

ATLAS FE-14

- Smaller pixels ($50 \cdot 250 \mu\text{m}^2$)
- Lower noise and threshold operation
- Compatibility for higher data rates
- Column drain architecture with local hit storage
- IBM 130nm process
- Largest chip to date in HEP:
 - maximize active area and reduce bump-bonding costs
- array size: 80 col. x 336 rows
=> 26880 pixels, 8×10^7 transistors
- average hit rate at 1% inefficiency
=> 400 MHz cm^{-2} ; max. trigger rate: 200kHz

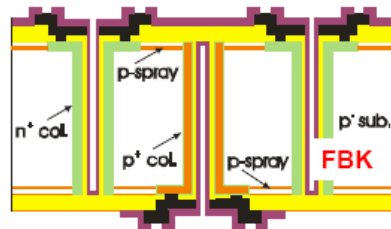
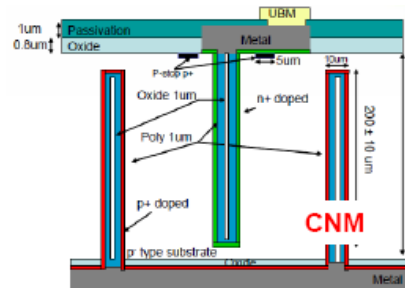
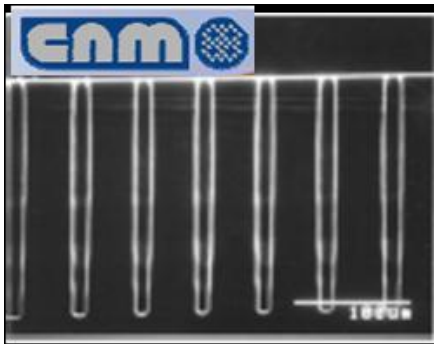


ATL-UPGRADE-PROC-2012-001

IBL Sensors Technologies

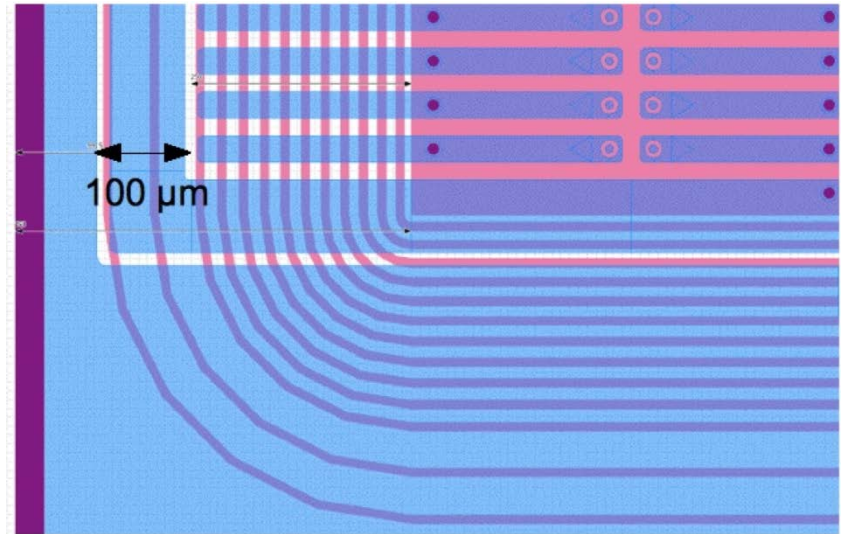
3D slim edge (FBK, CNM)

- Horizontal depletion (short depletion width leads to low bias voltage)
- Different processing but common top-layer mask for chip connection
- Manufacturing yield now being tested with pre-production runs by CNM and FBK

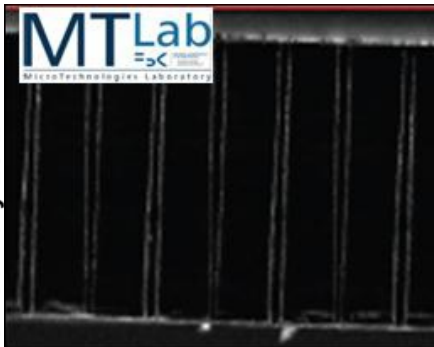


Planar n-in-n slim edge (CiS)

- minimize inactive edge by shifting guard rings underneath active pixel region
- Ongoing efficiency studies after full IBL irradiation
- Manufactured by CiS like present pixel sensors



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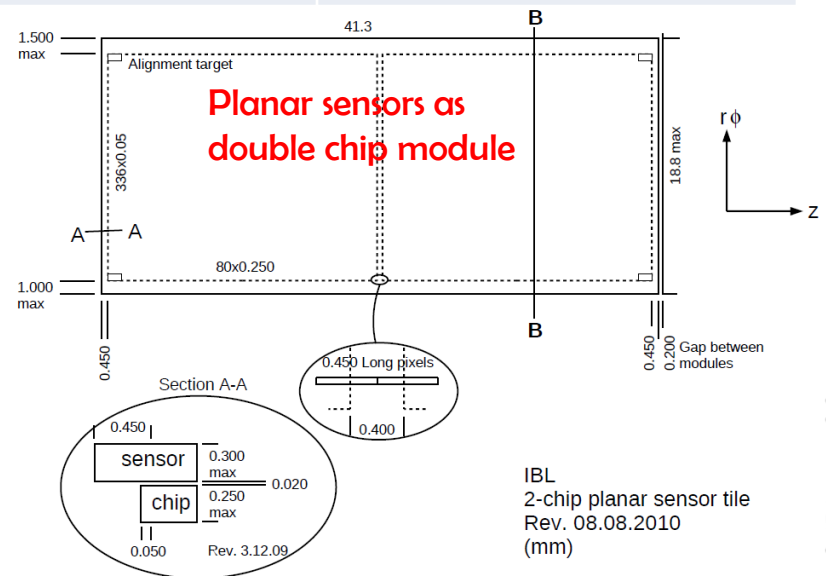
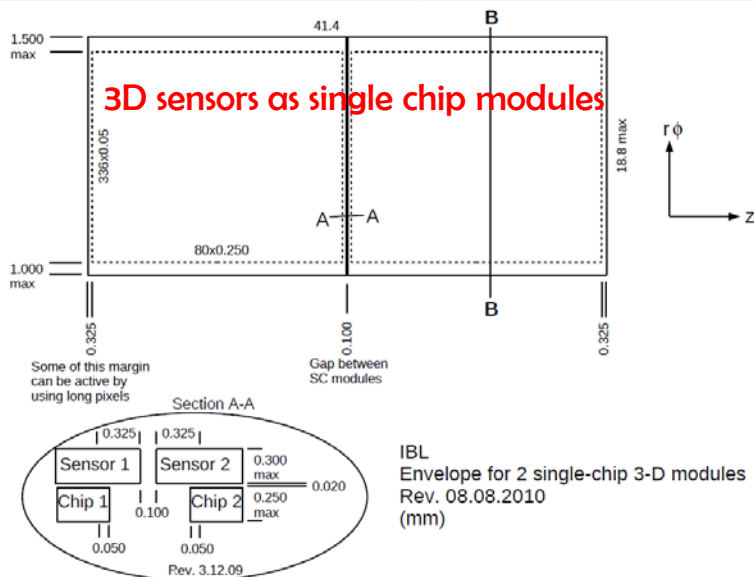


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MODULES AND STAVE

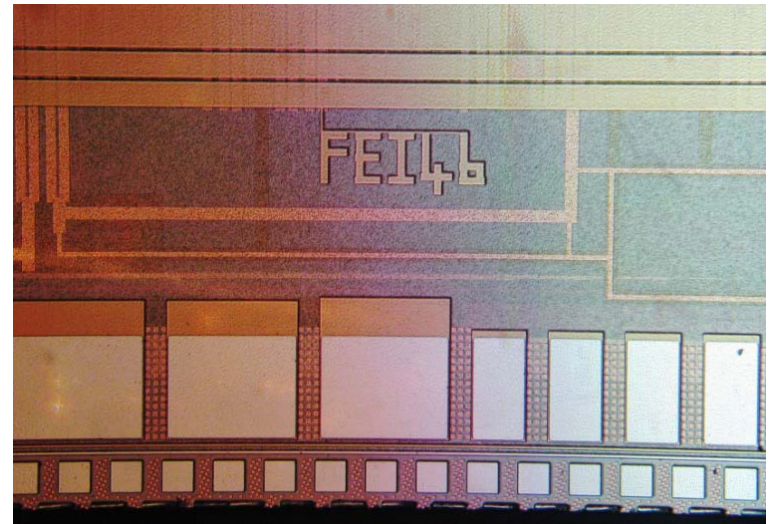
IBL modules

3D n-in-p sensor	Property	Planar n-in-n sensor
16.8 x 20.0	Active size $W \times L$ [mm ²]	16.8 x 40.9
18.8 x 20.5	Total size $W \times L$ [mm ²]	18.54 x 41.27
230	Thickness [μm]	200
≤ 15	Typical depletion voltage [V]	≤ 35
25	Typical initial operation voltage [V]	60
180	Operation voltage at the end of lifetime [V]	1000



IBL module production (I)

- Decision to install IBL in 2013 came in January 2011
 - Crash program to submit production version of chip in a few months
- Verification of new FE-I4B chip
 - Chip “has to work”
- Submission and tests
 - 16 wafers received in December 2011 and 8 wafer in February 2012
 - One diced wafer at LBNL by December 2011
 - 2 chips tested and in beam at LANL by December 2011



IBL module production (II)

ATLAS Pixel extended Institute Board endorsed the recommendation of the review panel:

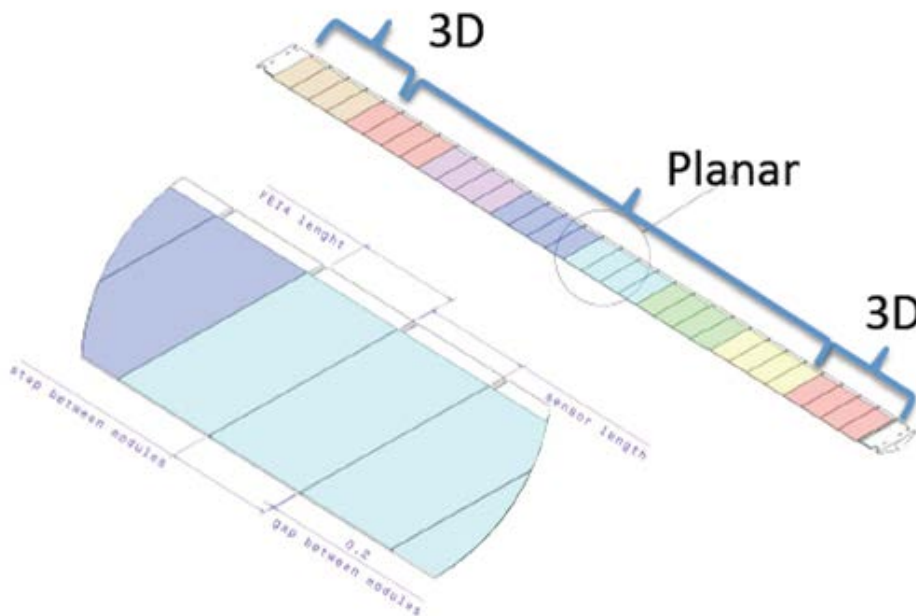
- produce enough Planar sensors to build 100% of the IBL
- continue current 3D sensor production to build 25% of the IBL

3D n-in-p sensor

- 6 batches in production: 3 at CNM and 3 at FBK, the first 3 batches will go to IZM for bump-bonding
- 49 out of 50 selected wafer available
- first batch now at IZM for bump-bonding

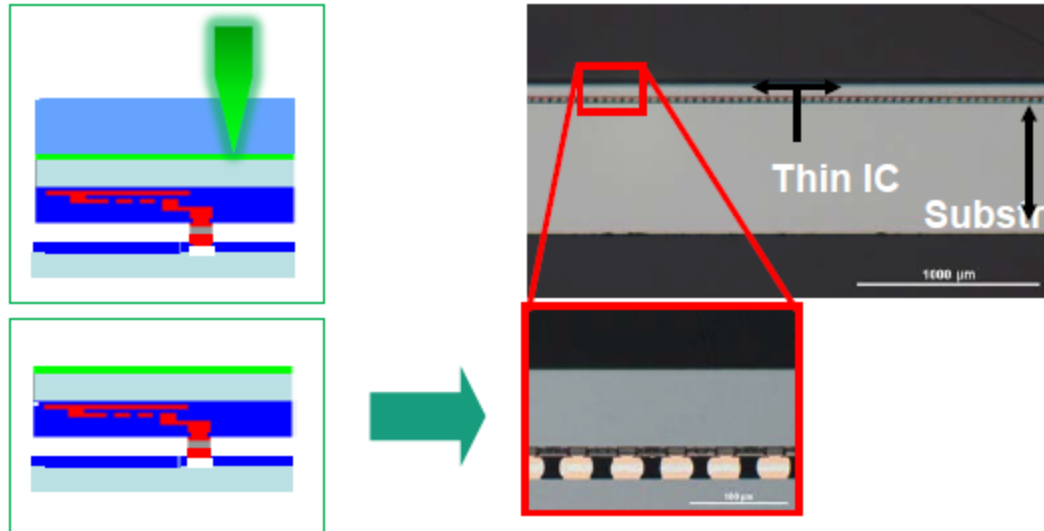
Planar n-in-n sensor

- 6 batches in production at CIS
- 119 out of 150 accepted wafer received
- 3 batches at IZM for bump-bonding



IBL bump-bonding

- Over 78 single-chip assemblies with planar and 3D sensors have been bump-bonded for the sensor qualification in 2011
- Thin FE-I4 (100 μm and 150 μm) on planar and 3D sensors have been prepared by IZM to test the feasibility of thin modules (i.e. final IBL modules):
 - first modules single and double chip have been produced successfully with 100 μm and 150 μm thick FE-I4A
 - 31 planar double chip and 17 3D single chip modules with thin FE-I4 chips done as pre-production to IBL module specifications



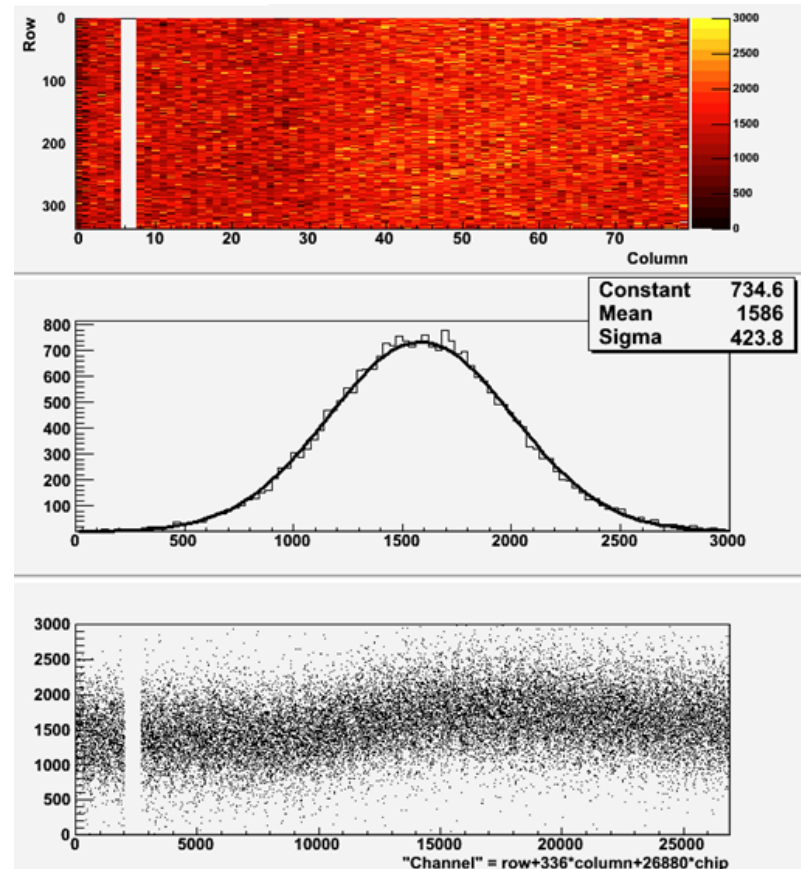
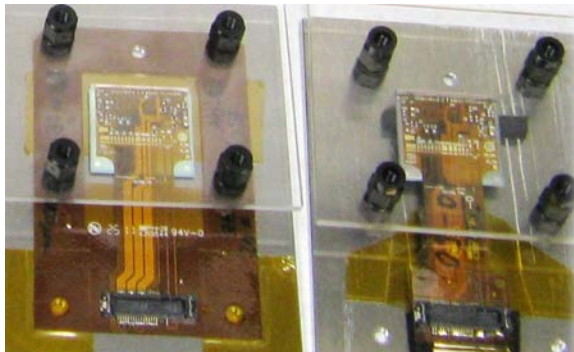
Test results on production chips

Characterization and tests of FE-I4B:

- 1 single chip tested so far on single-chip cards to test basic functionality and analog part
- New and corrected features with respect to FE-I4A are working fine
- More testing of FE-I4B needed before final conclusion on chip quality
- First chips have been irradiated

Wafer testing:

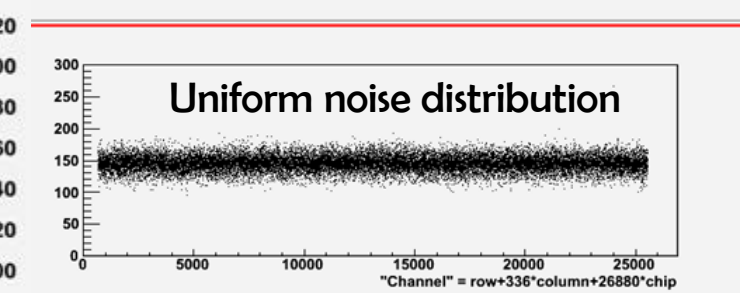
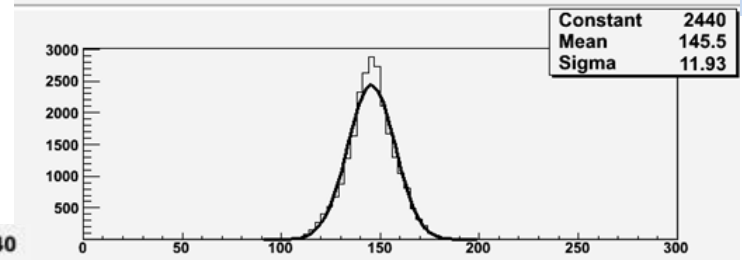
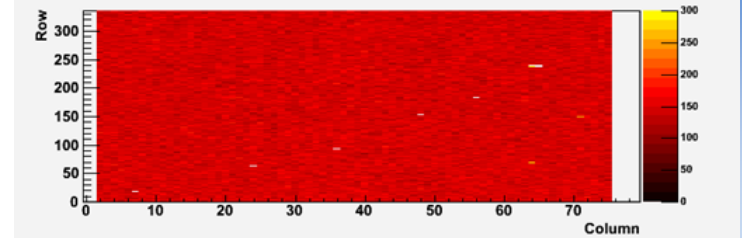
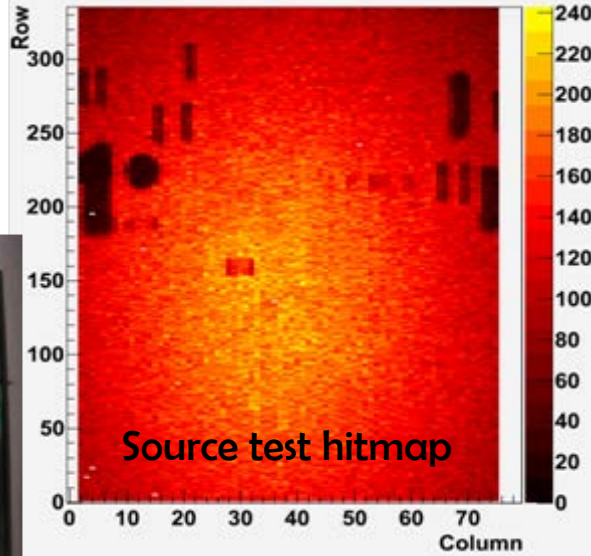
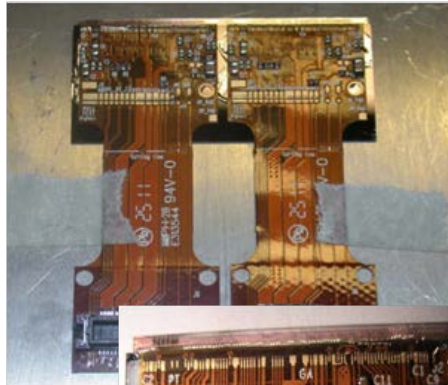
- Tests on FE-I4A wafers (scan chain etc...). Understanding of test results in progress.
- First batch of FE-I4B wafer tests during February -> All indicators are green so-far



Threshold scan of un-tuned chip shows the expected analog response

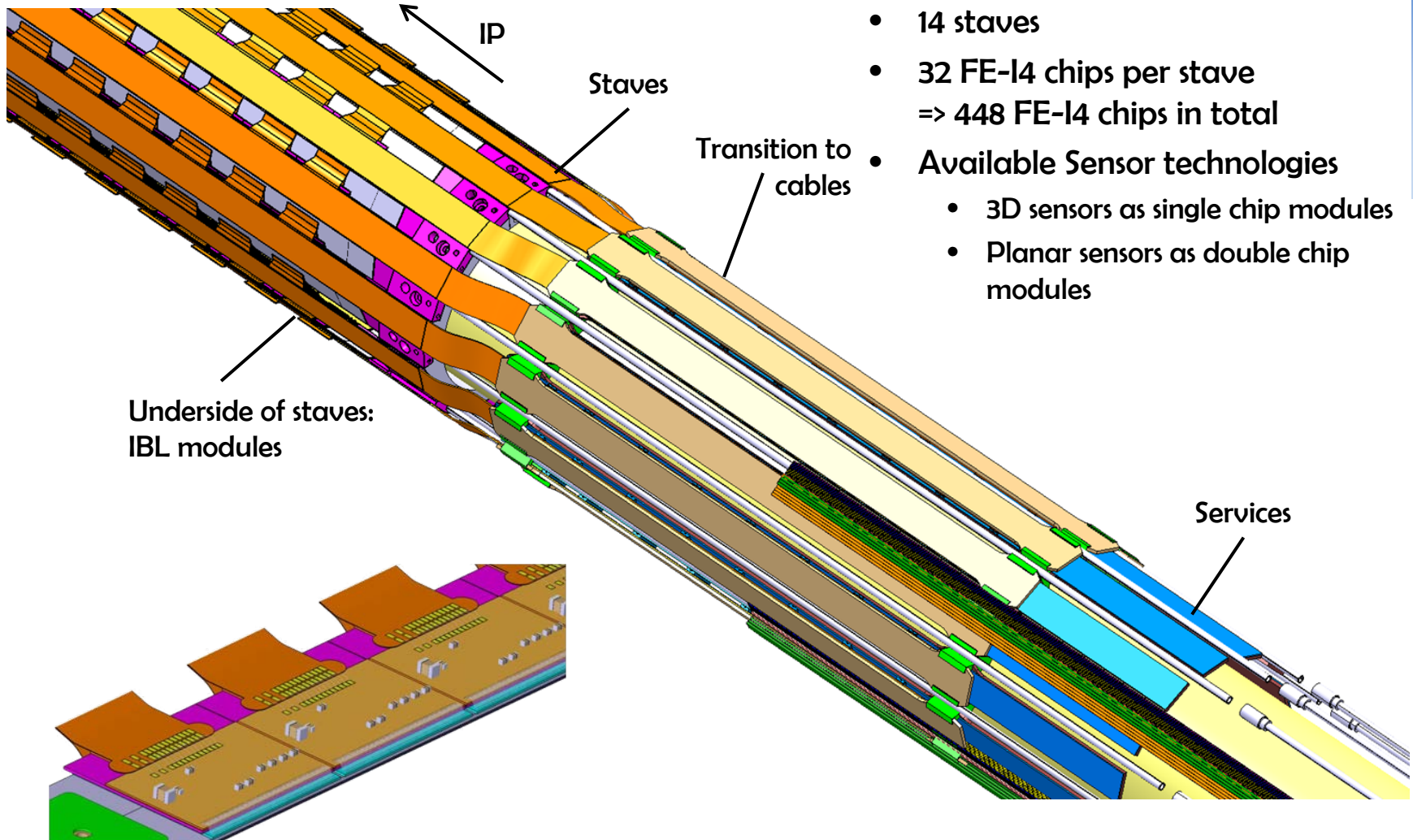
Tests on assembled IBL modules

- Finished pre-production with FE-I4 to
 - Test final module design
 - Prepare and test assembly and quality assurance procedure
 - Lab tests with calibration, Am-241 and Sr-90 sources
 - Good performance so far
- Finalizing module flex for final FE-I4B chip



- Production is running fine
- Expect first FE-I4B production modules end April
- Production will run until ~ end of 2012

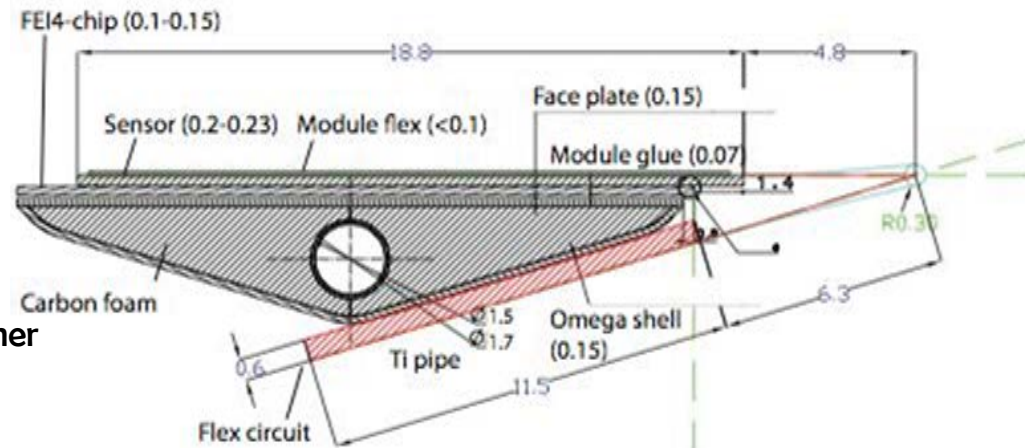
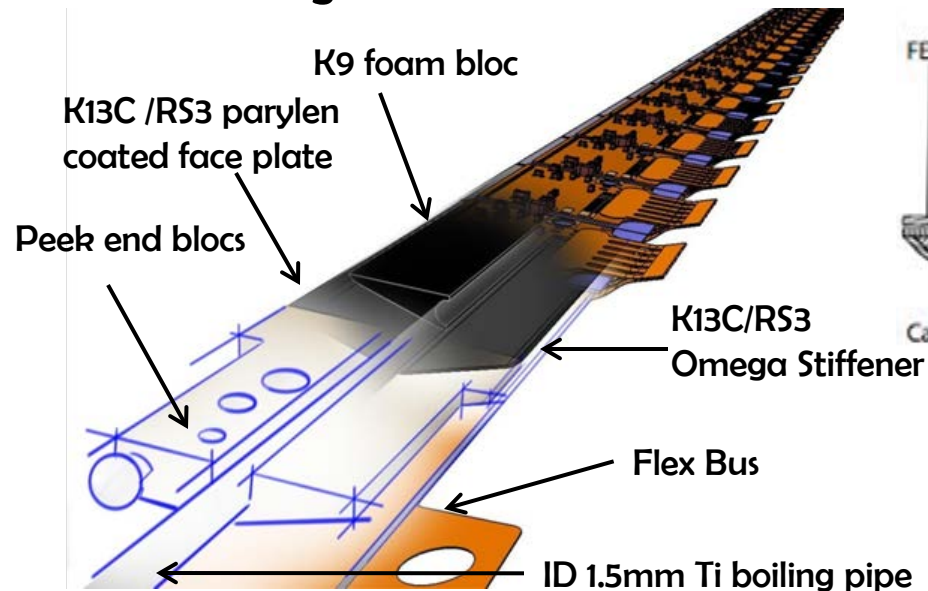
IBL stove



- 14 staves
- 32 FE-I4 chips per stove
=> 448 FE-I4 chips in total
- Available Sensor technologies
 - 3D sensors as single chip modules
 - Planar sensors as double chip modules

IBL carbon-fibre support

- Carbon-fibre support structure with minimal material budget
 $X/X_0 \sim 0.5\%$ for support and cooling
- Optimized stiffness and thermal conductivity
- Match thermal expansion
- Material qualification for use in high-radiation environments (300Mrad)
- Detector cooling with a CO_2 system working -40°C to minimize the leakage currents of the sensors



Stave production

- Bare stave production running -> 6 of 42 received
 - carbon fiber (K13C) Omega glued on the foam to provide mechanical rigidity and to assure the heat transfer to the central cooling pipe
 - Qualified with pressure tests, brazing to external pipes, deformation survey and flatness of staves and thermal conductivity to cooling pipe

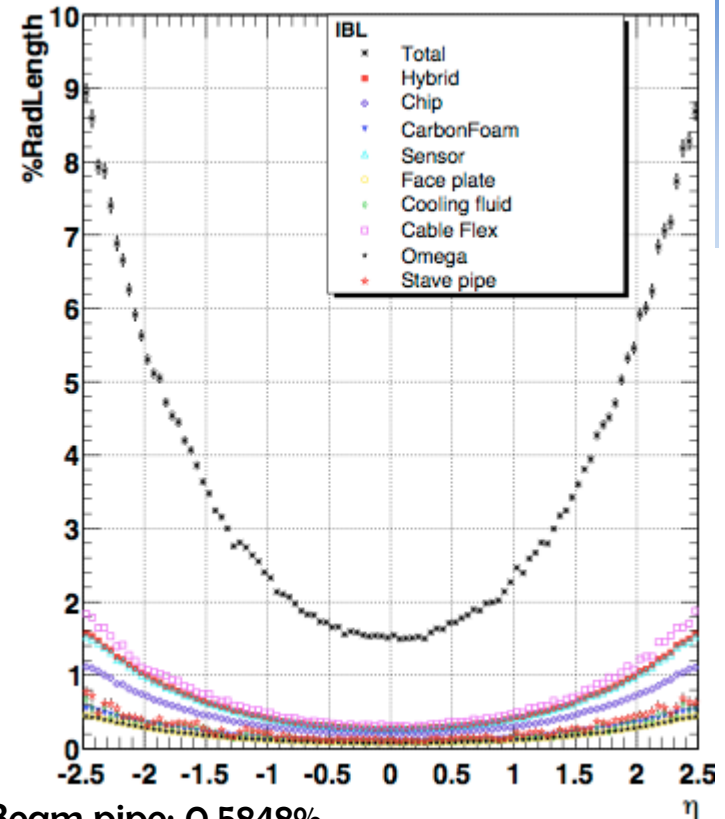
Design:

- Titanium cooling pipe
 - Inner diameter: 1.5mm
 - Wall thickness: 0.1mm
- 3 layer (0/90/0) face plate
- EOS and Central Peek support
- Flex fully glued on the Omega
- Short stave for loading (1300mm)



IBL Material Budget

- Status of X_0 in summer 2011 (end of prototyping):
 - perpendicular incident, smeared over active surface, average over stave length $\eta < 3$
- Task force in place to monitor actual X_0 during construction
- Increase of X_0 during prototyping from 1.5% (TDR) to 2.0%
- Decrease of $X_0 = 1.5\%$ after reduced material budget
- Aim on keeping X_0 within reasonable engineering limits



Beam pipe: 0.5848%

IST: 0.2151%

Stave: 0.6628%

Modules: 1.1395%

Total IBL (IST + staves + modules): 2.0174%

Services: ~1%

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OUTLOOK

IBL schedule overview

Activity	Starting	Ending
FEI4-B	September 2011: Submission	December 2011 chips received, tests of 1 st batch completed by the end of February 2012
Bump bonding	August 2011: pre-production	November 2012: Completion (incl. spares)
Module assembly	End May 2012: 1 st modules ready for loading	December 2012 (spare and contingency incl.)
Module loading	July 2012: → 4 staves to be ready by September 2012	April 2013: Completion (spare and contingency incl.)
Stave loading	Mar 2012: starting with the 1 st available staves	June 2013: Completion
Final tests and commissioning	July 2012	September 2013: IBL Installation

- FEI4B is as scheduled and working fine – Wafer tests to survey
- Next key step: module production with FEI4B to demonstrate the electrical functionality of the stave (flex, module, off-detector readout)
- Loading of first stave with pre-production modules is expected around March/April and first production staves July 2012

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**THANK YOU FOR YOUR
ATTENTION**