Radiation-hard active sensors in 180 nm HV CMOS technology

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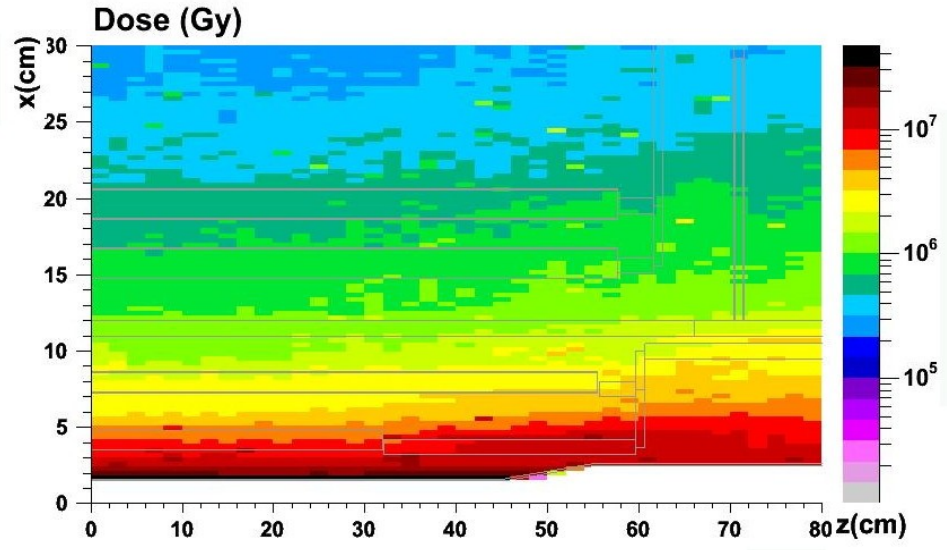
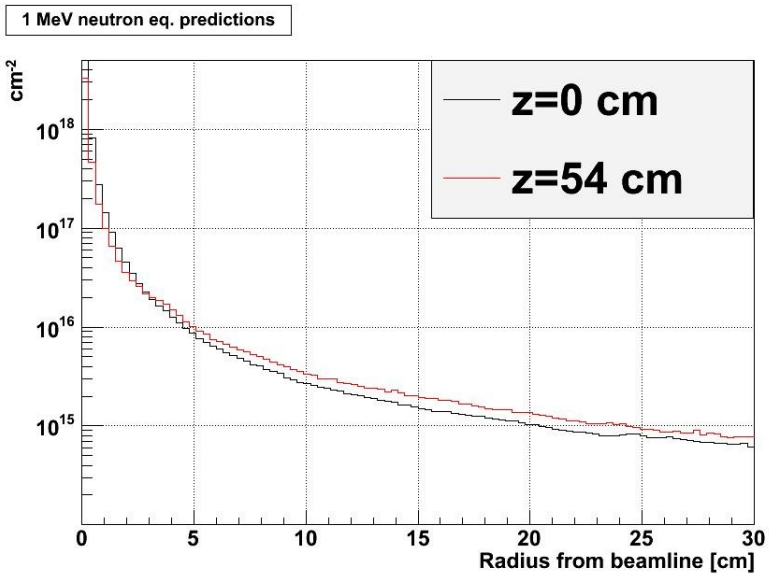
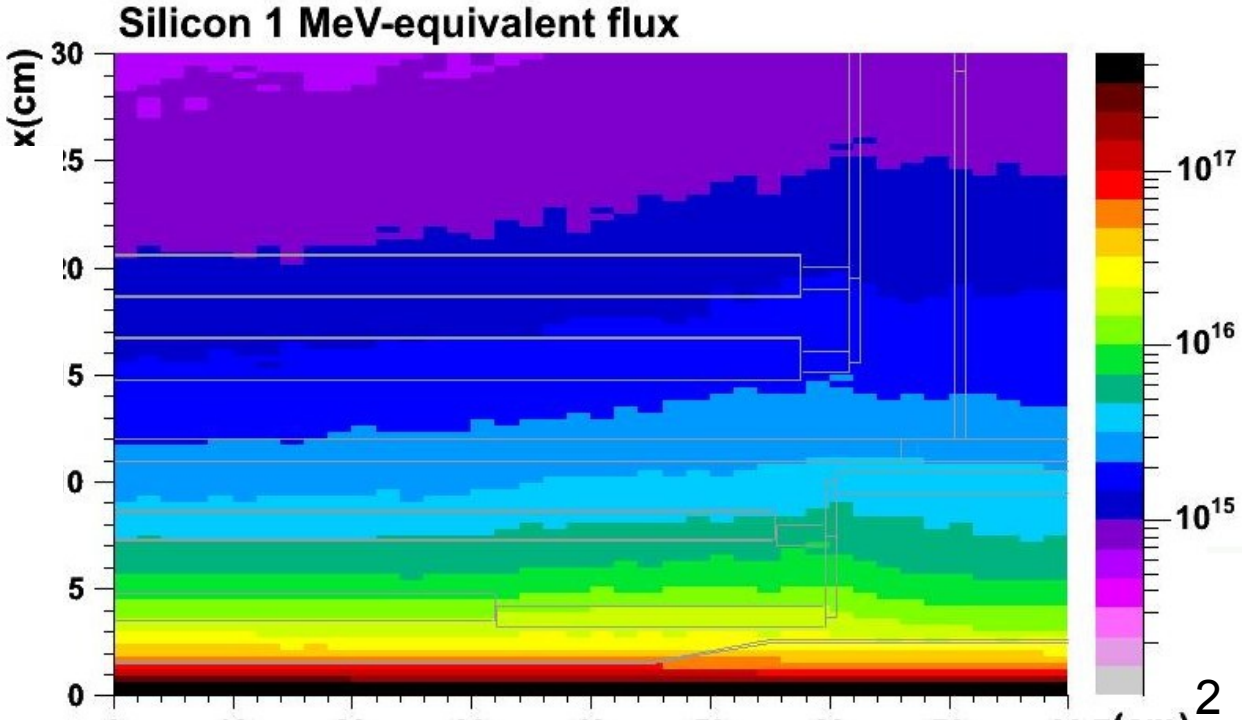
with lots of material from Ivan Peric (U Heidelberg)

Reminder: fluences at HL-LHC

- integrated luminosity: 3000 fb^{-1}
- including a safety factor of 2 to account for all uncertainties this yields for ATLAS:
  - at 5 cm radius:
    - ~$2 \cdot 10^{16}$ n_{eq} cm^{-2}
    - ~1500 MRad
  - at 25 cm radius
    - up to 10^{15} n_{eq} cm^{-2}
    - ~100 MRad
    - several m^2 of silicon







Active sensors

Implications

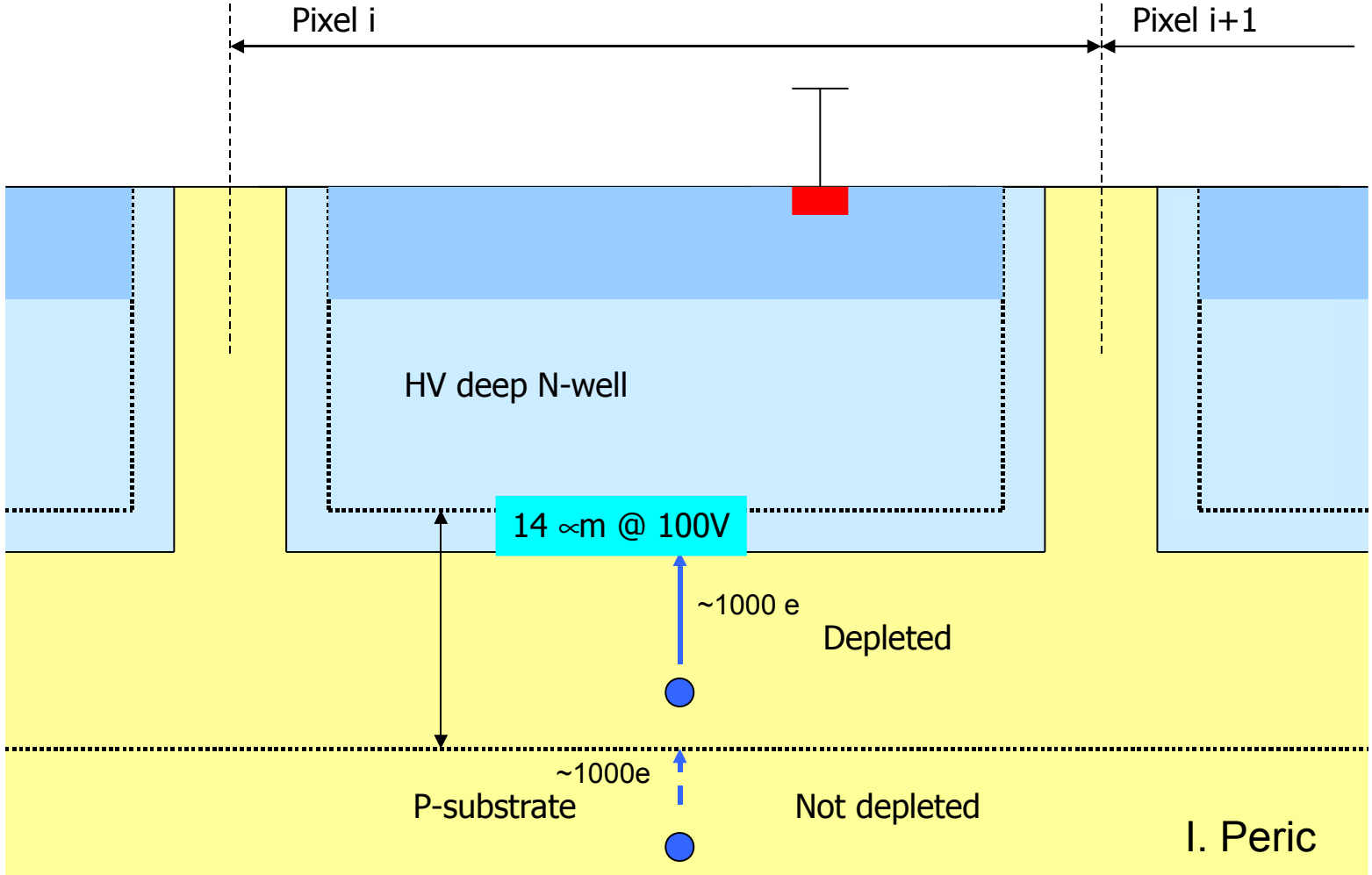
- High fluences: trapping dominant
  - reduce drift distance, increase field → reduce drift time:
    - 3D sensors
    - thin silicon
    - low depletion depth 'on purpose':
      - low(er) resistivity silicon
      - dedicated annealing to increase N_{eff}
- Large areas: low cost of prime importance
  - industrialised processes
  - large wafer sizes
  - cheap interconnection technologies
- Idea: explore industry standard CMOS processes as sensors
  - commercially available by variety of foundries
    - large volumes, more than one vendor possible
  - 8” to 12” wafers
    - low cost per area: “as cheap as chips”
  - (partially too) low resistivity p-type Cz silicon
    - thin active layer
    - wafer thinning possible

AMS H18 (and H35) HV-CMOS

- Project initiated and led by Ivan Peric (U Heidelberg)
- Austria Micro Systems offers HV-CMOS processes with 350 and 180 nm feature size, the latter one in cooperation with IBM
  - biasing of substrate to ~100V possible
  - substrate resistivity ~20 Ohm*cm → $N_{eff} > 10^{14}/cm^3$
    - radiation induced N_{eff} insignificant even for innermost layers
  - depletion depth in the order of 10-20 µm
  - on-sensor amplification possible - and necessary for good S/N
    - key: small pixel sizes → low capacitance → low noise
  - additional circuits possible, e.g. discriminator
    - beware of 'digital' crosstalk
  - full-sized radiation hard drift-based MAPS feasible, but challenging
    - aim for 'active sensors' in conjunction with rad-hard readout electronics first
- Scope of the talk:
  - Introduce the concept
  - Present first results with test chips
  - Details of a active sensor prototype currently being produced
  - Outlook: how small can pixels get?

A HV-CMOS sensor...

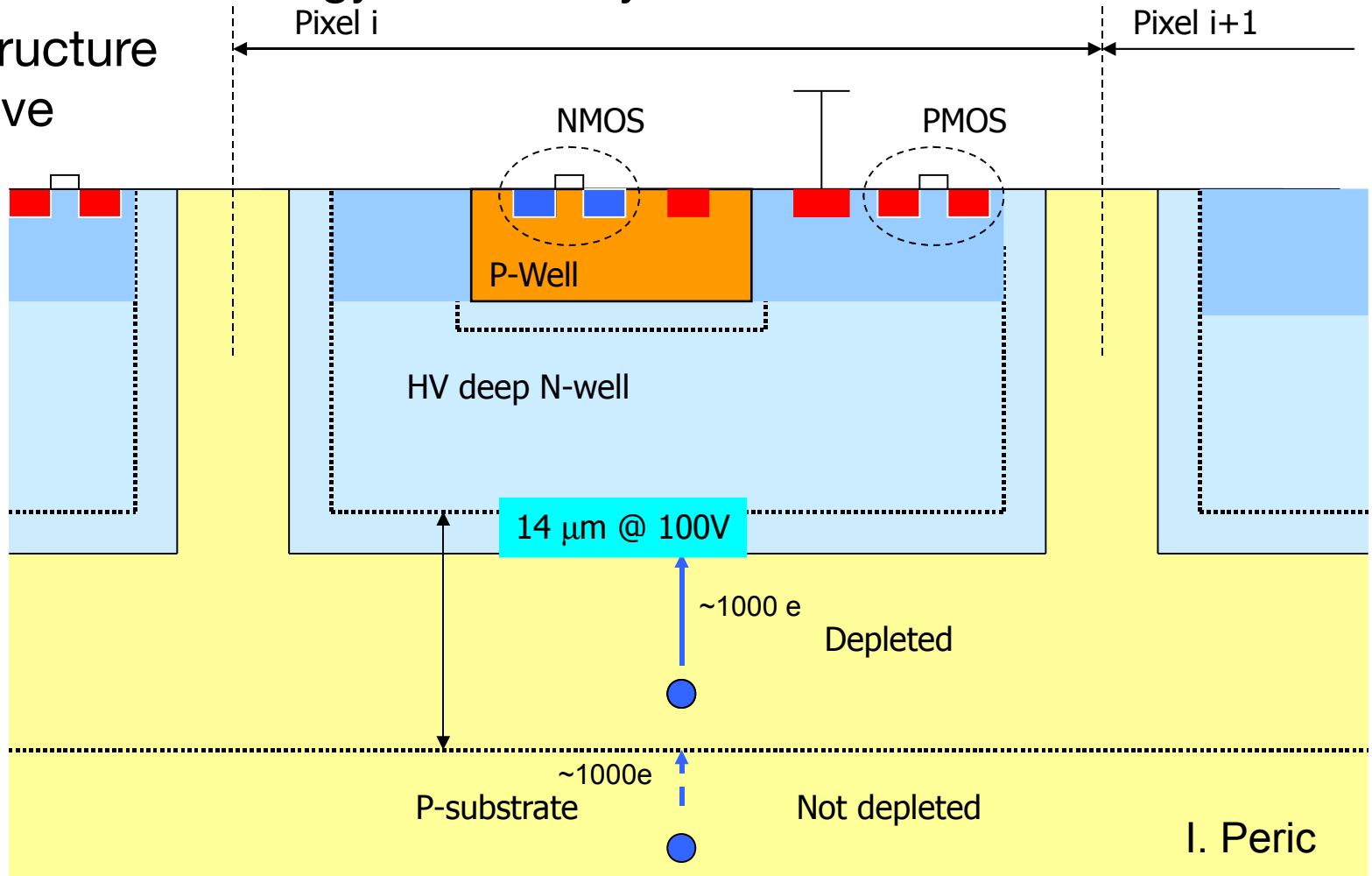
- essentially a standard n-in-p sensor
- depletion zone 10-20 µm: signal in the order of 1-2ke$^-$
  - challenging for hybrid pixel readout electronics
    - new ATLAS ROC FE-I4 might be able to reach this region – but no margin



The depleted high-voltage diode used as sensor (n-well in p-substrate diode)

...including active circuits: *smart diode array (SDA)*

- implementation of
  - first amplifier stages
  - additional cuircuits: discriminators, impedance converters, logic, …
- deep sub-micron technology intrinsically rad-hard
- triple-well structure would improve crosstalk-tolerance



CMOS electronics placed inside the diode (inside the n-well)

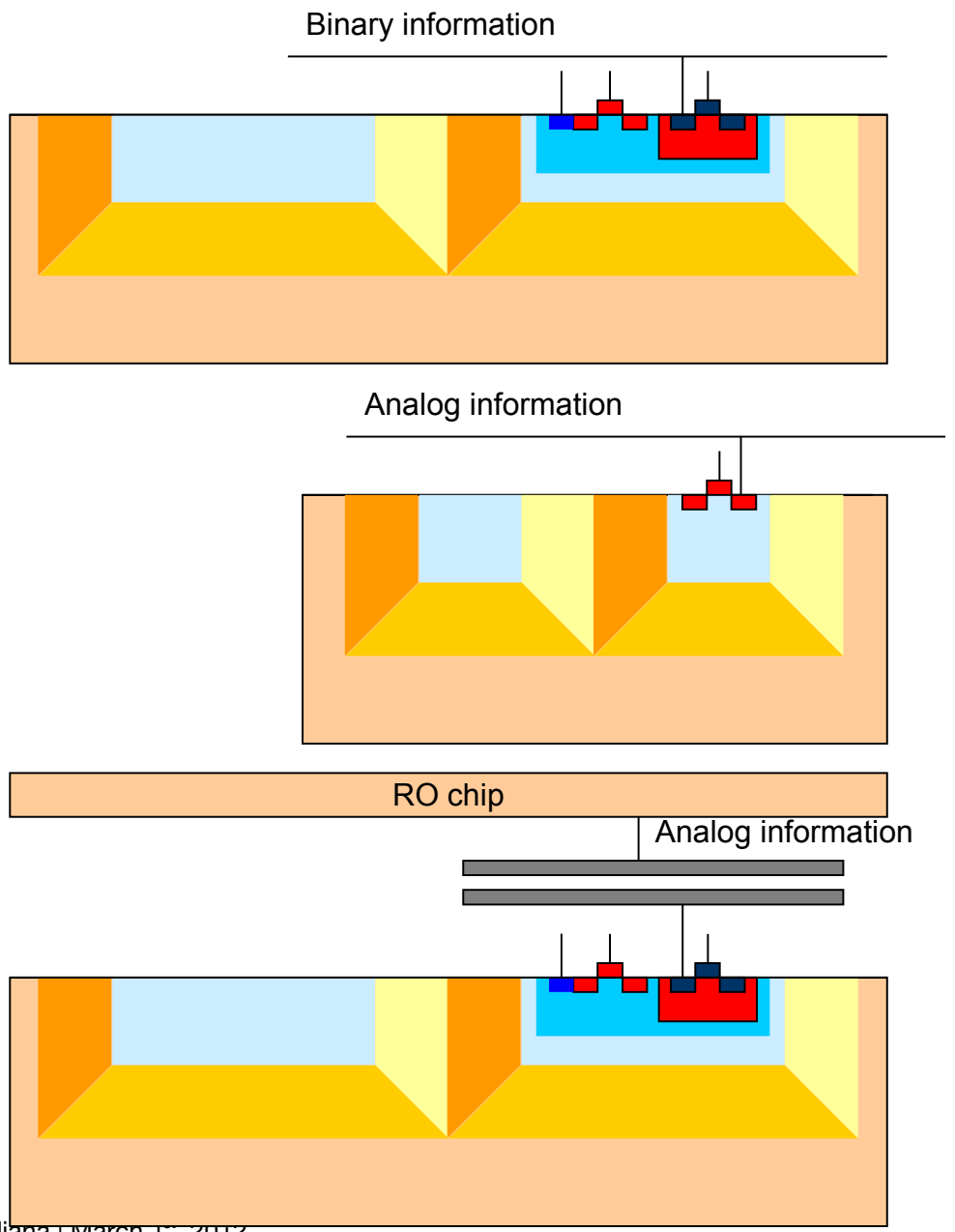
Prototypes

- Several test-chips submitted in both technologies already

SDA with sparse readout
("intelligent" CMOS pixels)
HV2/MuPixel chip

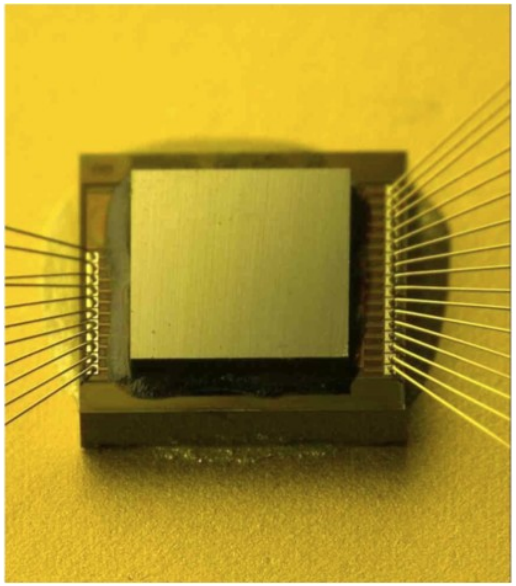
SDA with frame readout
(simple PMOS pixels)
HVM chip

SDA with capacitive readout
("intelligent" pixels)
Capacitive coupled pixel
detectors
CCPD1 and CCPD2 detectors



Prototype summaries

First chip – CMOS pixels
Hit detection in pixels
Binary RO
Pixel size 55x55µm
Noise: 60e
MIP seed pixel signal 1800 e
Time resolution 200ns

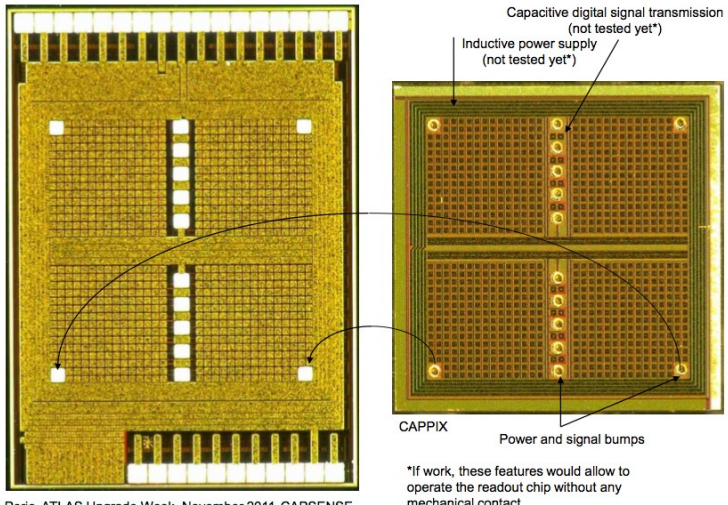


Bumpless hybrid detector

CCPD1 Chip
Bumpless hybrid detector
Based on capacitive chip to chip signal transfer
Pixel size 78x60µm
RO type: capacitive
Noise: 80e
MIP signal 1800e

CCPD2 Chip
Edgeless CCPD
Pixel size 50x50µm
Noise: 30-40e
Time resolution 300ns
SNR 45-60

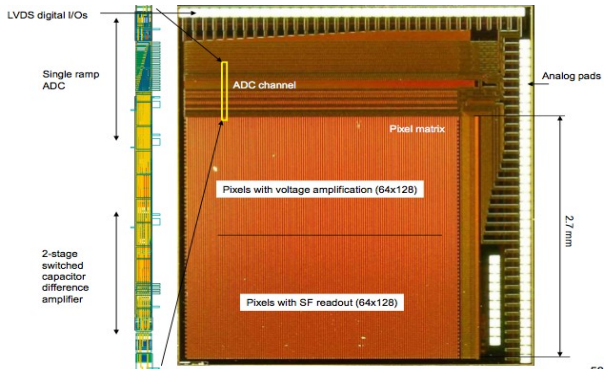
Irradiations of test pixels
60MRad – SNR 22 at 10C (CCPD1)
$10^{15} n_{eq}/cm^2$ – SNR 50 at 10C (CCPD2)



Frame readout - monolithic

PM1 Chip
Pixel size 21x21µm
Frame mode readout
4 PMOS pixel electronics
128 on chip ADCs
Noise: 90e
Test-beam: MIP signal 2200e/1300e
Efficiency > 85% (timing problem)
Spatial resolution 7µm
Uniform detection

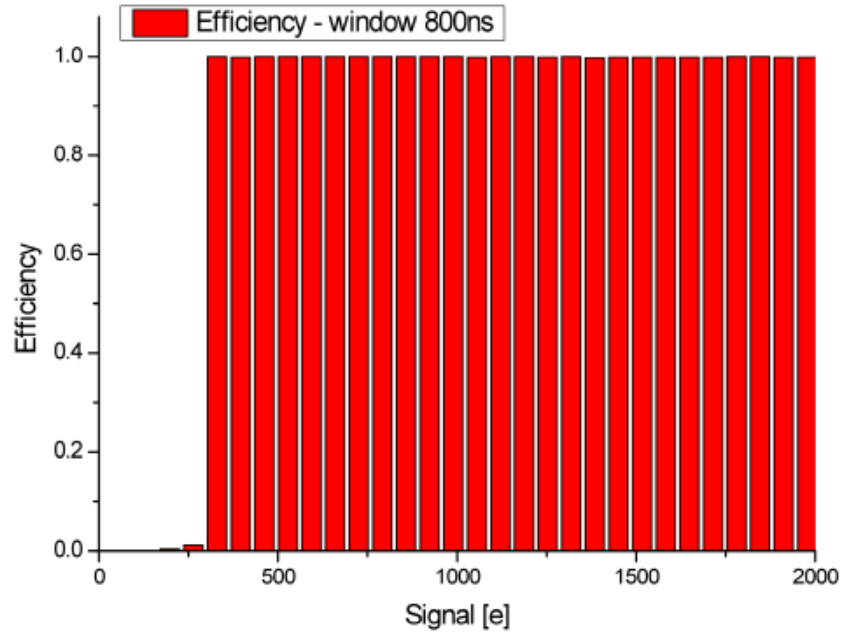
PM2 Chip
Noise: 21e (lab) - 44e (test beam)
Test beam: Detection efficiency 98%
Seed Pixel SNR ~ 27
Cluster Signal/Seed Pixel Noise ~ 47
Spatial resolution ~ 3.8 ∝m

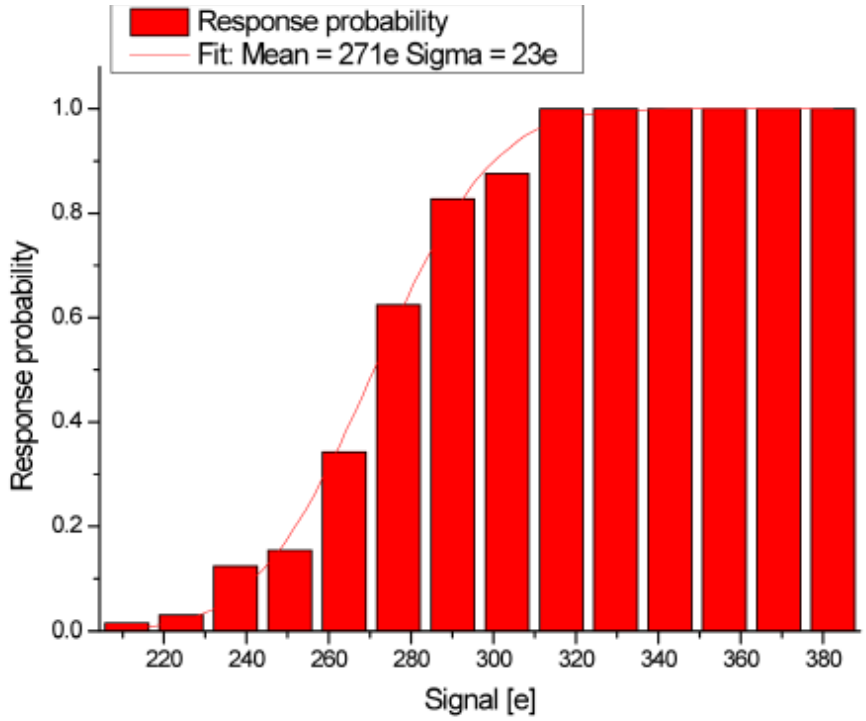


Active sensors

CCPD thresholds

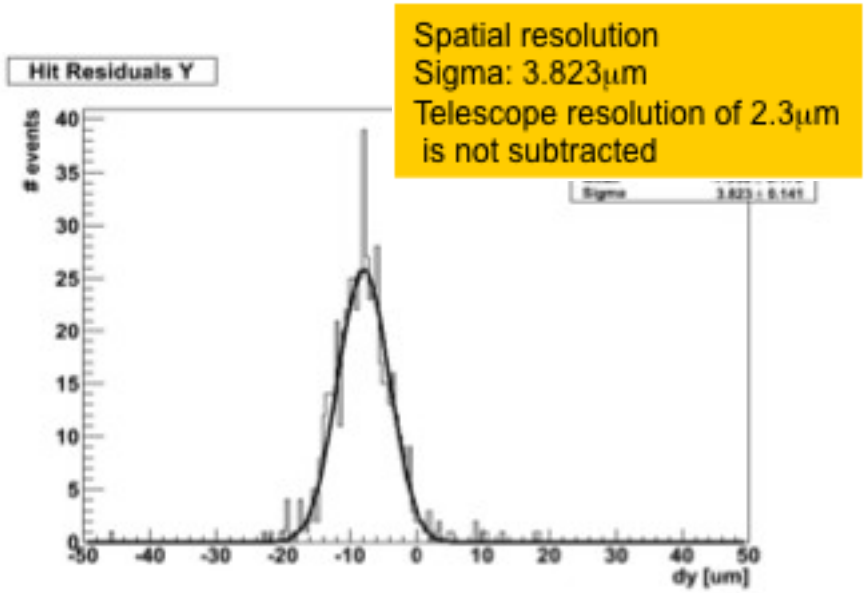
- threshold set to about 300 electrons
- noise extracted from s-curve about 23 electrons (!)

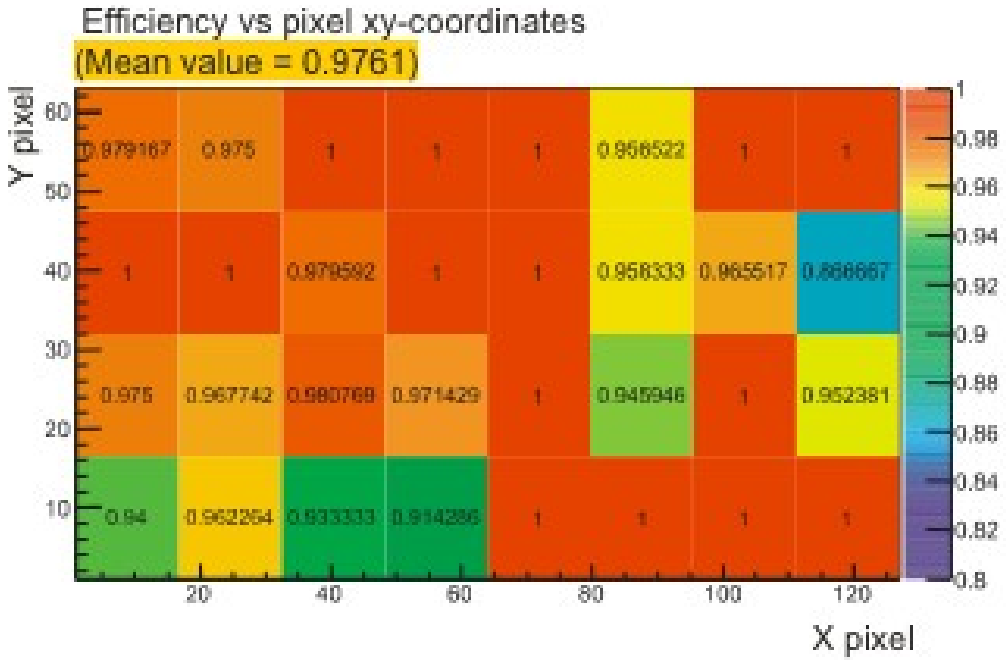


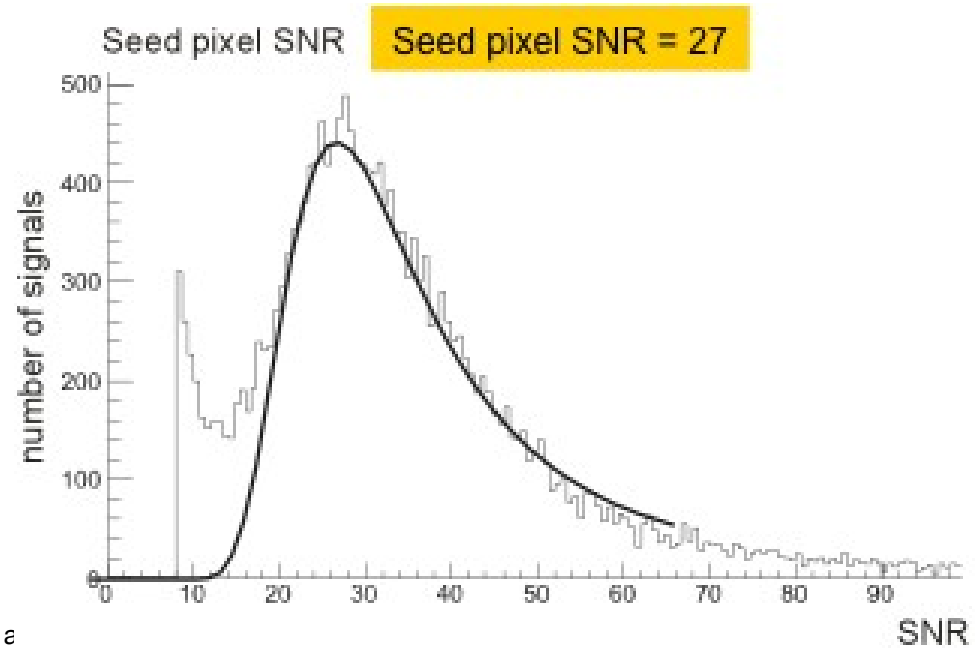


Test beam results

- excellent resolution
- very good S/N ratio
- efficiency limited by readout artifacts:
  - column-based readout
  - column not active during readout
  - data analysis did not correct for this
  - very small chip → low statistics

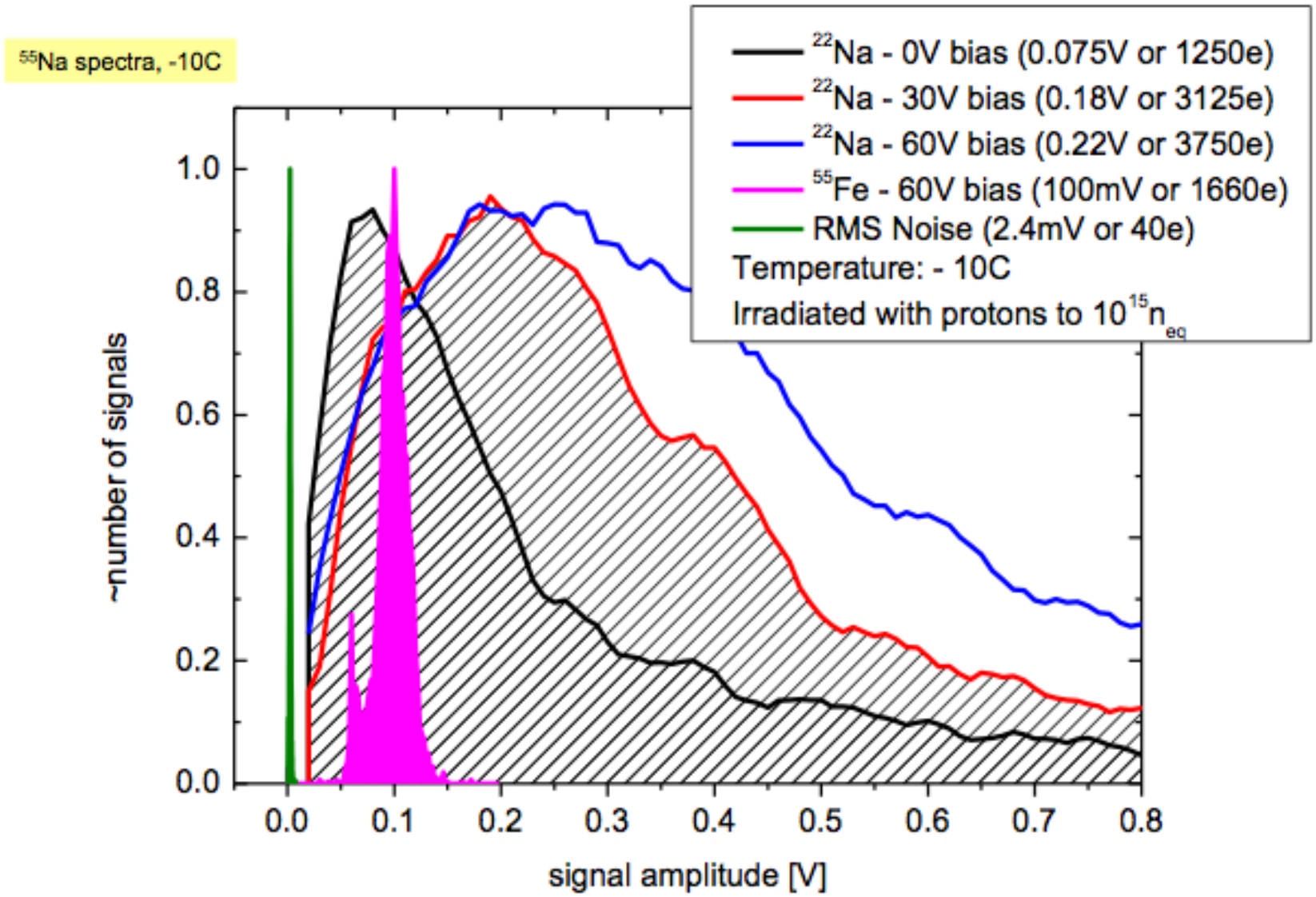






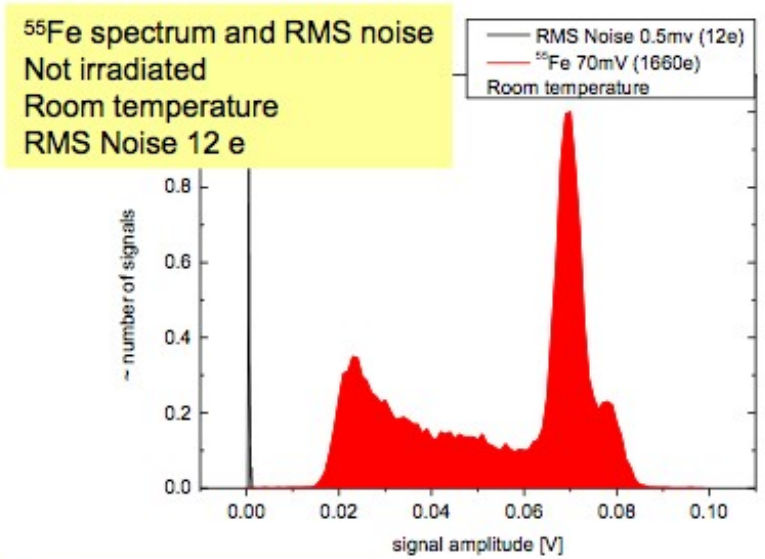
Some irradiated prototype results

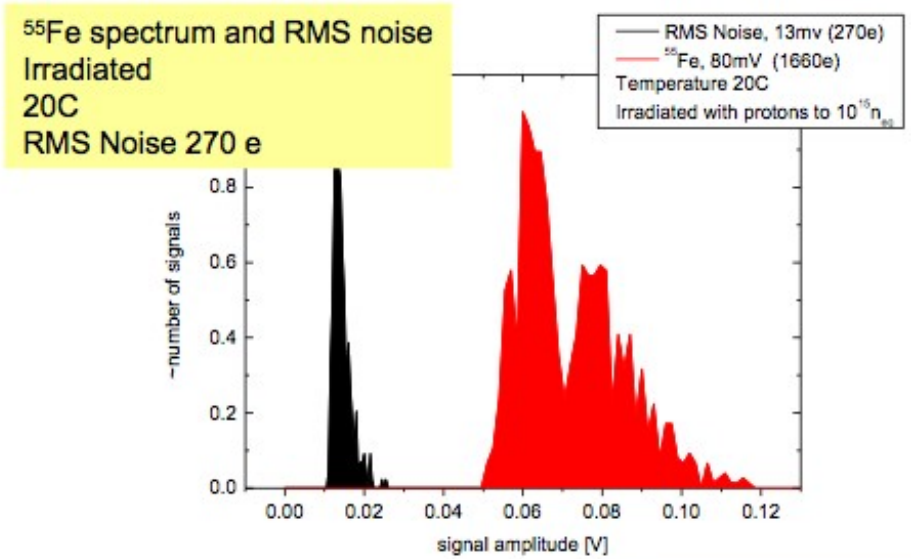
- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- generally very good S/N ratio

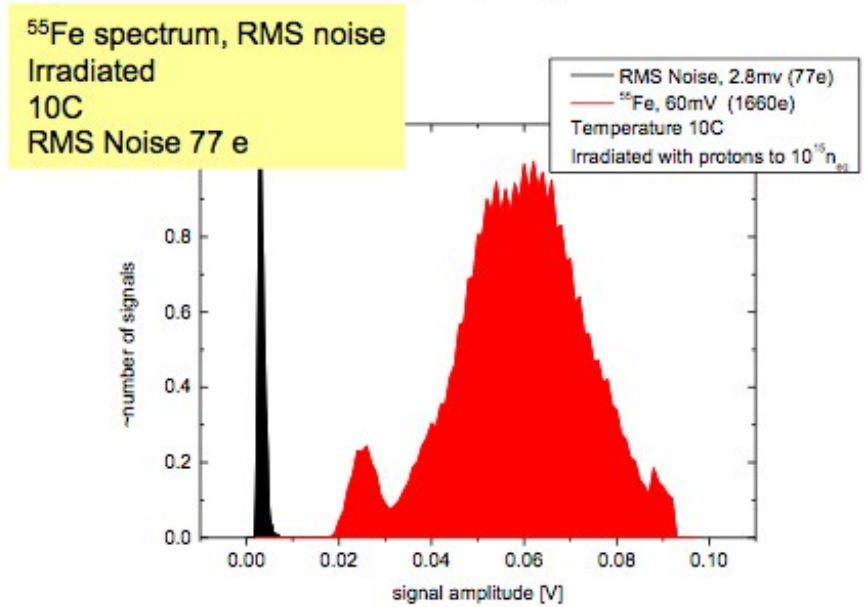


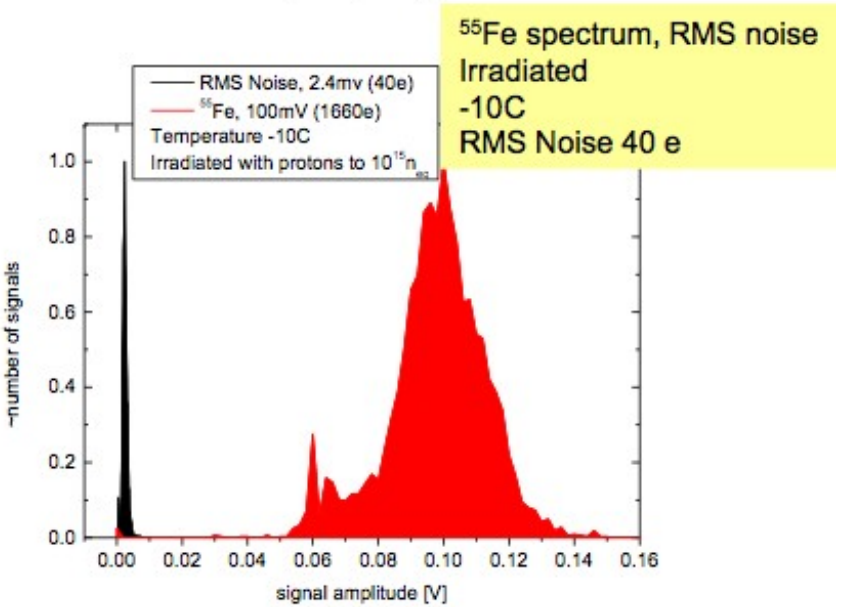
Some irradiated prototype results

- Irradiation with 23 MeV protons: 1e15 neq/cm2, 150MRad
- FE-55 performance recovers after slight cooling



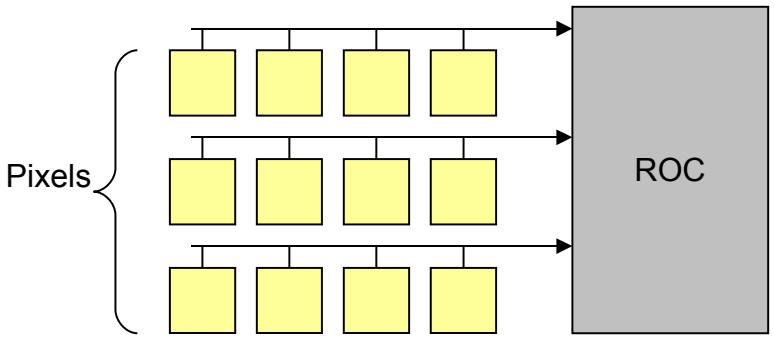






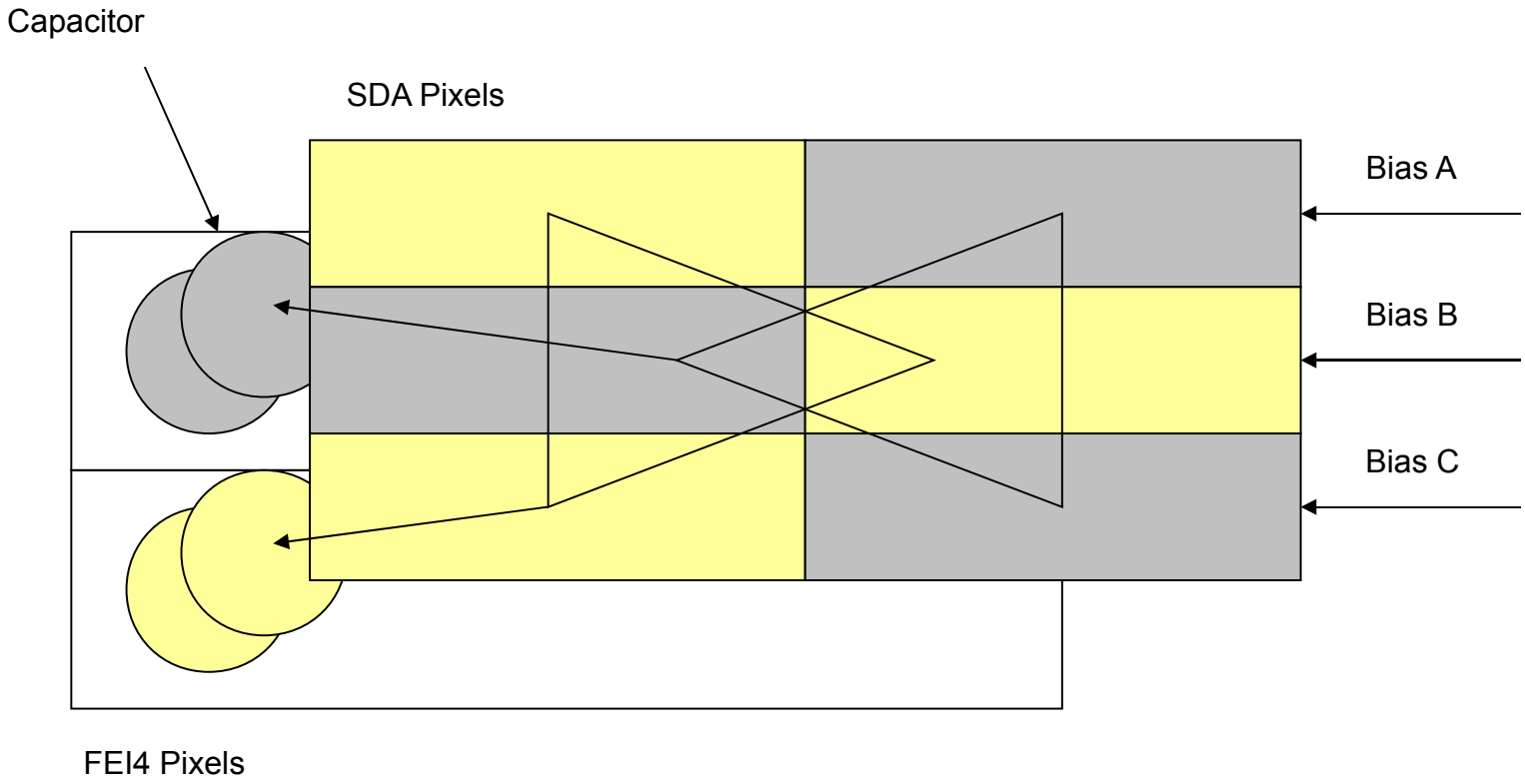
From MAPS to active sensors

- Existing prototypes would not suitable for HL-LHC, mainly because
  - readout too slow
  - time resolution not compatible with 40 MHz operation
  - high-speed digital circuits might affect noise performance
- Idea: use HV-CMOS as sensor in combination with existing readout technology
  - fully transparent, can be easily compared to other sensors
  - can be combined with several readout chips
  - makes use of highly optimised readout circuits
  - can be seen as first step towards a sensor being integrated into a 3D-stacked readout chip (not only analogue circuits but also charge collection)
- Basic building blocks: *small* pixels (low capacitance, low noise)
  - can be connected in any conceivable way to match existing readout granularity, e.g.
    - (larger) pixels
    - strips



Pixels

- Possible/sensible pixel sizes: 20x20 to 50x125 µm
  - 50x250 µm (current ATLAS FE-I4 chip) too large
  - combine several sensor “sub-pixels” to one ROC-pixel
    - sub-Pixels encode their address/position into the signal as pulse-height-information instead of signal proportional to collected charge
    - routing on chip is well possible, also non-neighbour sub-pixels could be combined and more than one combination is possible



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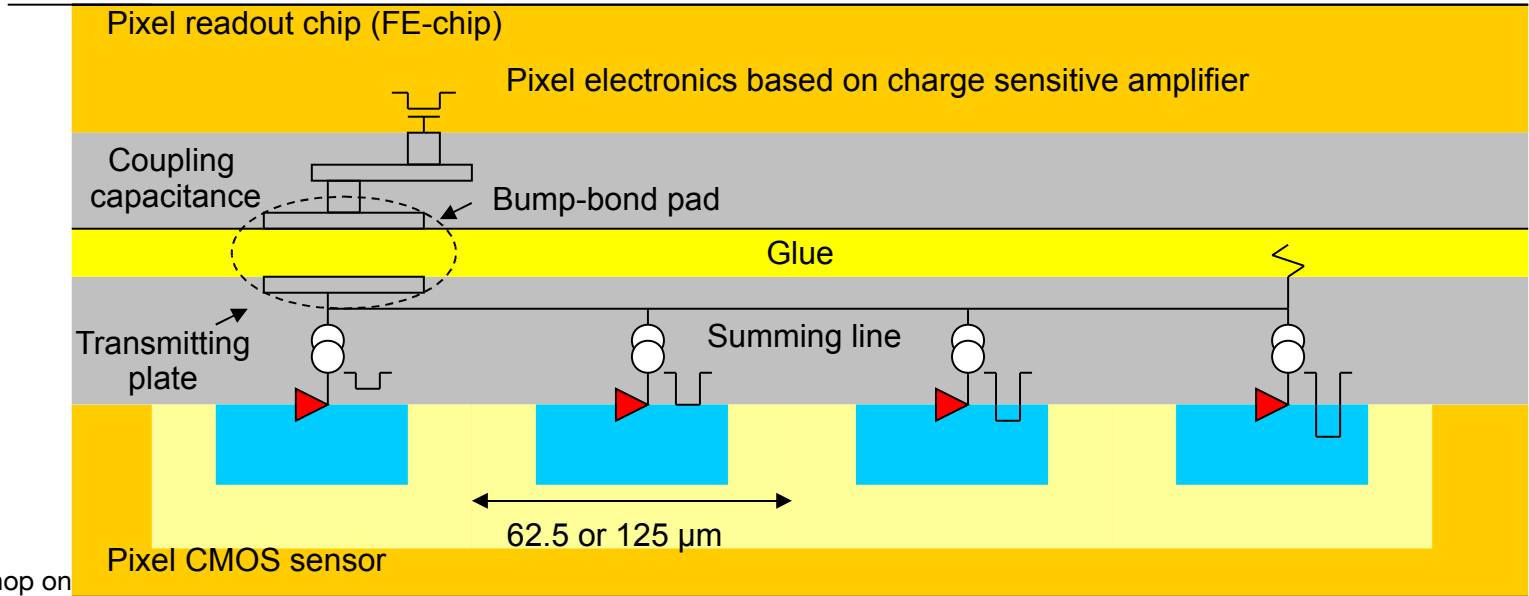
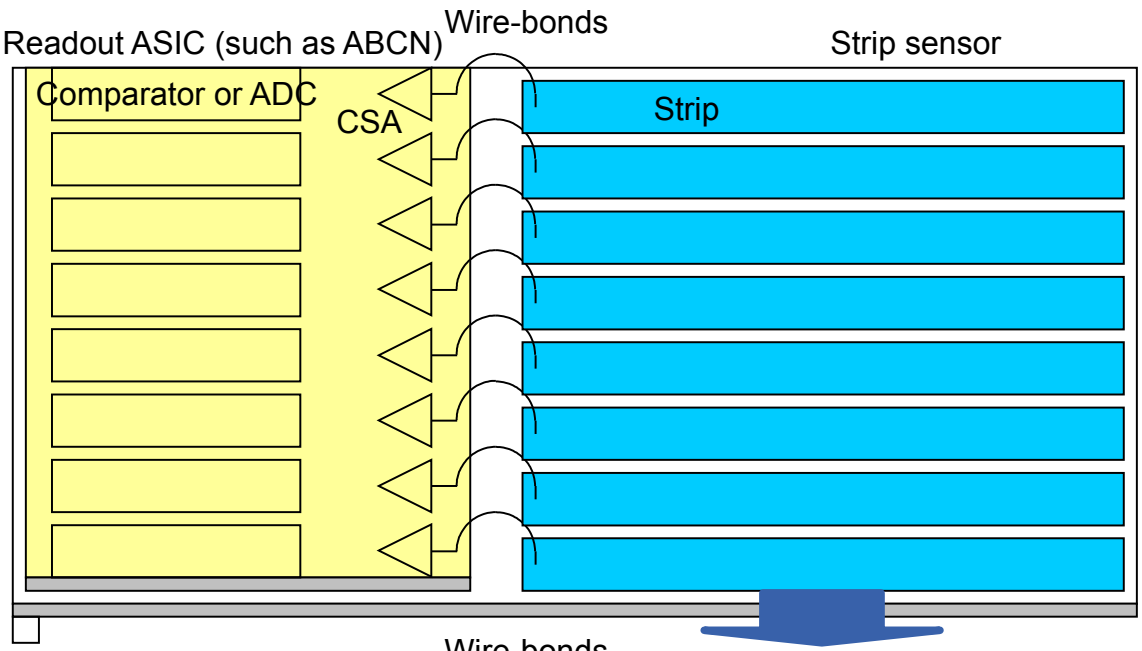
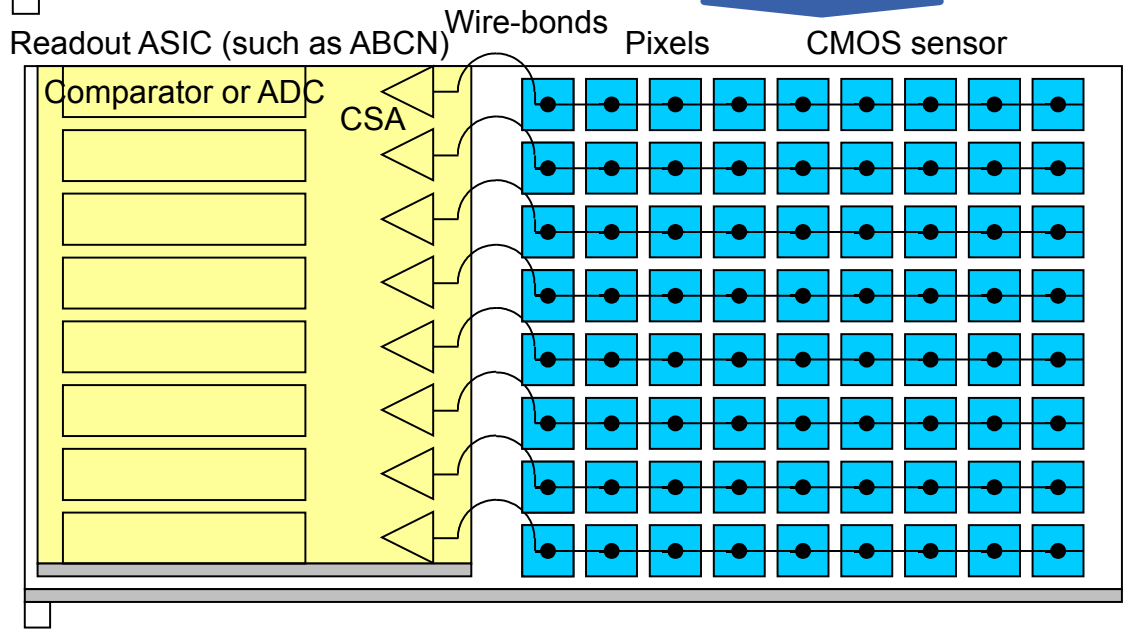
- Only reason not to use AC coupling with pixel sensors up to now was small coupling capacitance in association with low signal
  - amplification possible, hence AC transmission not a problem at all
  - would allow to get rid of costly bump-bonding

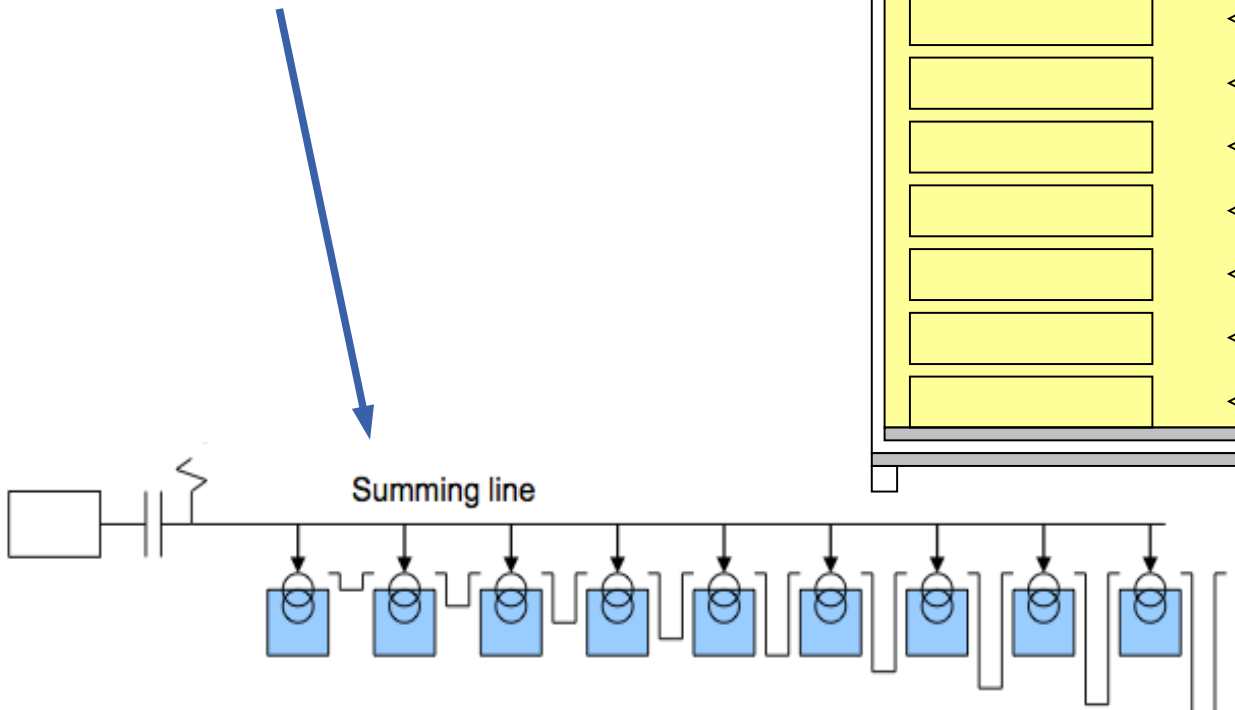


Strips

- Easiest idea would be to simply sum all pixels within a virtual strip
- Hit position along the strip could be again encoded by pulse height for analogue readout chips (e.g. Beetle)

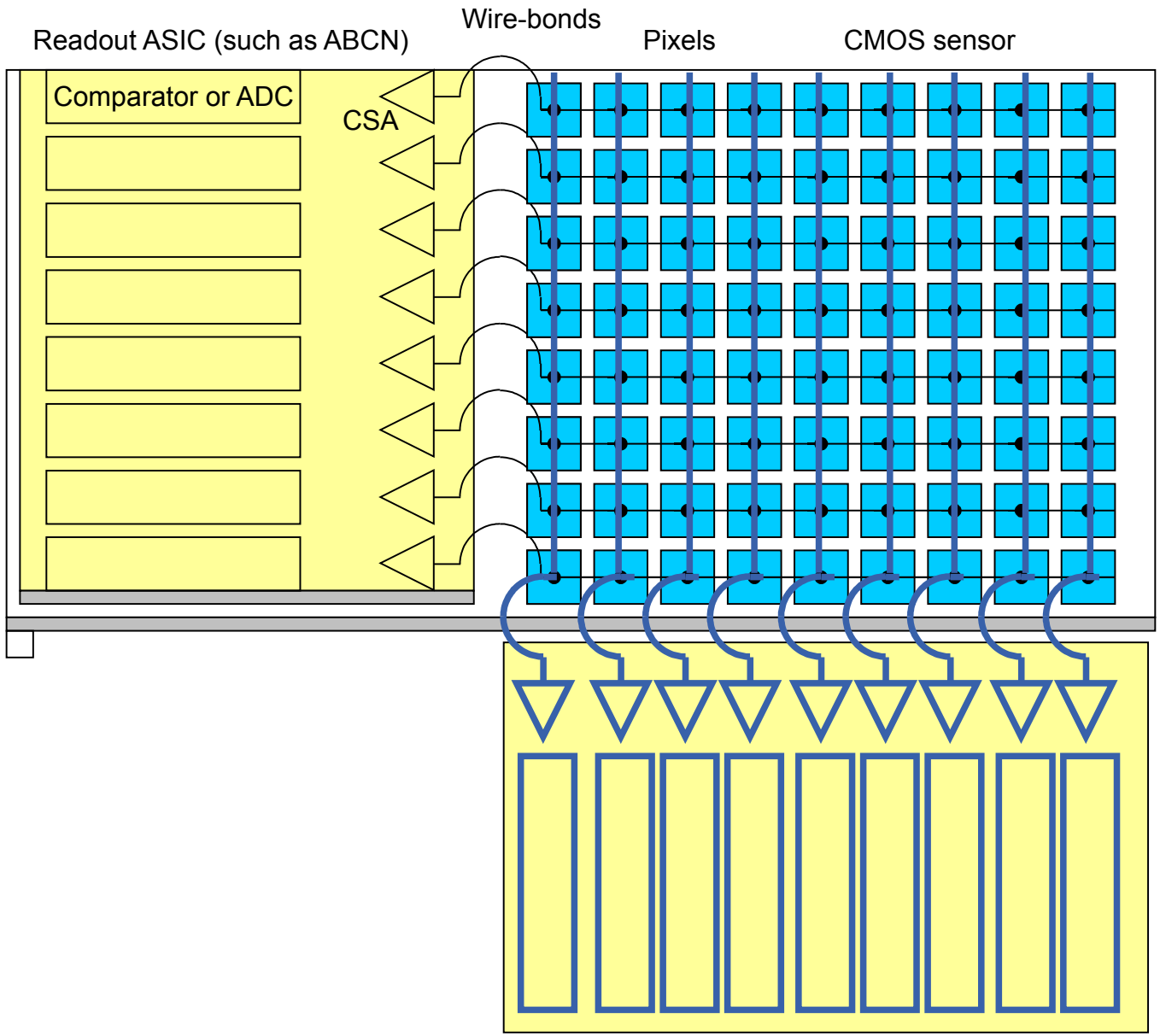






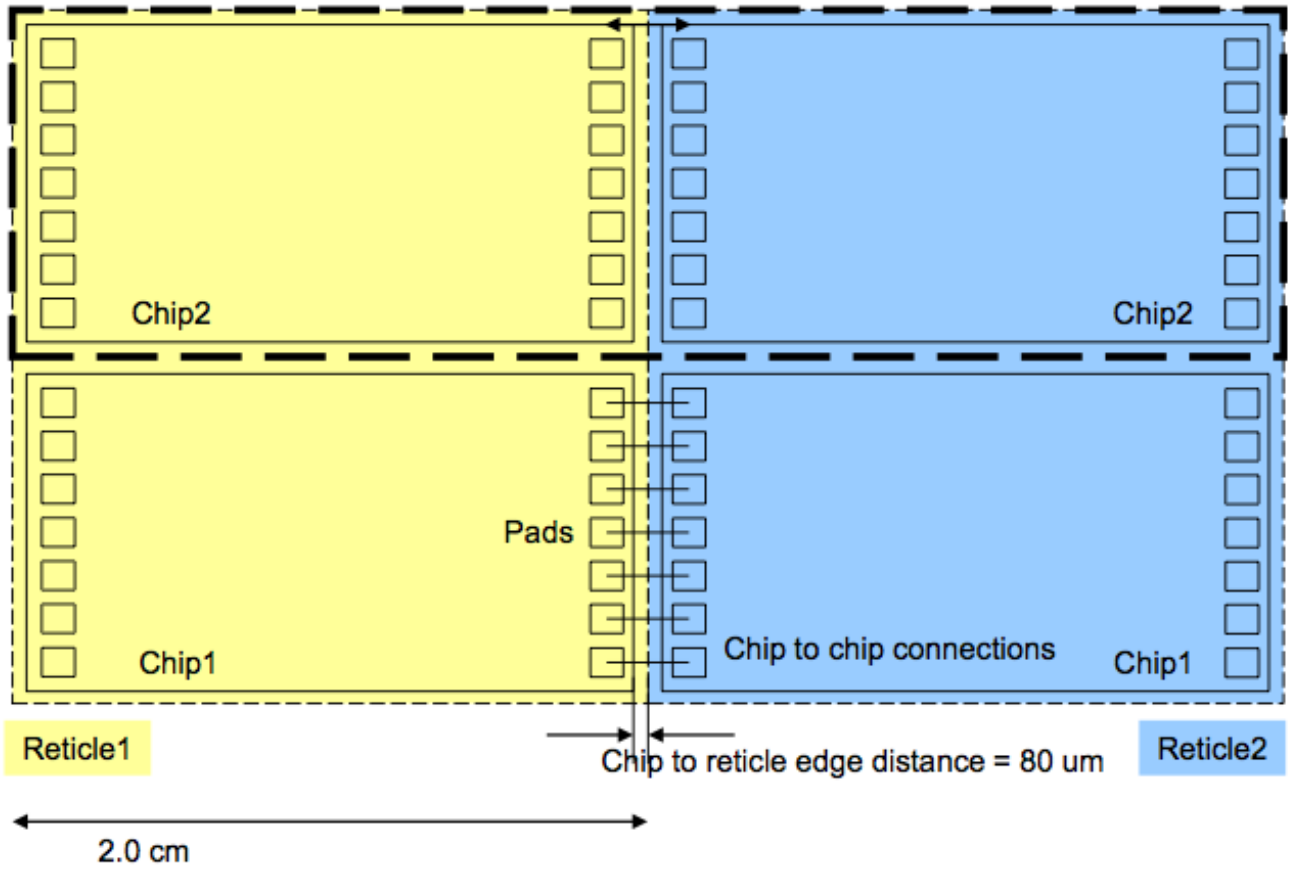
Strips

- Signals are digital so multiple connections are possible, e.g.
  - “crossed strips”
  - strips with double width but only half the pitch in r-phi



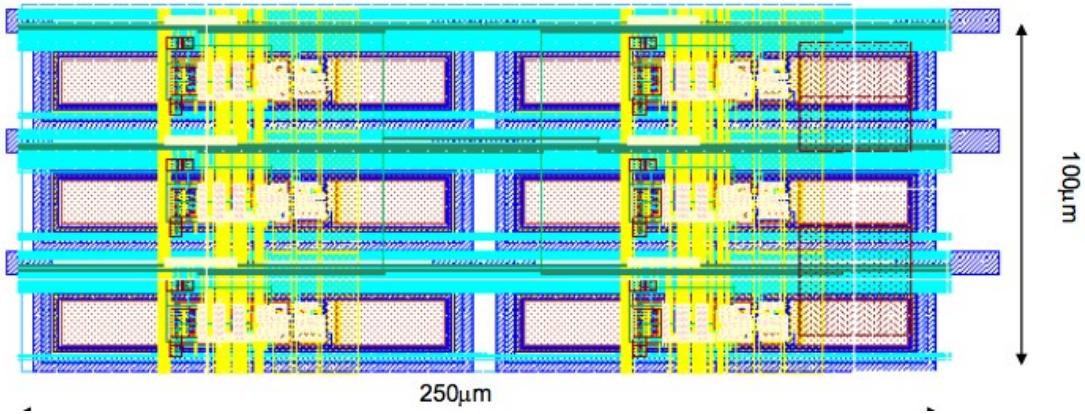
Reticule size/stitching

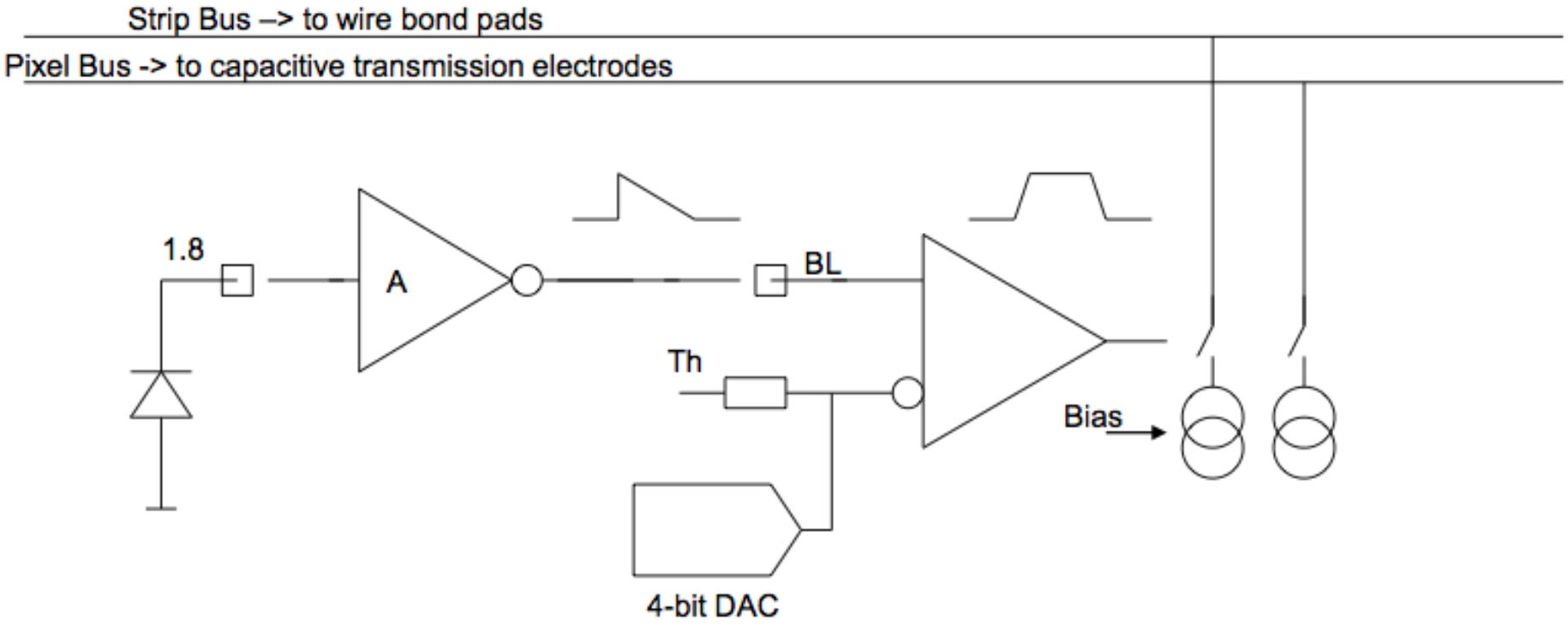
- Sensor size is currently limited by reticule size of ~2x2 cm
  - however, the yield should be excellent (very simple circuit, essentially no “central” parts) so it might be interesting to cut large arrays of sensors from a wafer and connect individual reticules by
    - wire-bonding
    - post-processing (one metal layer, large feature size)
- There are HV-CMOS processes/foundries which allow for stitching
- Very slim dicing streets
  - Gaps between 1-chip modules could be rather narrow



HV2FEI4

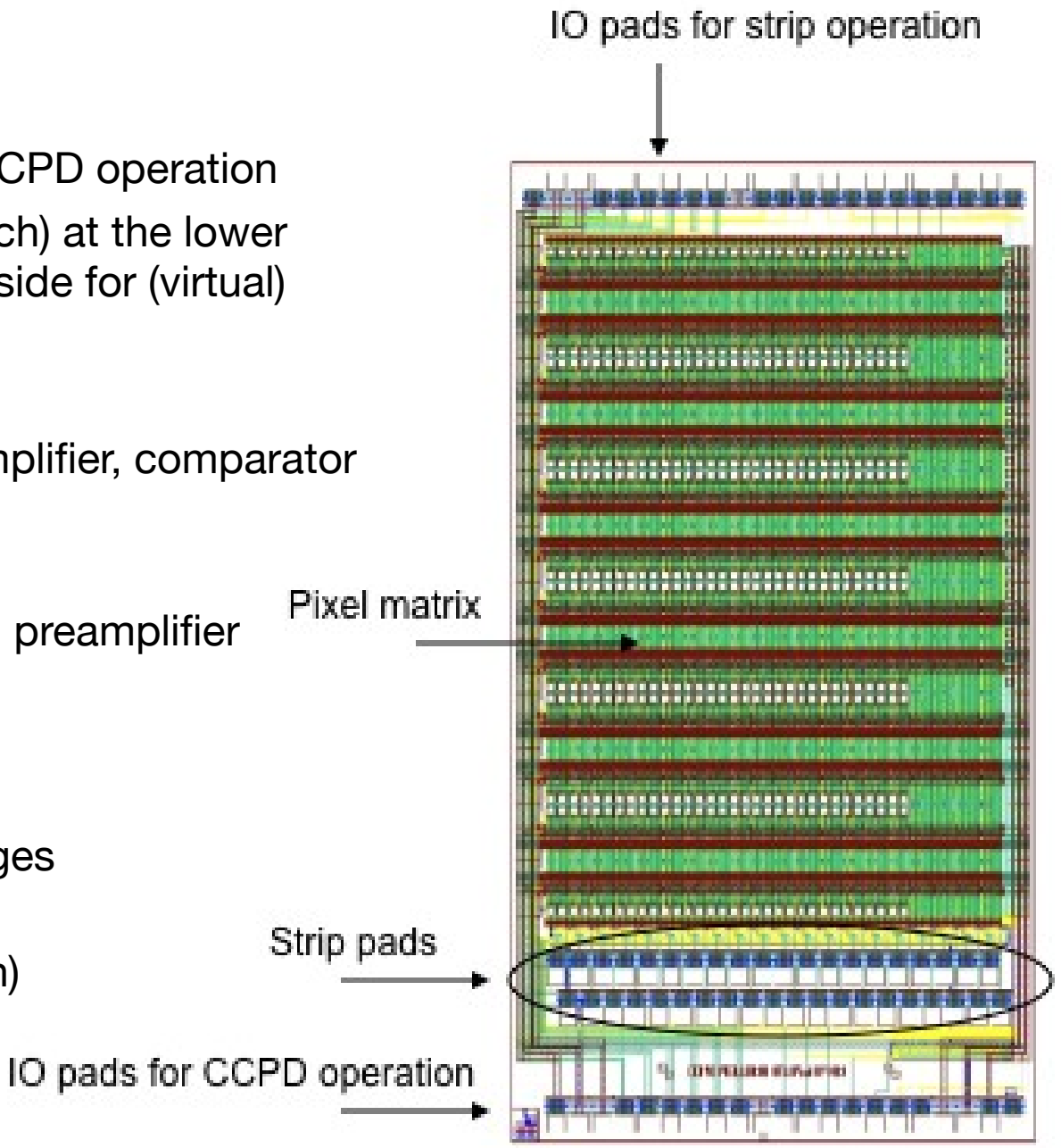
- ATLAS institutes submitted a combined active strip/pixel sensor
  - pixels match new ATLAS FE-I4 readout chip
    - capacitive coupling
    - bump-bonding possible
  - strips should be compatible with ATLAS ABCN and LHCb/Alibava Beetle
  - chip expected ~end of March





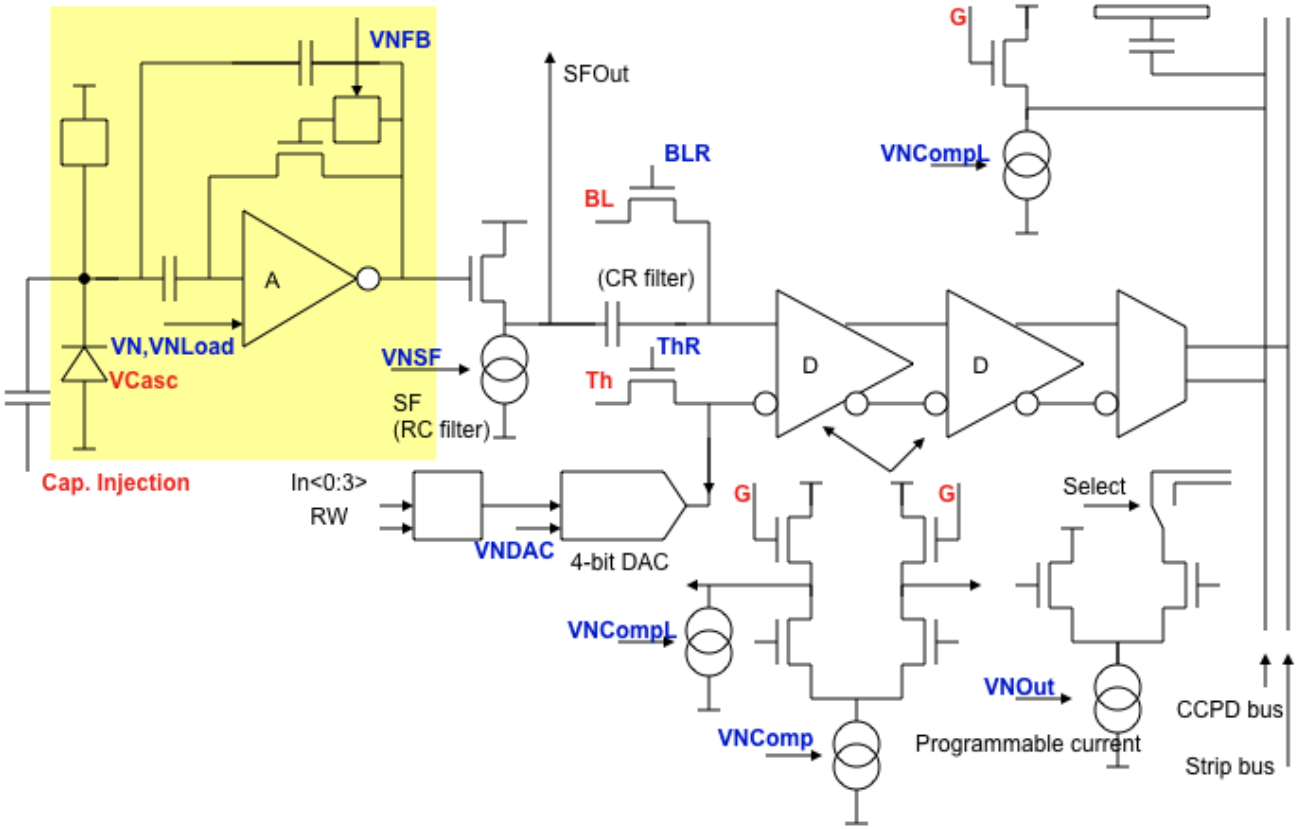
HV2FEI4

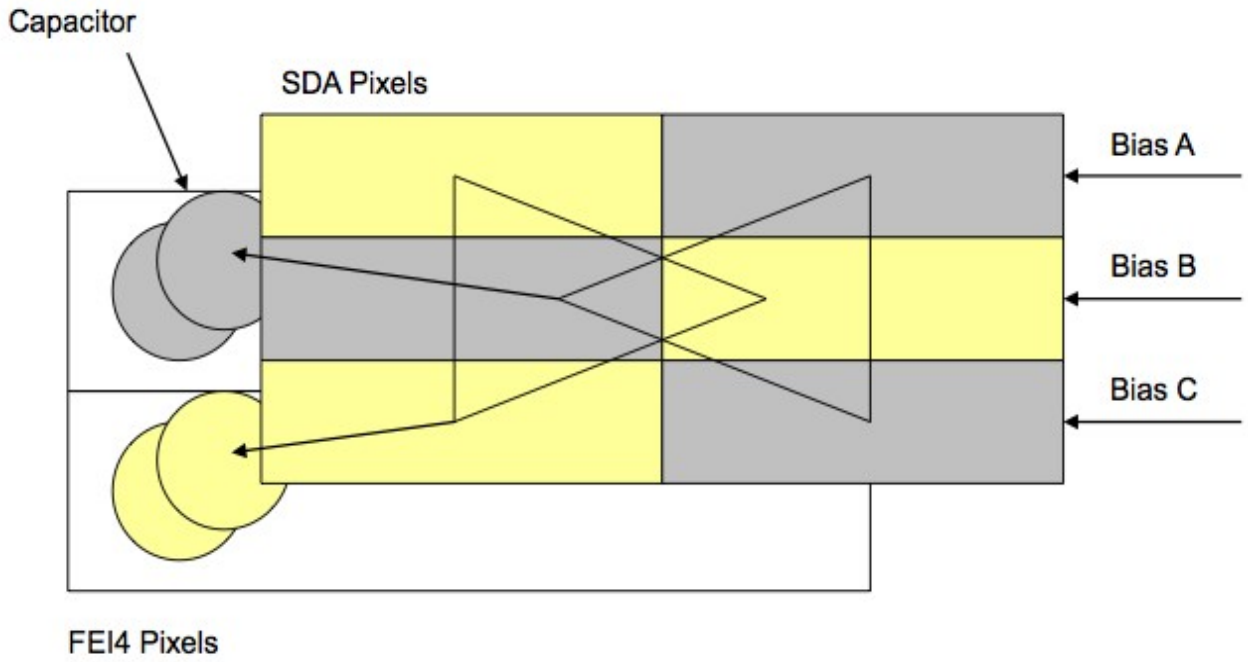
- Chip size: 2.2mm x 4.4mm
- Pixel matrix: 60x24 pixels
- Pixel size 33 µm x 125 µm
- 21 IO pads at the lower side for CCPD operation
- 40 strip-readout pads (100 µm pitch) at the lower side and 22 IO pads at the upper side for (virtual) strip operation
- On chip bias DACs
- Pixels contain charge sensitive amplifier, comparator and tune DAC
- Pads include:
  - Analog power (vdda 1.8V) and preamplifier supply 1.2V
  - Digital power (1.8V)
  - HV bias (-60V)
  - Threshold and base line voltages
  - Slow control for DACs
  - Test pulse (capacitive injection)



HV2FEI4

- Sub-pixel positions are encoded by 3-level pulses
  - additive: unique pulse heights for all pixel combinations
  - FE-I4's 4-bit ToT should be able to disentangle

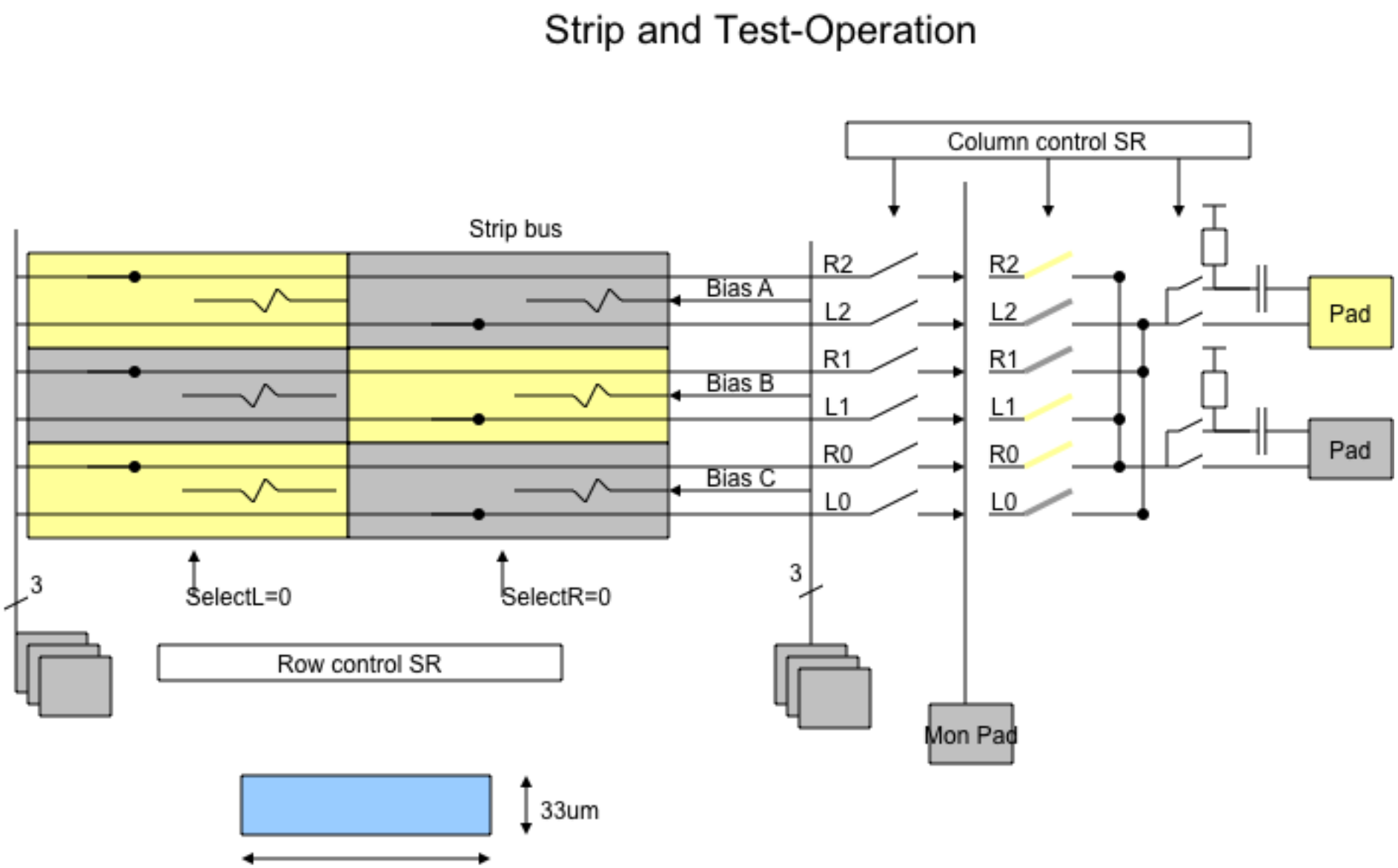




Active sensors

HV2FEI4

- Strips readout: z-position encoding via resistor network
- r-phi encoding just “proof of concept” not yet really useful



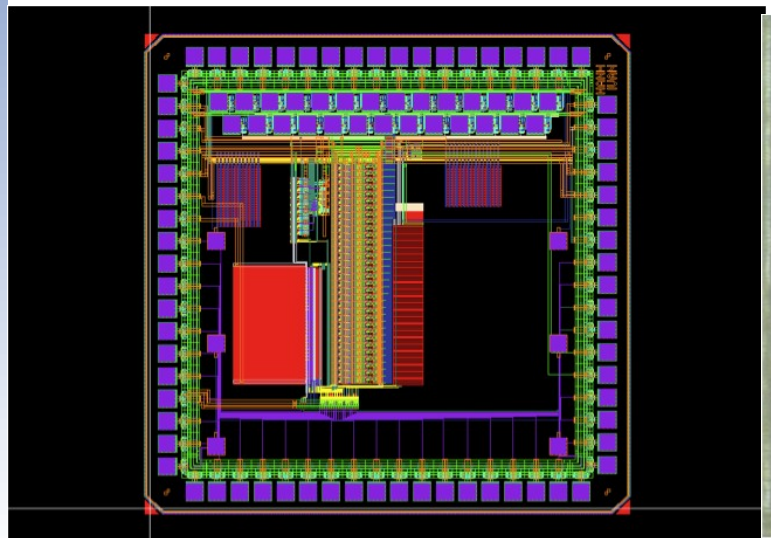
Outlook: back to MAPS?

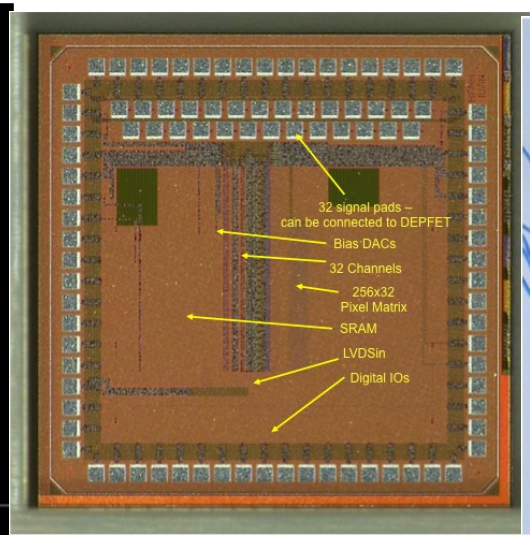
- 3 aspects for further improvement:
  - reduce pixel sizes further – how far can one go?
  - reduce thickness of “module” to save radiation length
  - reduce cost for large scale usage of a system with pixel-resolution

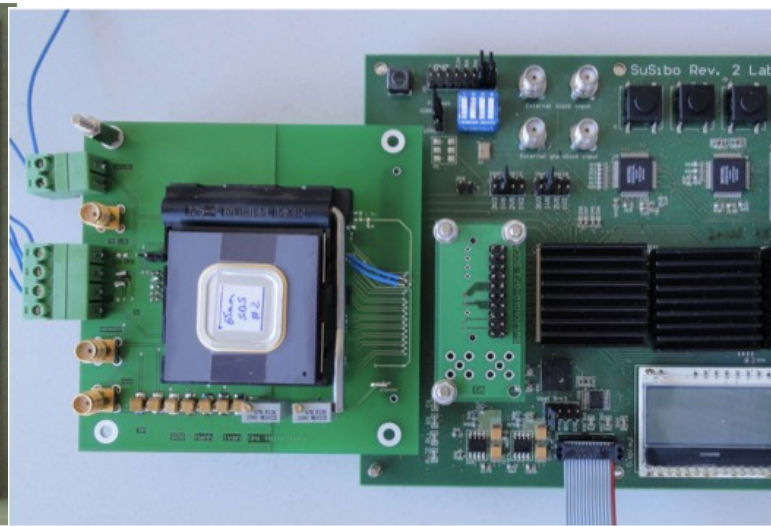
- smaller pixel sizes
  - go to smaller feature size
    - digital part directly scales
    - analogue part at least partially
  - lower capacitance
    - even lower noise
    - less preamp-power (but of course more channels)
  - interconnect
    - no bump-bonding for pixels in the order of 10x10 µm (maybe SLID)
    - capacitive coupling, but also here very dense
    - go to 3D interconnect? Maybe even 180nm HV-CMOS to 130nm CMOS?
    - go towards drift-based MAPS? In the end it's all a CMOS flavour...

CMOS MAPS

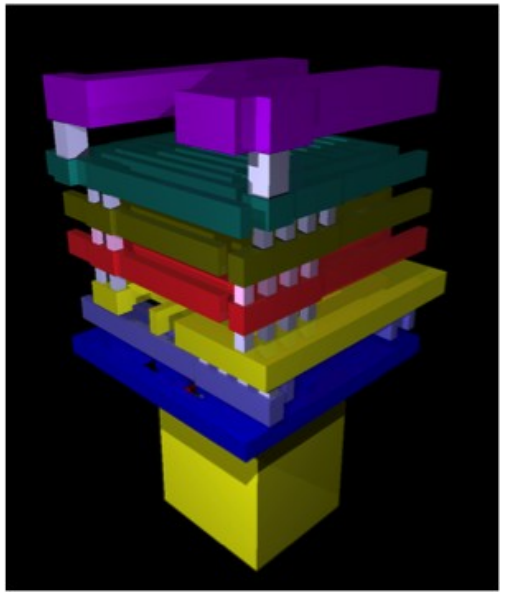
- What feature size/pixel size should be used?
  - test chips in 350 and 180nm HV-CMOS had different pixel sizes and varying levels of intelligence, but were generally not fast enough/did not have time stamps with 40 MHz
  - FE-I4 in 130nm has a cell size of 50x250 um → probably too large
  - 65nm aimed for by several chip developers within ATLAS
    - suitable as sensor/MAPS?
- 65nm process features
  - 20 Ohm*cm resistivity (!)
  - deep n-wells (not as deep as in HV processes, but might do)
  - work on 65nm chips has anyway started within ATLAS → synergy
  - first test chip containing tiny pixels (standard n-well) already done:



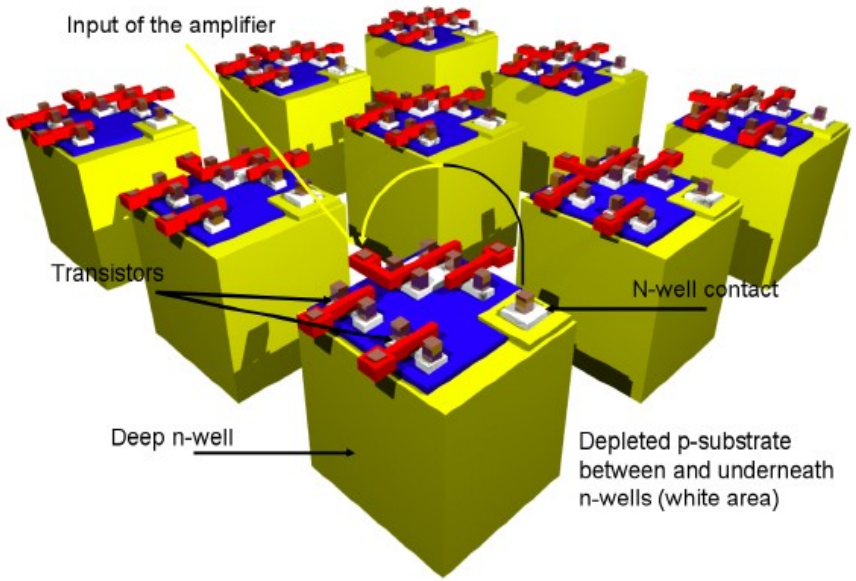


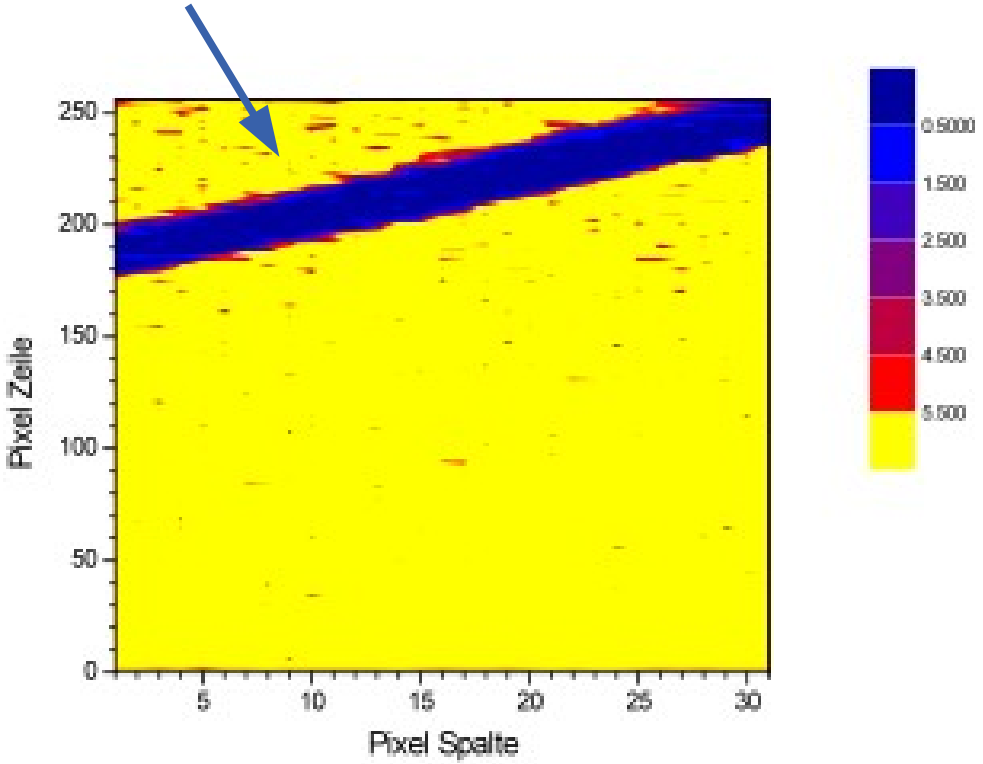


65nm test chip



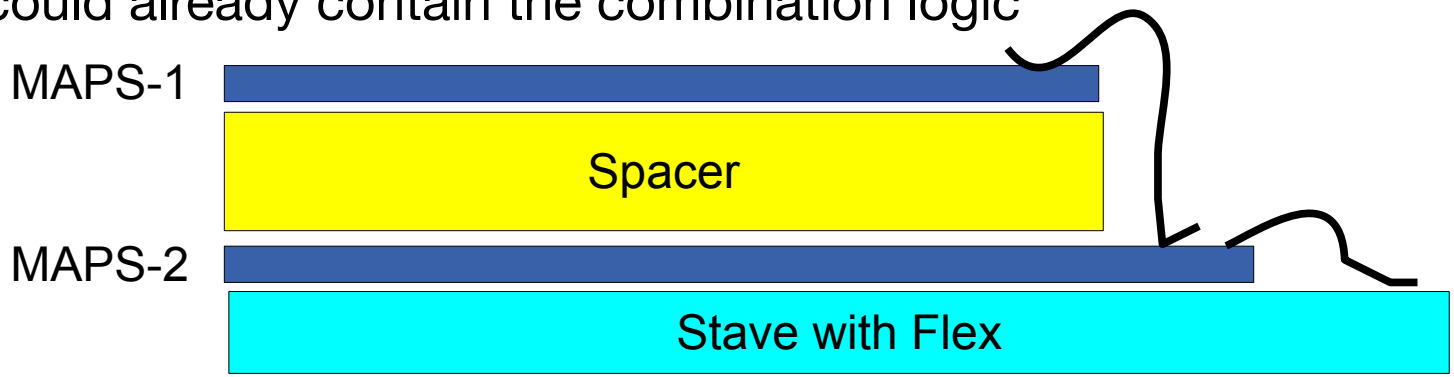
- Tiny pixels (2.5 µm pitch) with charge storage read-out sequentially
  - obviously not for HL-LHC, but 2.5 µm shows what is possible
  - 1 µm gaps between pixels, ~1V bias voltage (!)
  - minimal charge sharing due to very shallow depetion zone: Na-22 clusters are 2-3 pixels
  - spatial resolution (~binary) of 2.5µm/√12=0.7µm (!!)
  - shadow of a 16 µm thick golden bond-wire





Realistically – what is desirable?

- resolution of tracks in dense jets would be highly welcome for various reasons
  - very thin depletion zone would help to avoid large clusters at high eta in innermost layers
  - realistic pixels sizes (area matters, not shape – can be sqare or rectangular)
    - ~10x10 µm with little intelligence, but with LHC-speed, sparse readout, ...
    - ~20x40 µm should be able to contain all features one could wish for
- track-trigger applications?
  - current ATLAS concepts work with short-strip layers without stereo-angle
  - 3 double-layers necessary due to fake-rate
  - improved resolution (in particular in z) would significantly reduce this
    - no loss of z-information for tracking purposes
    - better track resolution → better spacer thickness/pT resolution ratio
  - MAPS-chips could already contain the combination logic



Conclusions

- HV-CMOS processes might yield radiation-hard, low-cost, improved-resolution, low-bias-voltage, low-mass sensors
- First test chips indicate rad-hardness up to at least 1e15 n_{eq}/cm^2
  - general principles suggest rad-hardness up to full HL-LHC fluence
- Process can be used for
  - 'active' n-in-p sensors
  - drift-based MAPS chips (baseline for µ3e-Experiment at PSI)
- First active sensor design submitted within ATLAS framework
  - capacitively coupled pixel sensors
  - “virtual” strip sensors
  - Irradiation and testbeam campaign planned for 2012
    - up to HL-LHC fluences
    - testbeam at CERN with Timepix telescope
- First test chip in standard 65nm CMOS process
  - pixels with 2.5 µm pitch, though no intelligence
  - only ~µm depletion, but S/N still good (low capacitance)
  - should try deep n-well allowing more bias voltage and some more realistic pixel size/intelligence