Progress on Scribe-Cleave-Passivate (SCP) Slim Edge Technology

Vitaliy Fadeyev[1], Hartmut F.-W. Sadrozinski[1], Scott Eli[1], John G. Wright[1],

Marc Christophersen[2], Bernard F. Phlips[2],

Riccardo Mori[1,3], Matteo Cartiglia[3], Mara Bruzzi[3]

(1) Santa Cruz Institute for Particle Physics, University of California Santa Cruz

(2) Code 7654, U.S. Naval Research Laboratory

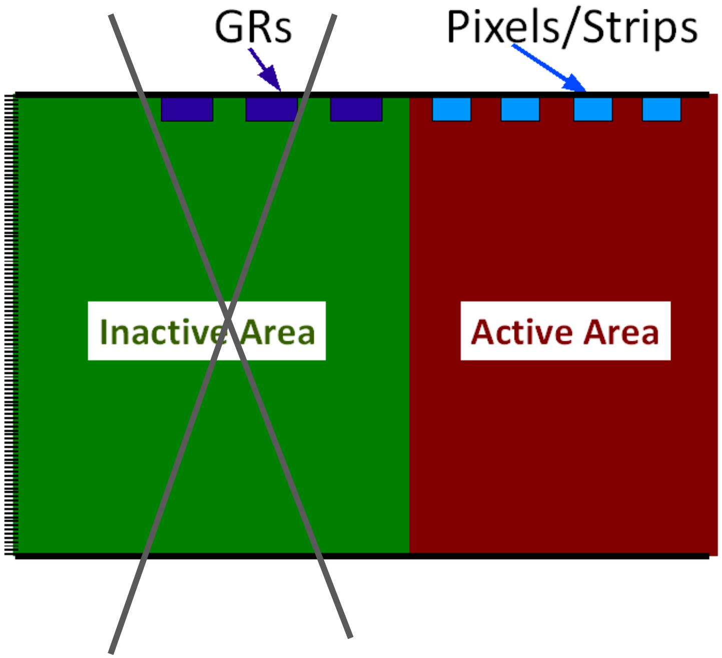
(3) University of Florence

Outline

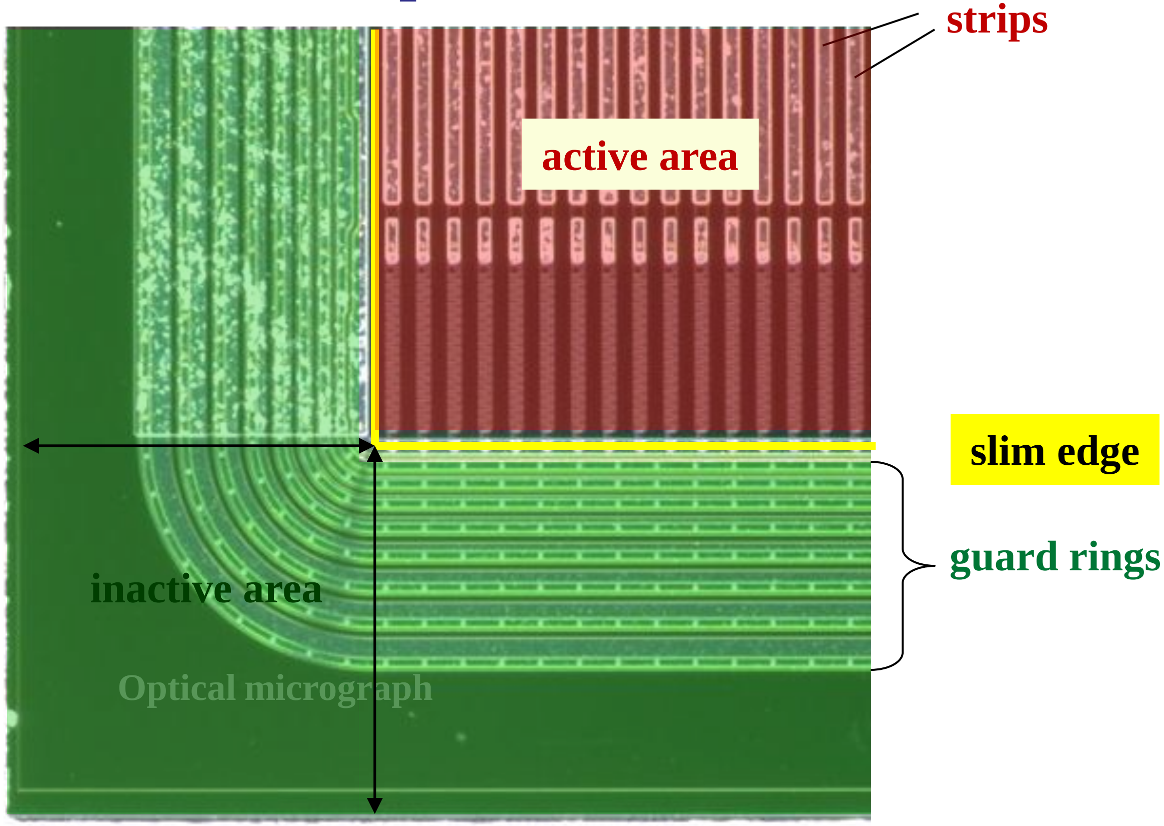
- Slim Edges – Motivation
- SCP Method
- Recent Progress:
  - Passivation for N-type devices
  - Scribing
  - Industrialization
  - Radiation Hardness
  - Charge Collection
- RD50 and Matrix of Requests
- Conclusions and Outlook

Motivation – Slim Edges

Side View



Top View



Slim edges offer:

- **reduced inactive area =>**
- **more hermetic coverage (better tiling of sensors)**

This is especially important for pixels and large-area systems

Our Approach:

- **treat finished devices on the single die level**
- **treat p- and n-type devices**
- **minimize leakage current**
- **achieve uniform bias dependence of charge collection**

SCP Method

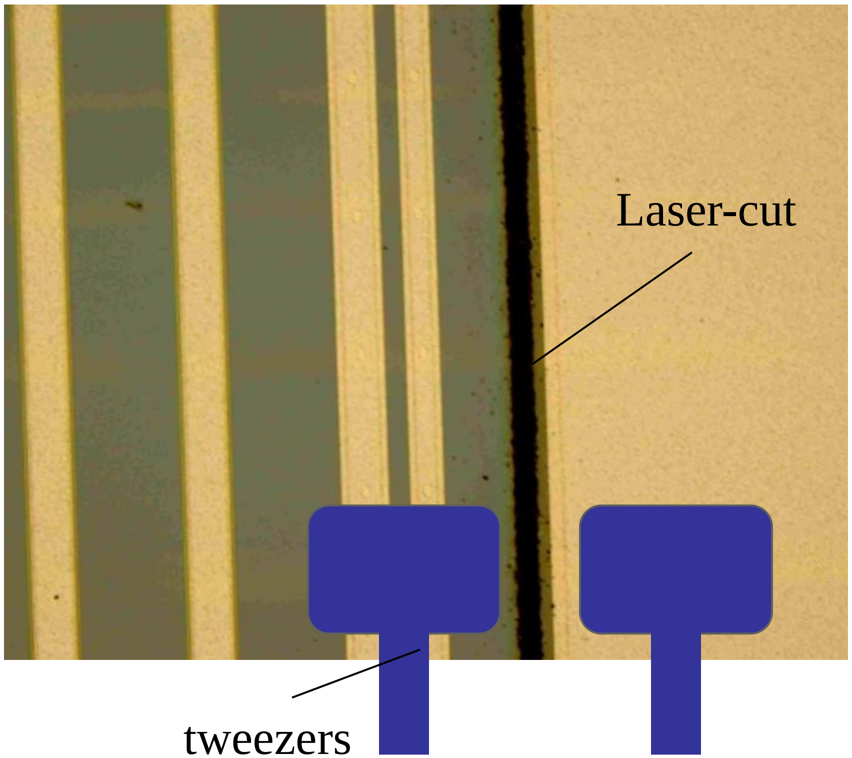
There are three key steps of the process:

1) Scribing on front-side (initially done by laser)

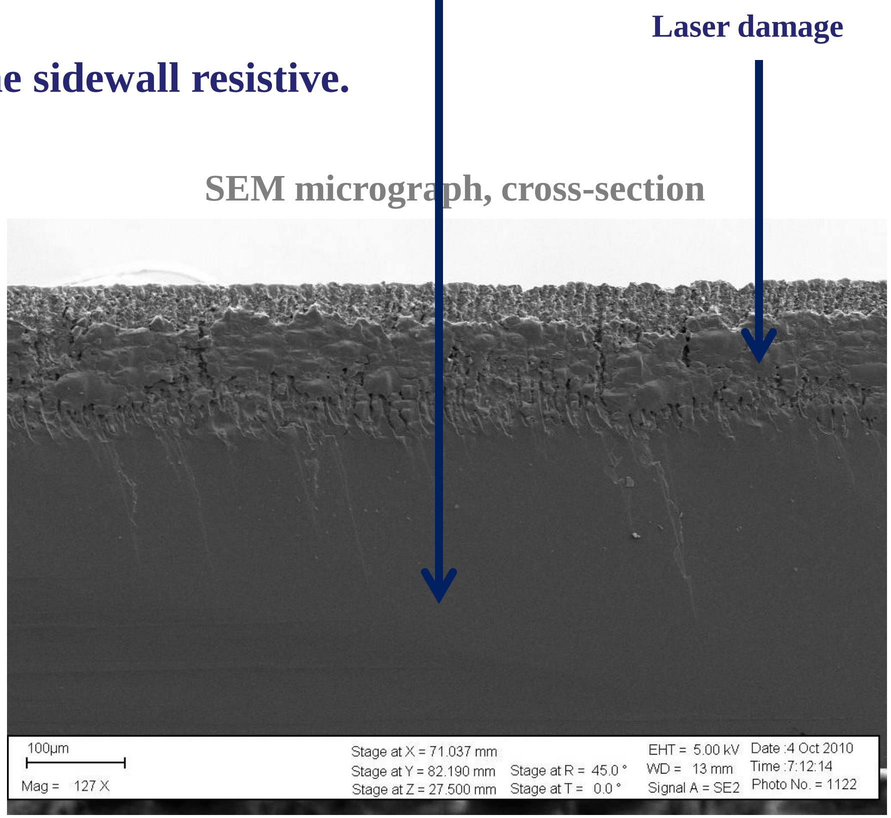
2) Cleaving, which leaves the surface with low defect density (initially done by tweezers)

3) Surface passivation to make the sidewall resistive.

Optical micrograph, top-view

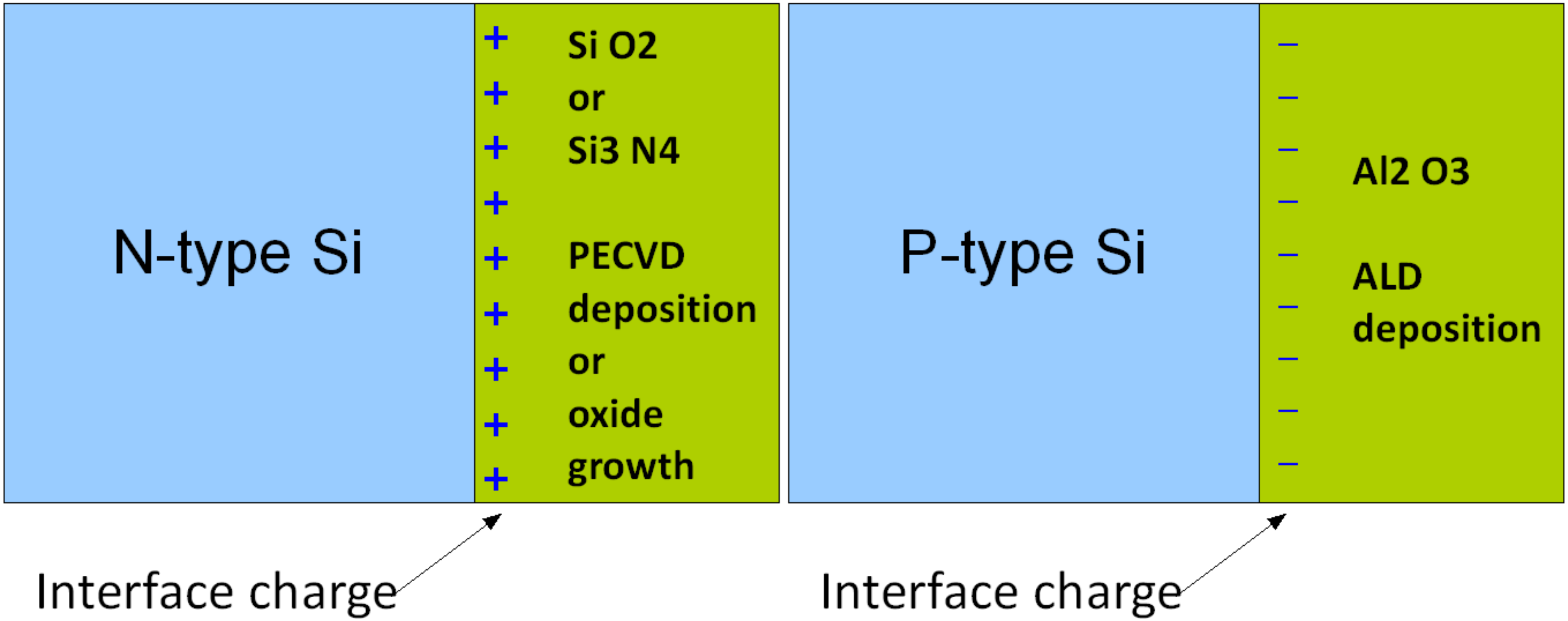


SEM micrograph, cross-section



Laser-scribing done at U.S. Naval Research Laboratory using an Oxford Laser Instruments E-Series tool. Breaking was initially done by hand using tweezers, but can be done fully automatic.

Passivation Options

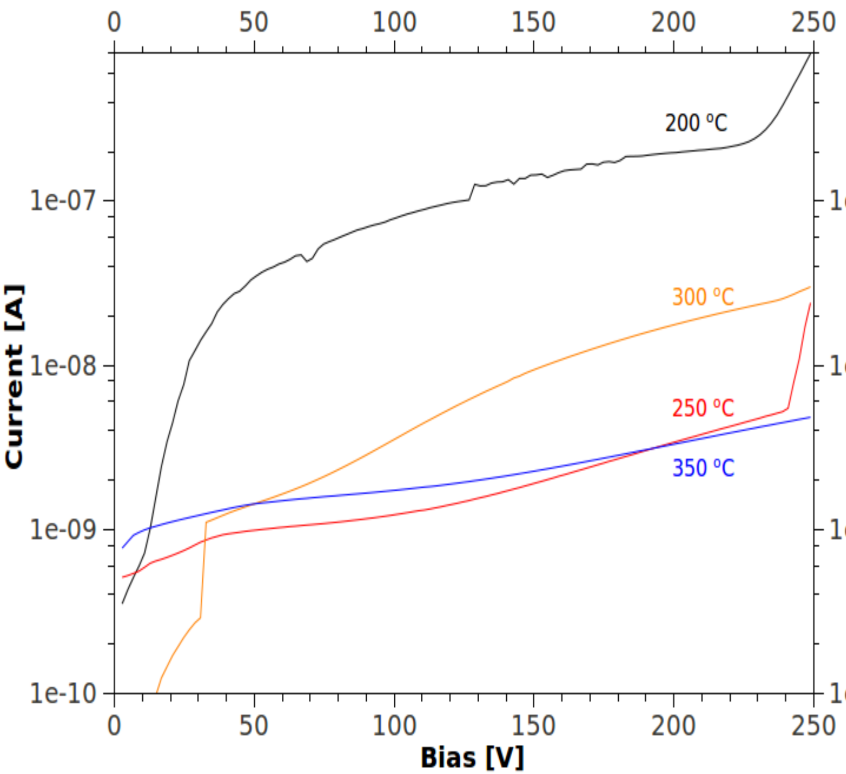


Surface passivation makes the sidewall resistive. N- and p-type devices require different technologies.

- **For n-type devices one needs a passivation with *positive* interface charge. SiO_2 and Si_3N_4 layers works well.**
- **For p-type material a passivation with negative interface charge is necessary. We found that Al_2O_3 works in this case.**

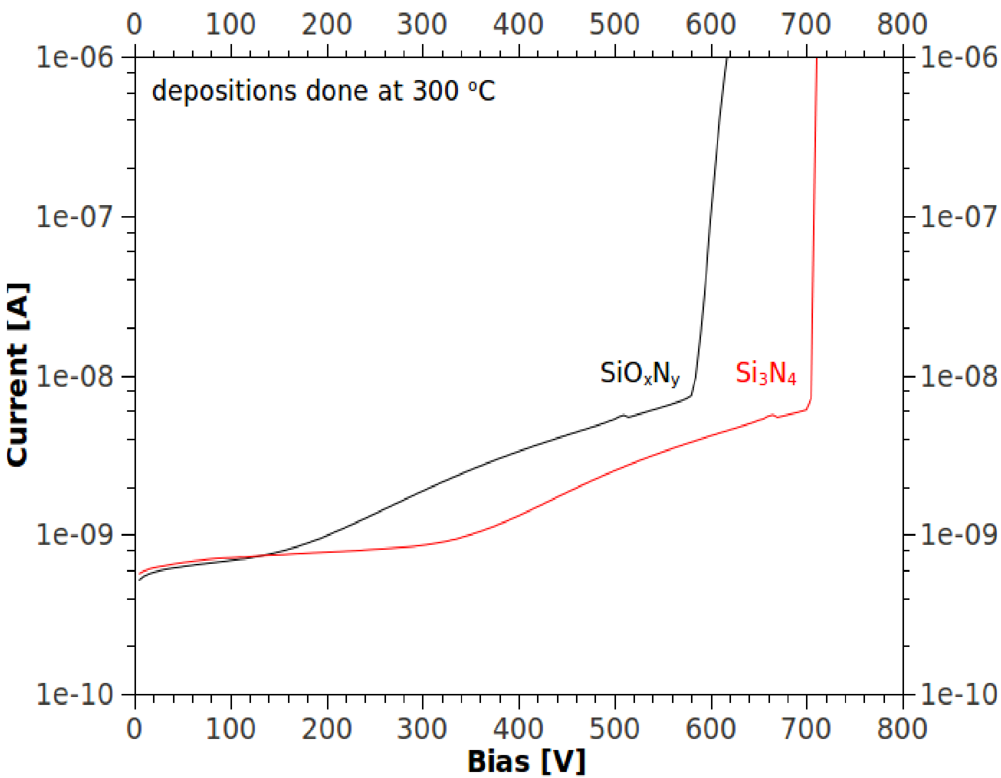
Progress with Passivation (N-type Diodes)

Si Oxide PECVD



Performance dependence on the deposition temperature:
Can work in the T range that is safe for the finished devices!

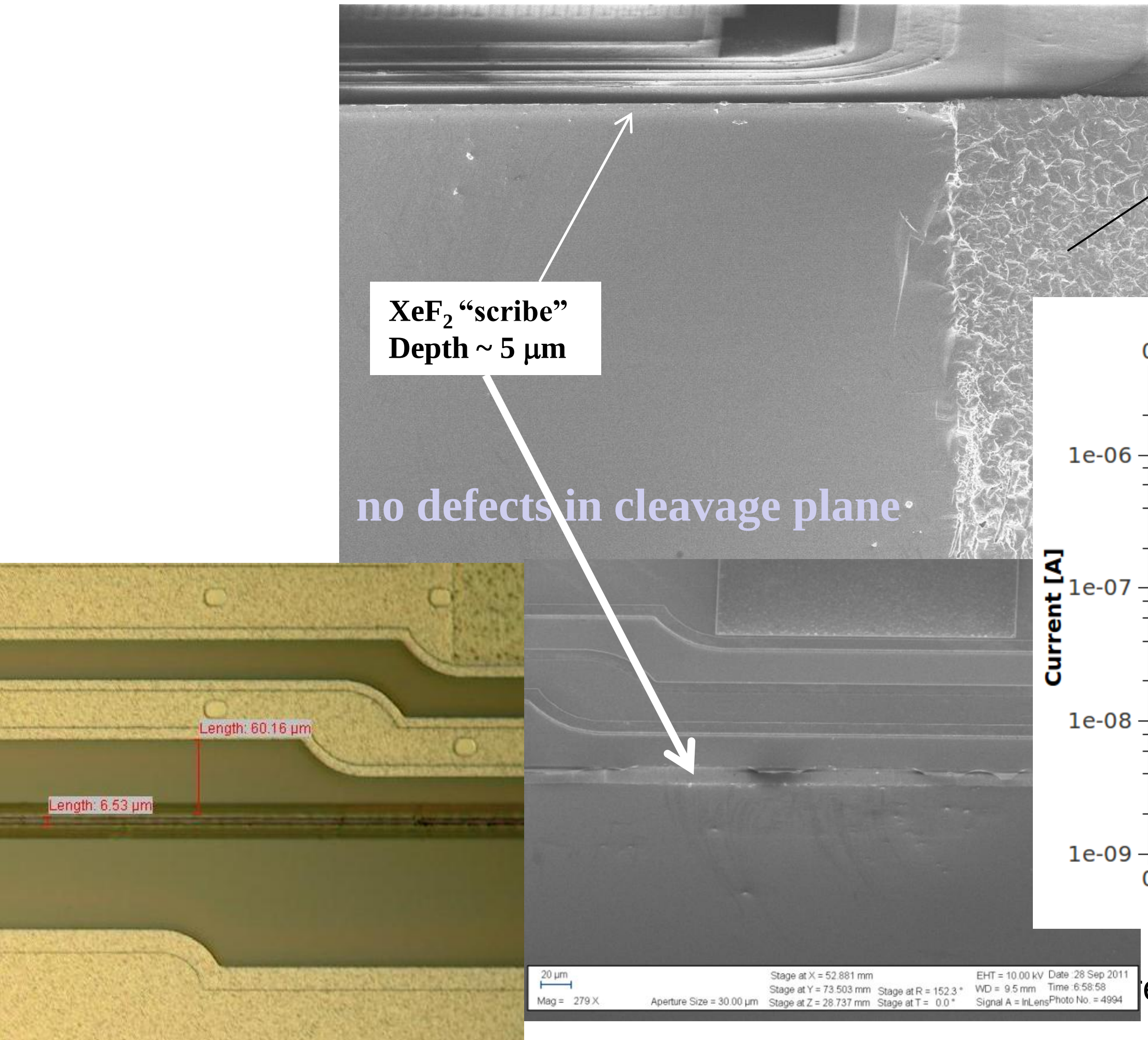
Si Nitride PECVD

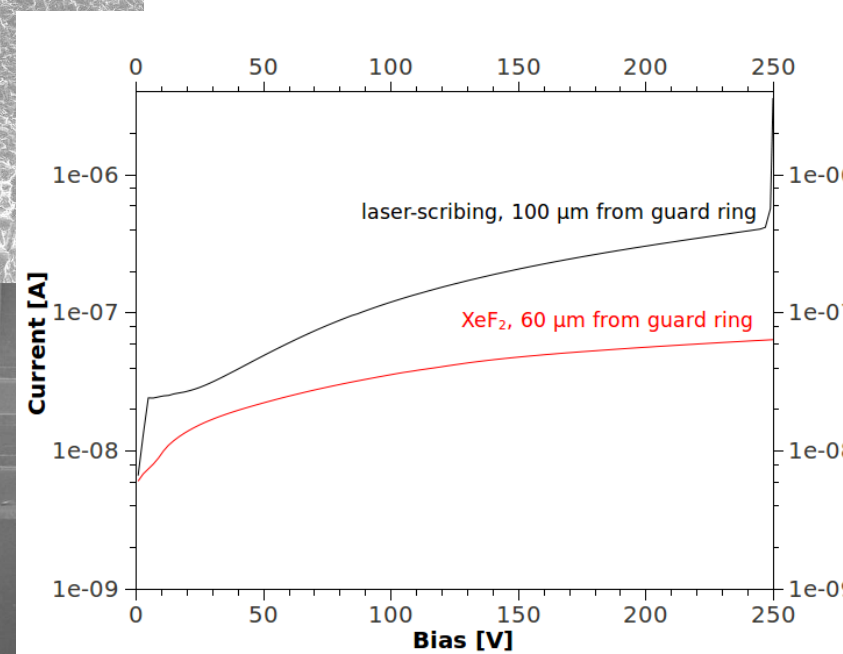


Much improved leakage current and breakdown voltage with Si Nitride.

Progress in Scribing

Laser Scribing → XeF_2 Etch:
reduction of the amount of sidewall damage, more control, reliability

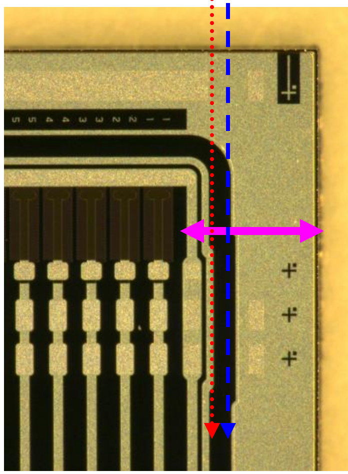




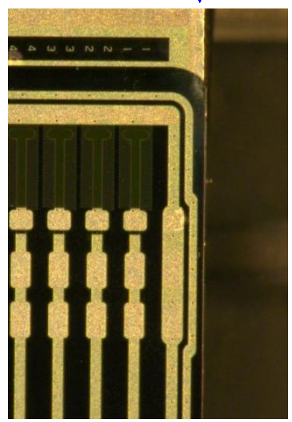
Progress with N-type Sensors

XeF2 scribing + Nitride PECVD

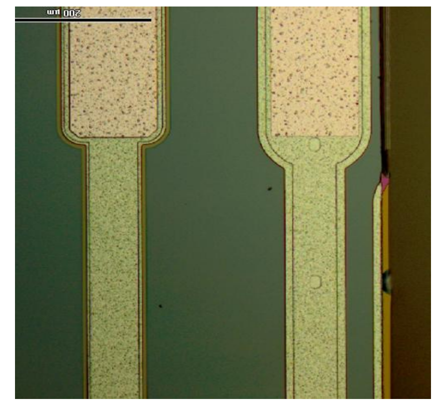
Si SSD with
900μm dead edge

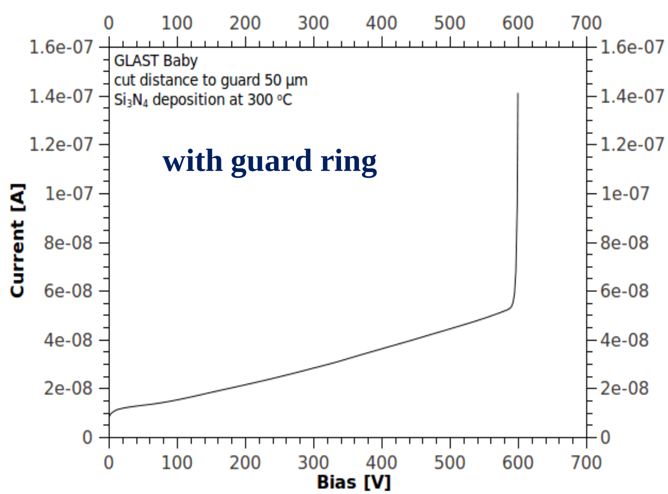


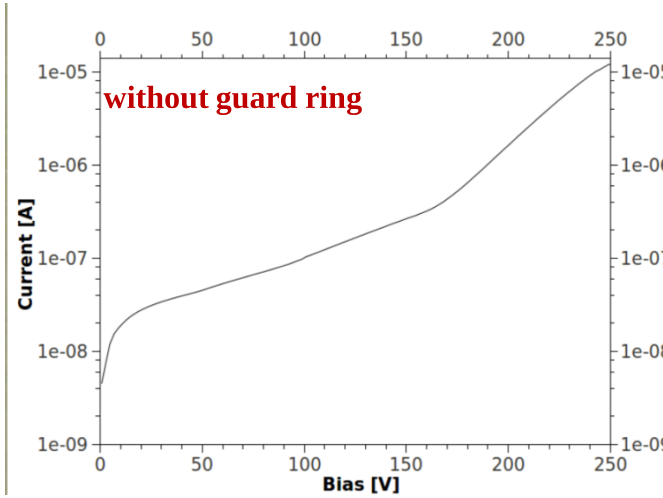
Cut within 50 μm
of Guard Ring



Guard Ring Cut (!)
0 μm to Guard Ring

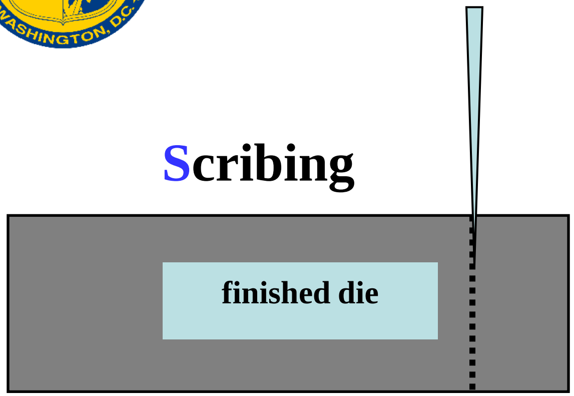






Evolution of Slim Edge SCP Treatment

Scribing

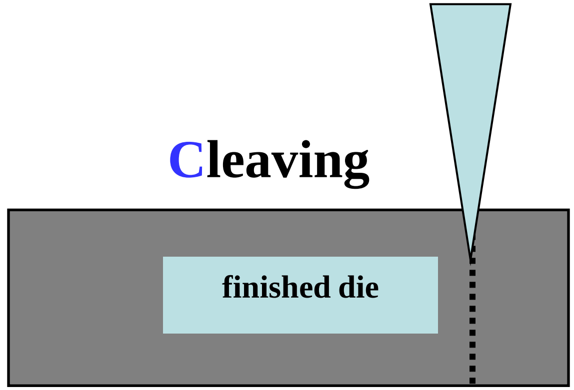


Laser

↓

XeF_2 Etch

Cleaving



Tweezers

↓

Present Focus: Automated Cleaving

Passivation

Native Oxide + Radiation

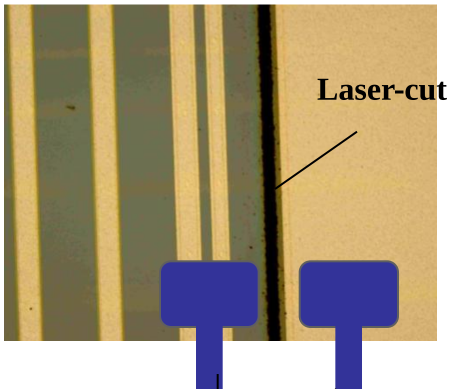
N-type → **PECVD Oxide** → **PECVD Nitride** → **CCE, Rad. Hardness**

P-type → **ALD Alumina** → **CCE, Rad. Hardness**

All Treatment is post-processing & low-temp (Etch-scribing can be done during fabrication)

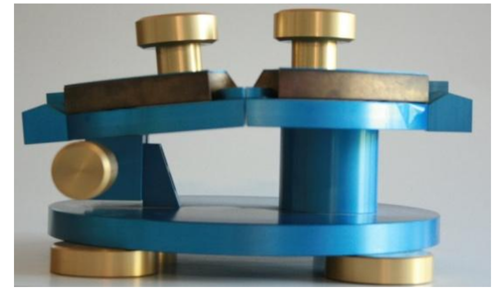
R&D for Large-Scale Application of SCP

Key issues in making further progress: replacement of tweezer-based cleaving!



Build

Wafer Brech Maschine
Courtesy PSI and Uni Bonn



Contract

Industrial-scale cleaving machines:
- Dynatex (manufacturer)
- Loomis Industries (manufacturer)
- Kavli Nanosciences Institute @ CIT (facility)

LOOMIS
Patented Scribe and Break Dicing Technology
LSD-150
Scriber-dicing machine

dynatex INTERNATIONAL
semiconductor dicing equipment and materials
GST-150
ScriberBreaker

Industrialization: Automated Scribing

Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

Automated scribing depends on the method:

- For laser scribing, it's built-in in the programmable laser + motion stages operation
- For etch-scribing, there is a need for an extra mask, but the process in inherently wafer-scale

We are in process of making wafer-level singulation tests:

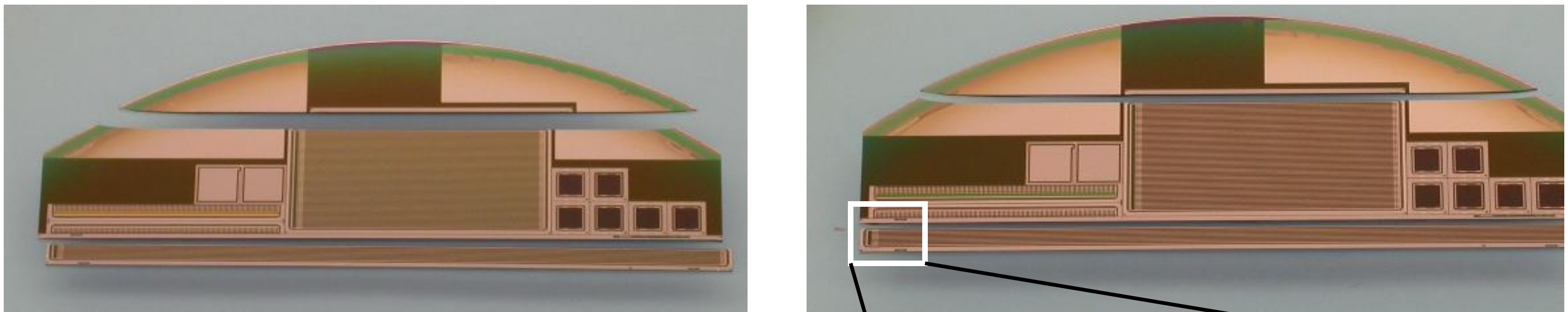
- Post-production scribing with CIS wafers courtesy Anna Macchiolo, as well as wafer pieces from recent "charge multiplication" production at Micron (Gianluigi Casse).
- Discussing scribing during fabrication with low-strip-resistance run at CNM (Miguel Ullan et al)

Besides XeF2 etch, there is an idea of using plasma etching for scribing (Giulio Pellegrini).

Industrialization: Automated Processing

Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides



overview photos

Cleaving tests done at **Loomis Industries**, makers of cleaving machines.
Loomis was able to cleave the laser-scribed sensors , but not etch-scribed ones.

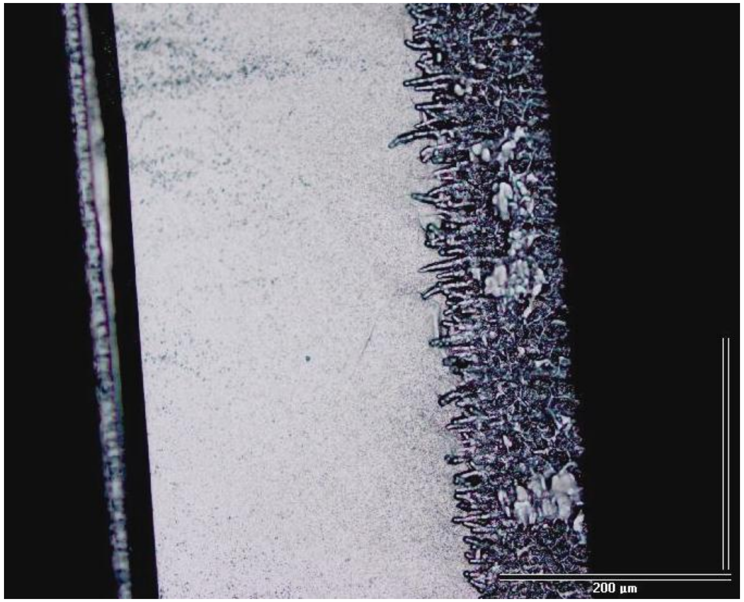
Optical micrograph, "skinny"

Industrialization: Automated Processing

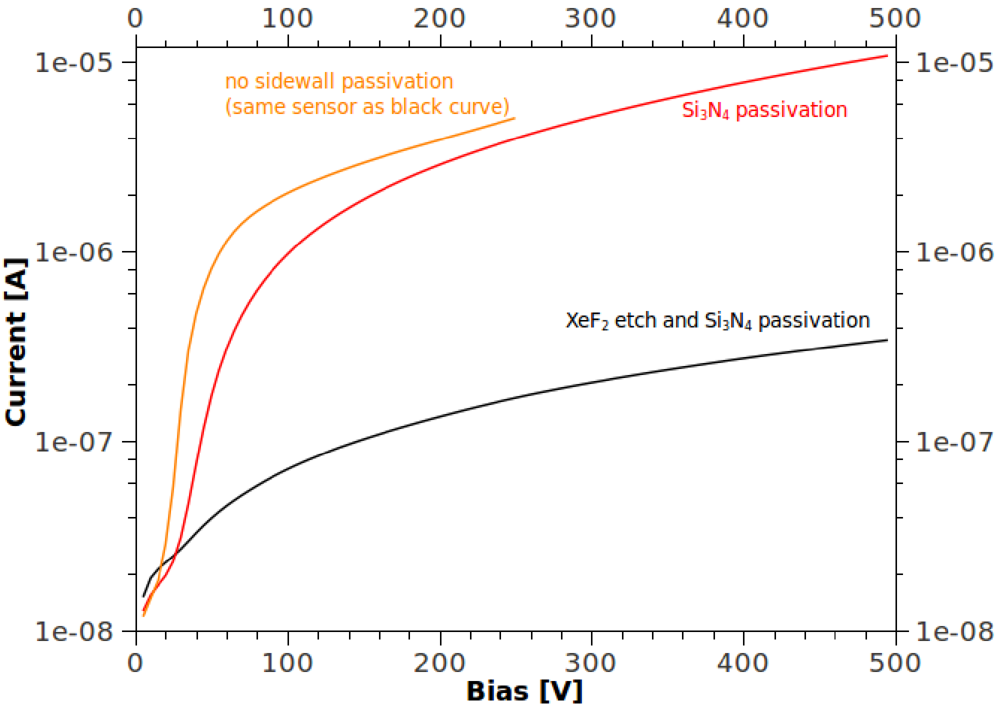
Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

Initially had high current after cleaving, even with passivation.
A key improvement was XeF2 etching of the sidewall, that removed the surface damage.



Sidewall surface after etching step.



Industrialization: Realistic Singulation

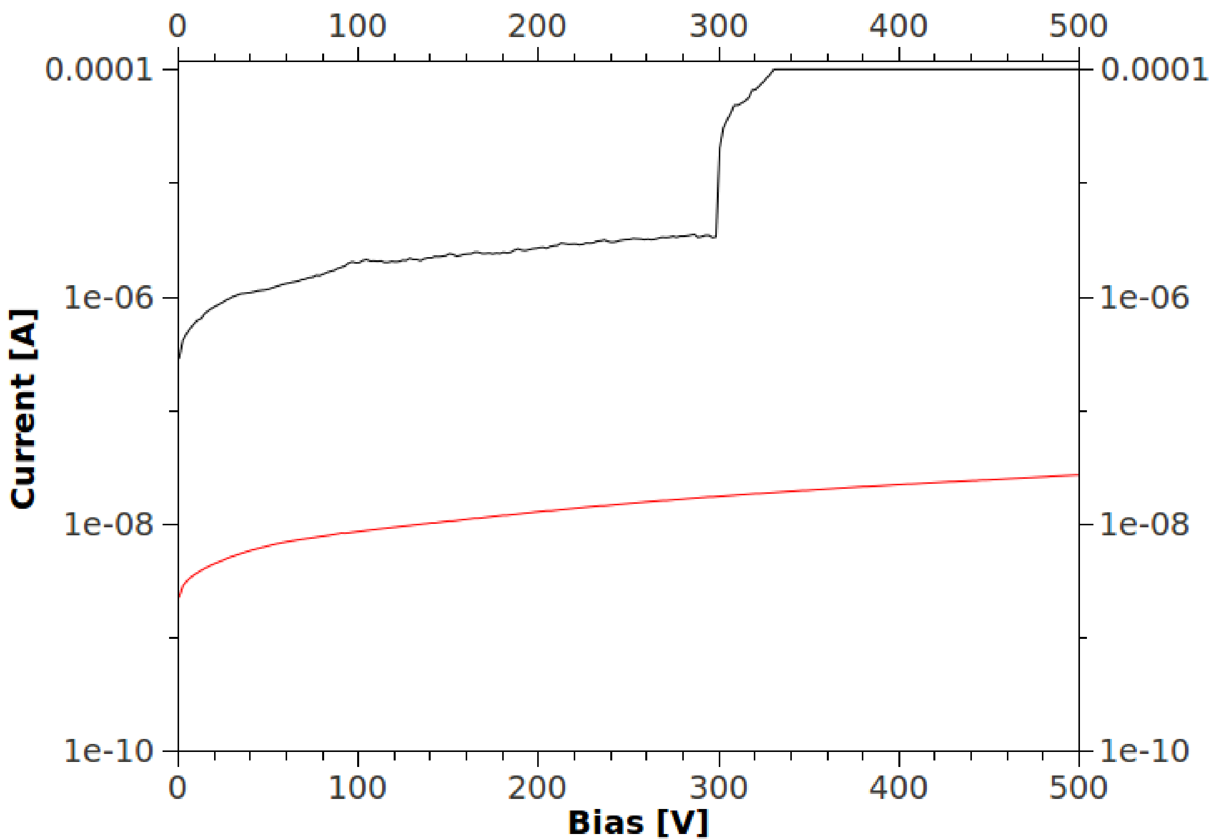
Production-ready device singulation is different from initial trials:

1) Automated scribing
2) Automated cleaving
3) Done on all four sides

4-side cleaving means intersecting cleaved wall with 'sharp corner".

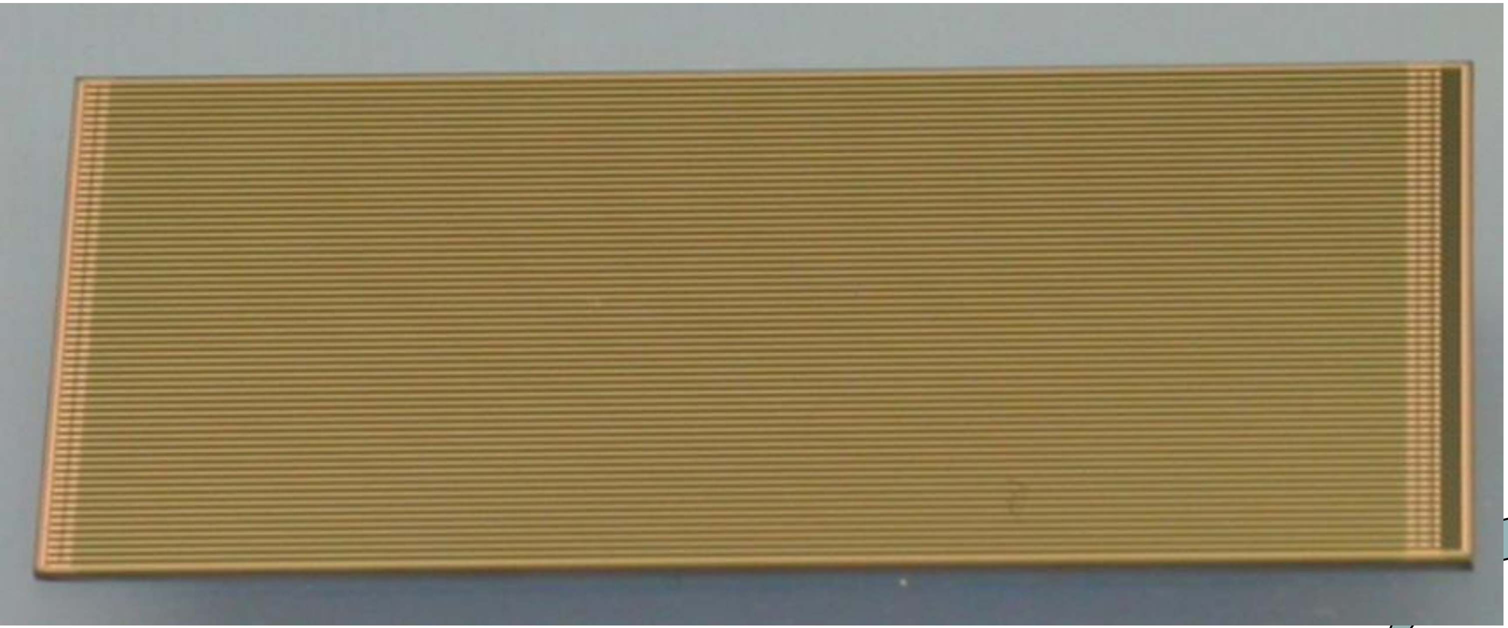
This leads to high current.

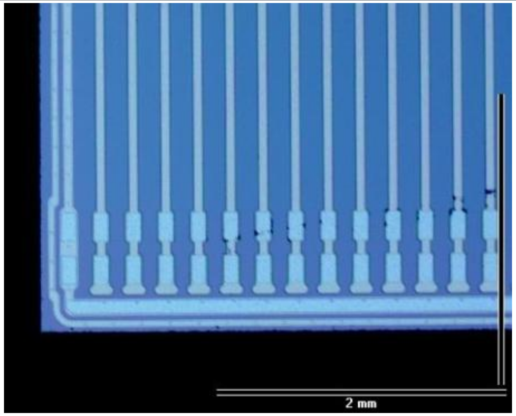
XeF2 etching of the sidewall drastically reduces the current – by two orders of magnitude!



Four-side Cleaving

An example of a device cleaved on all four sides.
This is what we'd like to make!

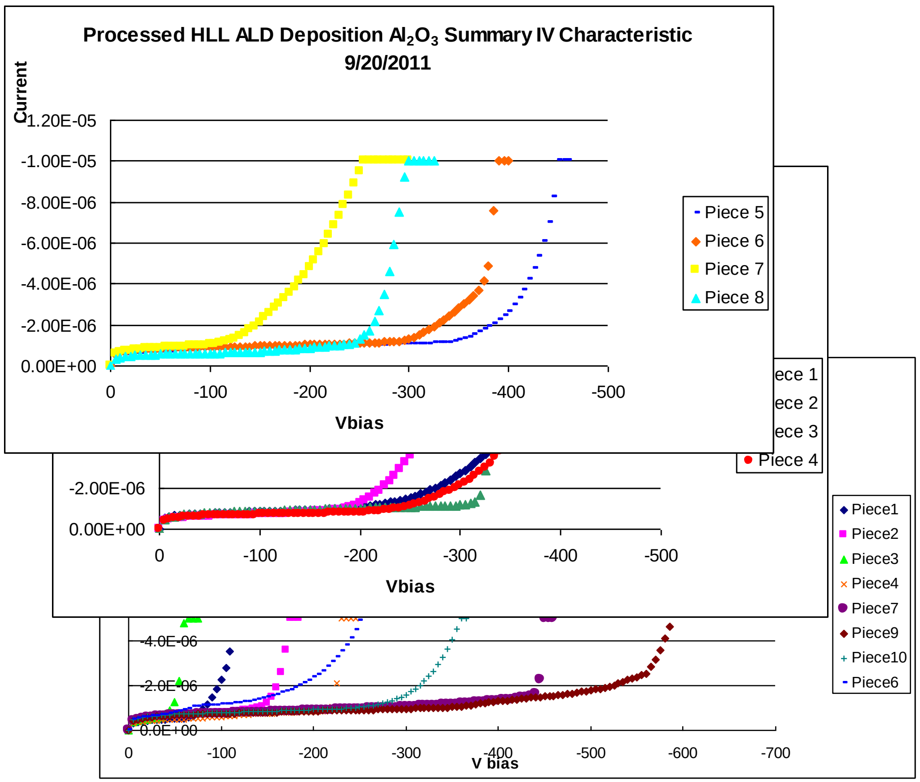




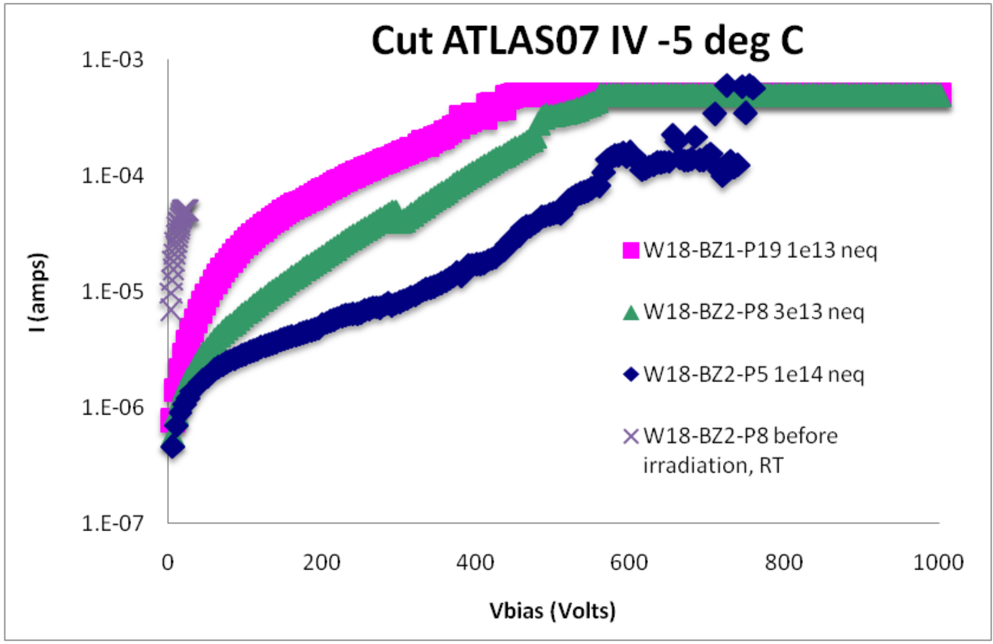
Irradiation Studies

One of the key questions is a performance of the new sidewall technology under irradiation. Work is on-going:

- **We have irradiated 12 processed strip devices (CIS courtesy A. Macchiolo) at LANL in Dec.**
- **We took available cleaved HPK devices (ATLAS07) from prior trials and irradiated them in LANL proton beam. They do not have Al_2O_3 deposition => did NOT work before the irradiation. They are starting to work after 10^{13}-10^{14} neq/cm^2. This observation lends hope that the irradiated devices with alumina will work as well.**



Characterization of HLL sensors before irradiation (total of 21 sensors processsed)

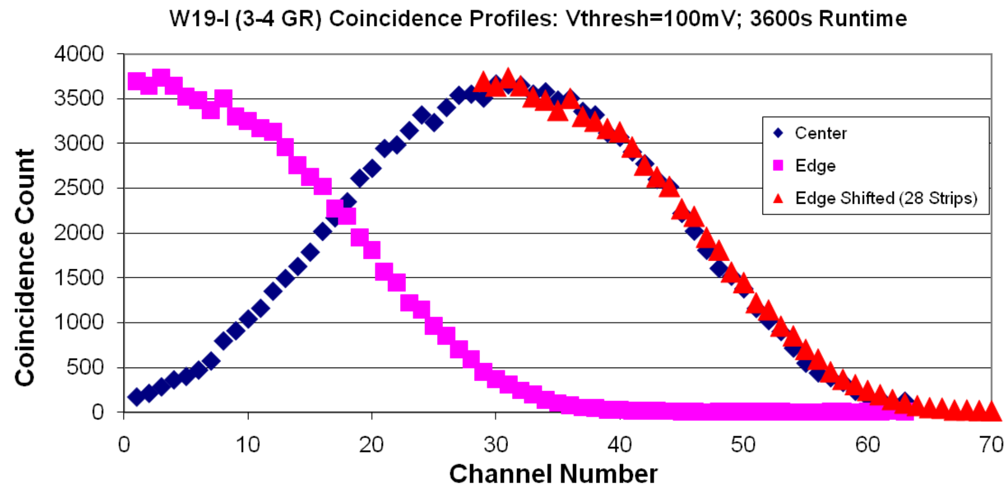


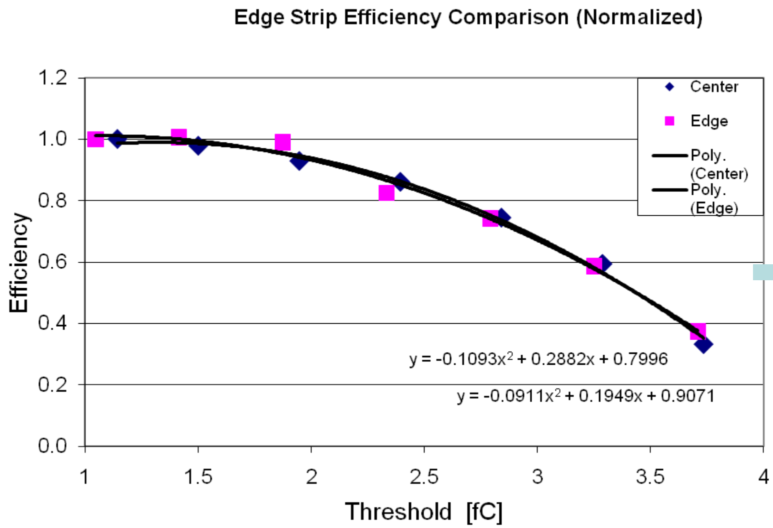
Irradiation	1.00E+13	3.00E+13	1.00E+14
I_expect (200V)	7.50E-07	2.25E-06	7.50E-06
I_observe(200V)	7.39E-05	2.02E-05	5.16E-06
Observe / expect (for bulk current)	98.57	8.99	0.69

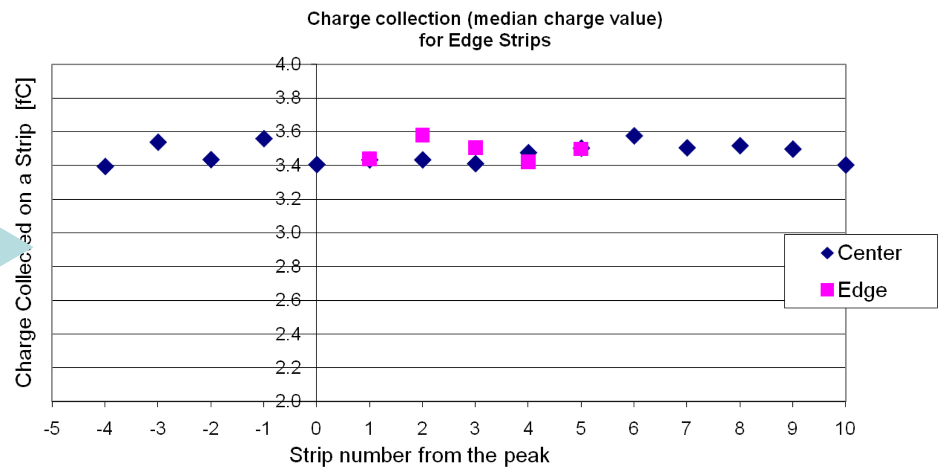
Charge Collection With Binary Readout System

We want to make sure that the charge collection near the edge does not suffer because of the slimming.

- **Consistent beam profiles taken at different positions is an indication of high efficiency at the edge.**
- **By scanning the thresholds we can derive the collected charge on each strip.**
- **We observe the same collected charge at all locations to a few percent on a p-type sensor.**

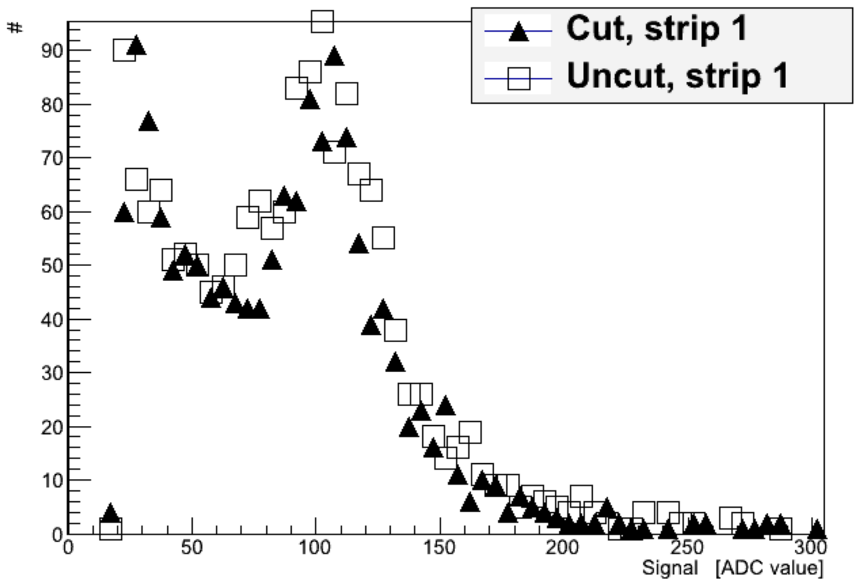




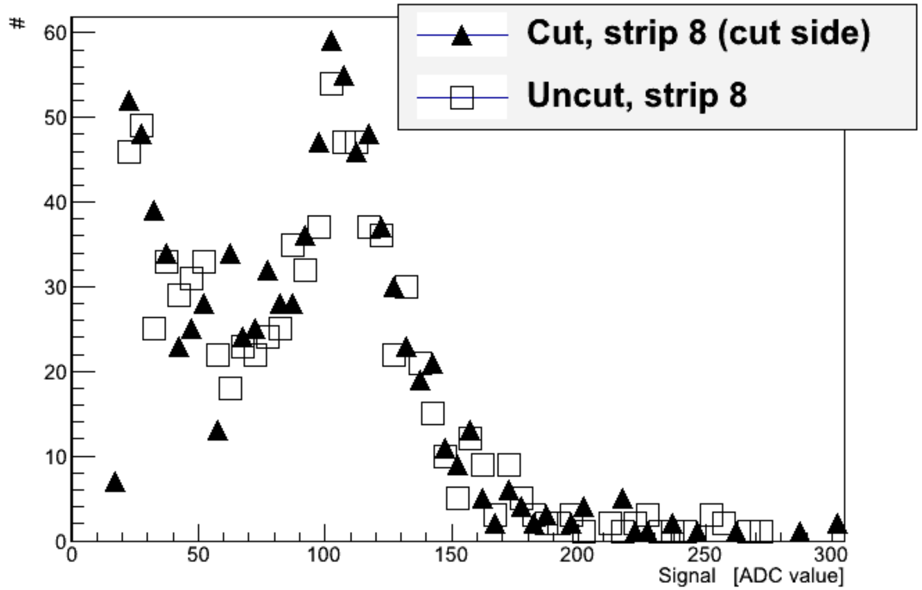


Charge Collection with AliBaVa

AliBaVa allows pulse height readout => More direct view of the signal.
Data taken and analyzed by R. Mori of Florence.



Edge strips at the normal (wide) edge



Edge strips at the slim (cut) edge

- **A comparison of the data from two n-type Fermi detectors from HPK, one after slim edge processing, another without. The cut is 100 um from the GR.**
- **The pulse height for the "outer" strip (closest to the edge) might be less by about 4%. The low-side tail is due to absence of neighbor for clustering.**

SCP: RD 50 Common Project

The initial trials started within the framework of ATLAS Planar Pixel Collaboration.

Last summer, the scribe-cleave-passivate (SCP) technology of fabricating slim edge sensors has been approved as RD50 project.

The participating institutions are interested in p- and n-type and 3D sensors.

We are currently actively working with CNM Barcelona, FBK Trento, MPI Muenchen, UNFN Bari, Ljubljana U., Glasgow U., and TU Dortmund on SCP application to their devices

Note that the methods developed are rather generic, applicable to a wide variety of Si devices.

RD50 funding request

- Date: *05-26-2011 (Distributed version)*

Development of "slim edges" using cleaving and ALD processing methods
Hartmut Sadrozinski (UC Santa Cruz) hartmut@scipp.ucsc.edu
Vitaliy Fadeyev (UC Santa Cruz) vf@scipp.ucsc.edu

1. *UC Santa Cruz, V. Fadeyev vf@scipp.ucsc.edu*
2. *Liverpool U., G. Casse gcasse@hep.ph.liv.ac.uk*
3. *INFN Bari, D. Creanza donato.creanza@ba.infn.it*
4. *Ljubljana U., G. Kramberger gregor.kramberger@ijs.si*
5. *CERN, M. Moll Michael.Moll@cern.ch*
6. *Freiburg U., U. Parzefall Ulrich.Parzefall@cern.ch*
7. *Florence U., M. Bruzzi mara.bruzzi@unifi.it*
8. *CNM Barcelona, G. Pellegrini giulio.pellegrini@csic.es*
9. *PSI, T. Rohe tilman.rohe@psi.ch*
10. *Glasgow U., R. Bates r.bates@physics.gla.ac.uk*
11. *Prague, M. Solar michael.solar@fs.cvut.cz*
12. *Vilnius U., J. Vaitkus juozas.vaitkus@ff.vu.lt*
13. *Trento U., G.-F. Dalla Betta dallabe@dit.unitn.it*
14. *Dortmund U., D. Muenstermann Daniel.Muenstermann@gmx.de*
15. *HLL Muenchen, A. Macchiolo annamac@mail.cern.ch*

1. *US Naval Research Laboratory, Bernard Phlips*
2. *FBK Trento, M. Boscardin*

SCP: RD 50 Current work

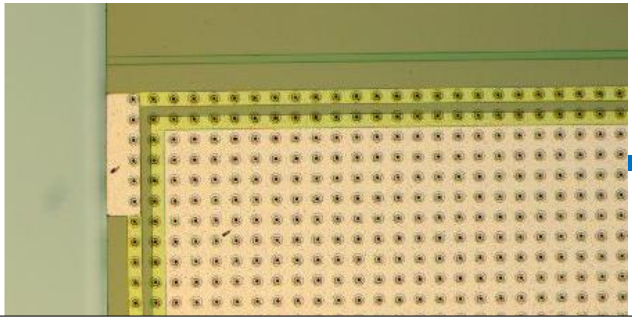
We are very happy to fulfill "slim edge" requests from the RD50 Collaboration

Institute	Contact Person	Sensors	Status
CNM Barcelona	G. Pellegrini	3D diodes, strips, pixels	Completed (next slide) **
FBK Trento	G.-F. Dalla Betta	3D diodes, strips	In progress (next-2 slide)
MPI Muenchen	A. Macchiolo	P-type planar pixels	In progress**
UNFN Bari	D. Creanza	N-type "SMART" detectors	On hold**
Ljubljana U.	G. Kramberger	P- and N- type	Devices sent
Glasgow U.	R. Bates	P- and N- type	Discussions
TU Dortmund	T. Wittig	IBL-style n-on-n sensors	Initial tests done, discussions

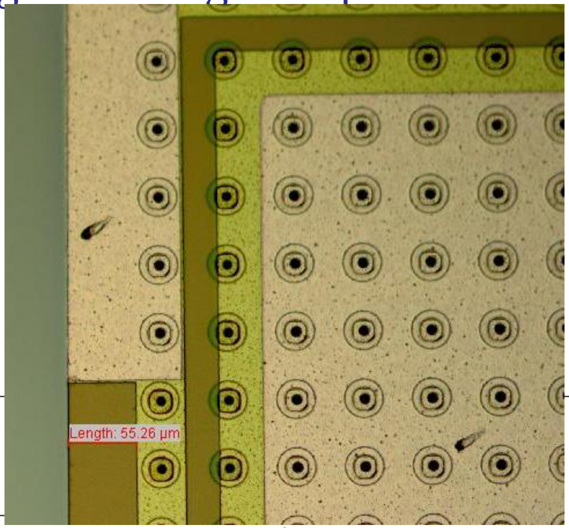
**In these instances we are limited by the available margin around the device and performance of the "tweezers" technique. Automated cleaving machines should work better.

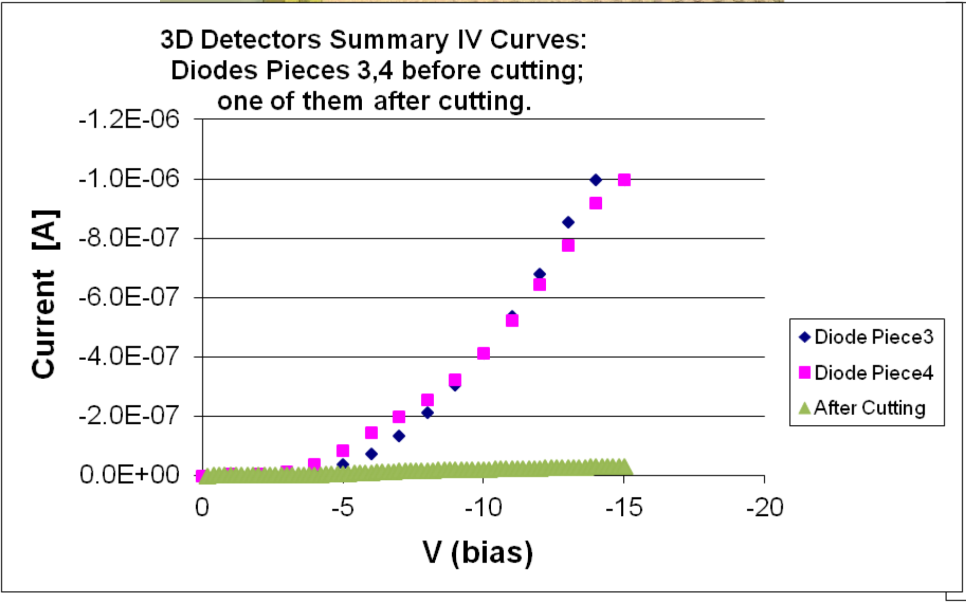
CNM 3D Sensors: p-type (Alumina Passivation)

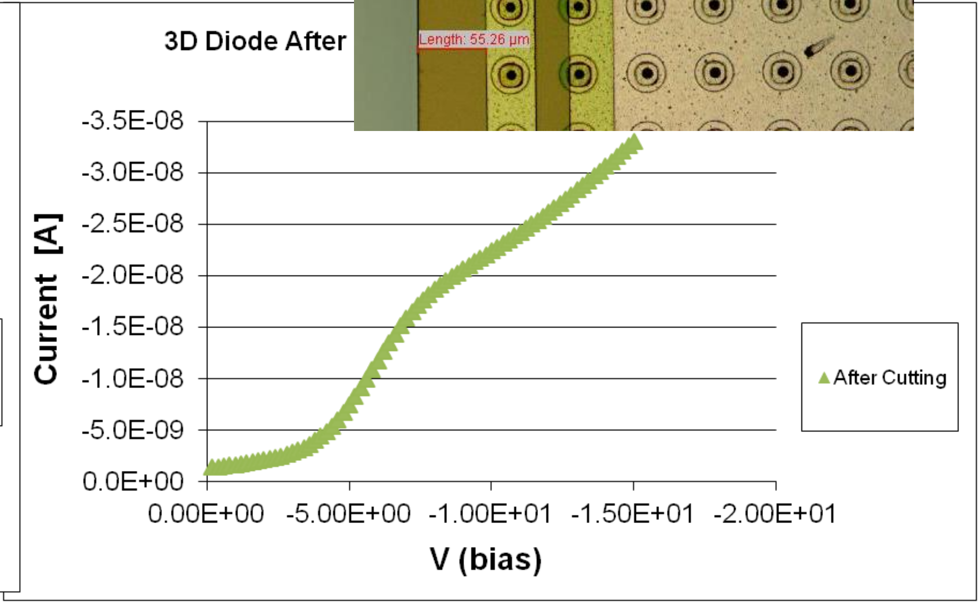
- This is 3D diode fabricated by CNM. It was cleaved at 55 um away from GR.
- As a result of the scribing, cleaving, and ALD deposition of alumina, the current seems to *improve* a lot. The exact cause is unknown. It might be a high-temperature exposure post-ALD.



Zoom in





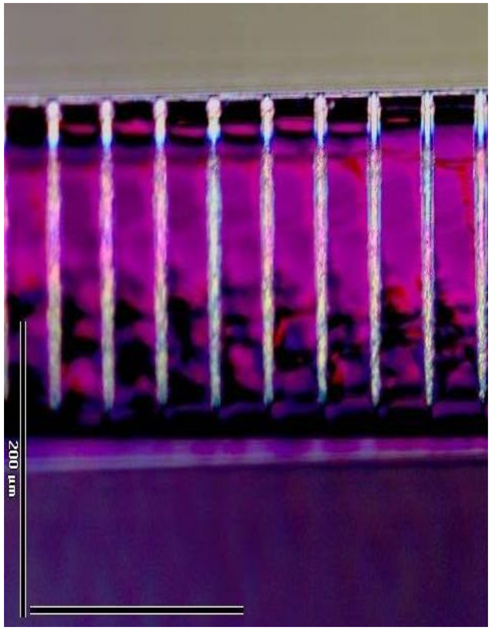


Comparison of before and after cutting

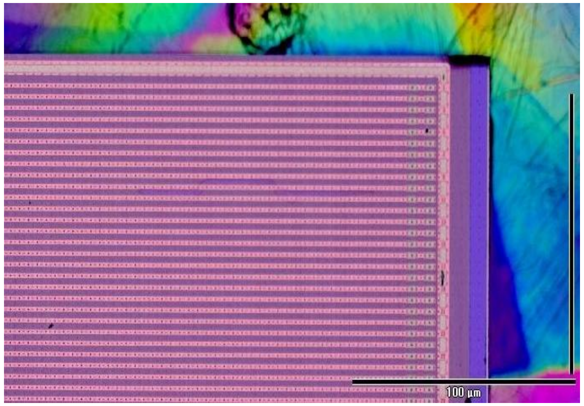
After cutting alone (note different scale).

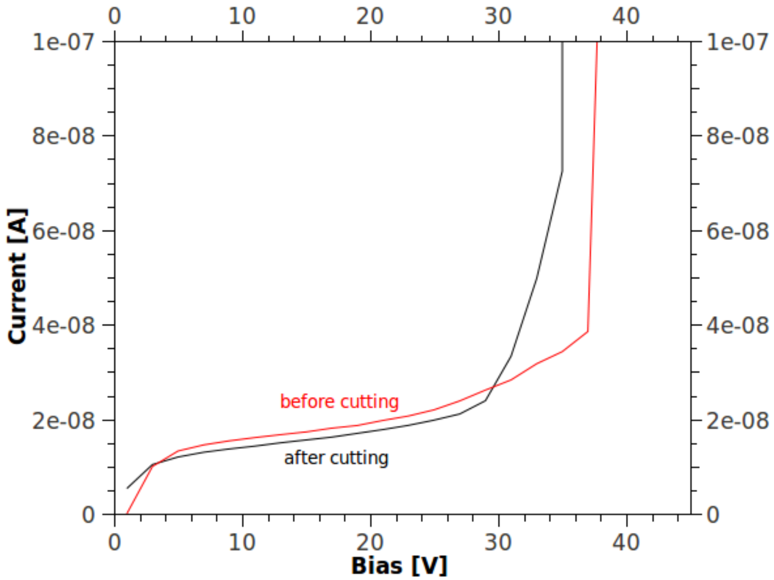
FBK 3D Strip: p-type (Alumina Passivation)

Cleavage plane "follows" row of "guard fence" holes.



Cleavage plane remains parallel to strip (length of device).

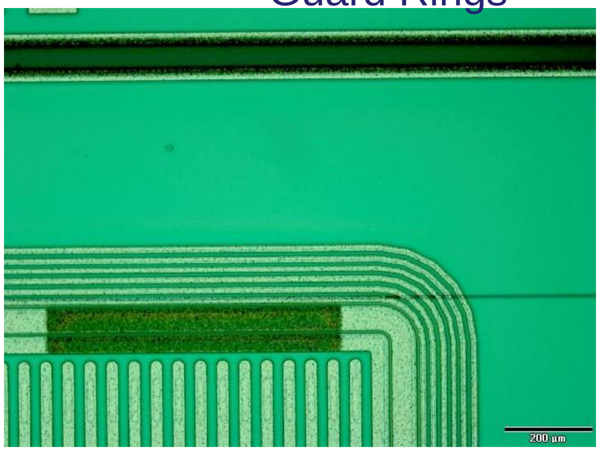


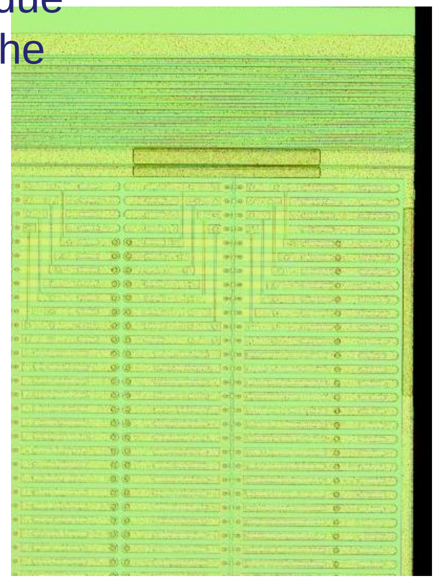


No change in leakage current due to SCP slim edge (50 µm distance from cut to guard)

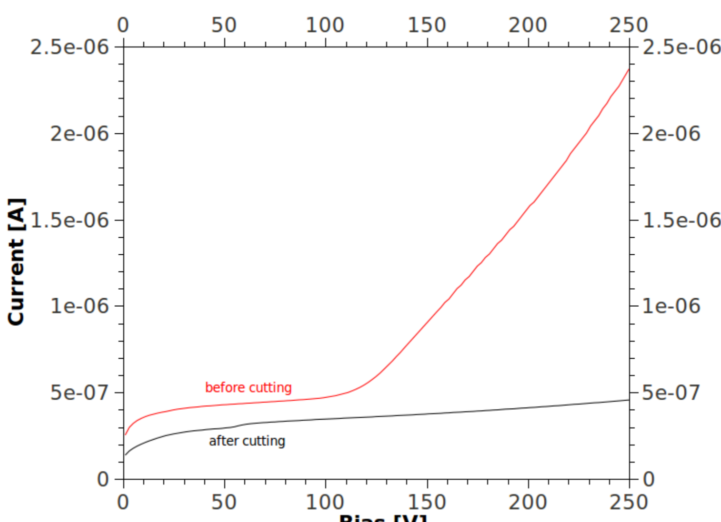
MPI Devices

Initially had issues with post-processing etch-scribing, due to presense of metal on the Guard Rings

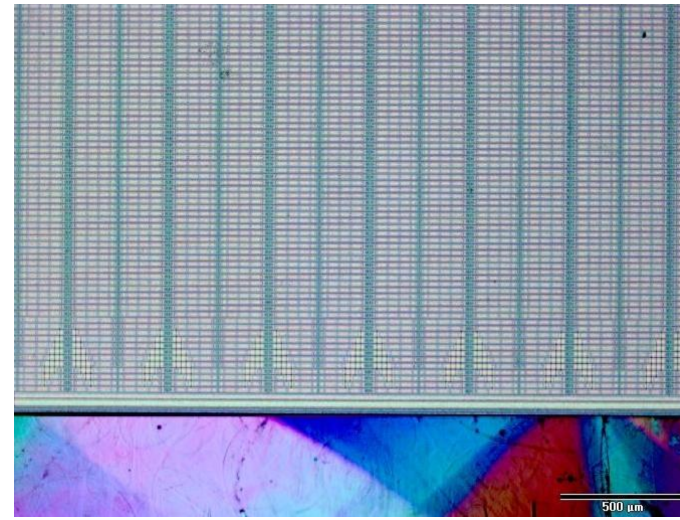


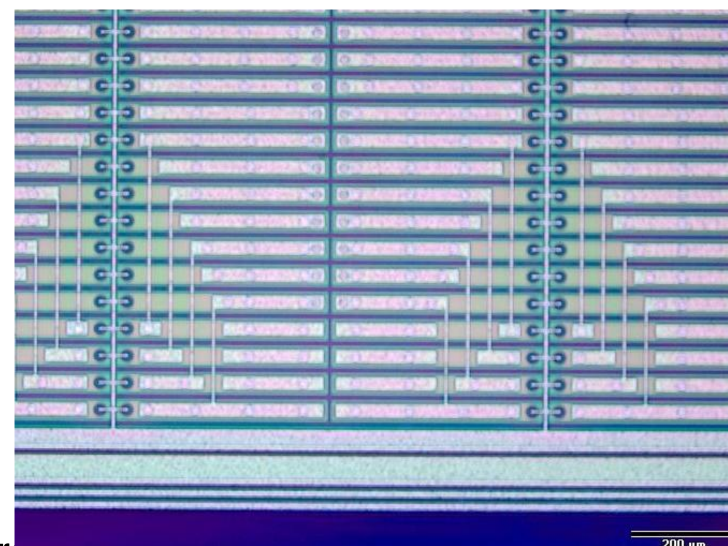


No Guard Ring on one end
But the sensor is still working!



The scribing issue was later solved:





Conclusions and Future Work

- Scribe-cleave-passivate (SCP) method of making a slim edge device holds a lot of promise.
- Work goes on in the framework of PPS and RD50 collaboration.
- The method development continues:
  - Etch-based scribing looks promising
  - For N-type devices, PECVD deposition of nitride/oxide works well
- We have ongoing studies of:
  - Industrialization of the technology – wafer-level automated scribing and cleaving
  - Physics performance: Radiation tolerance, Charge collection
- We are thrilled to perform dedicated studies and service for the community

Acknowledgements

We would like to thank the Institute for Nanoscience (NSI) at the Naval Research Laboratory (NRL) and the NSI staff members.

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U.S. Department of Energy and National Science Foundation.**

Back-Up Slides

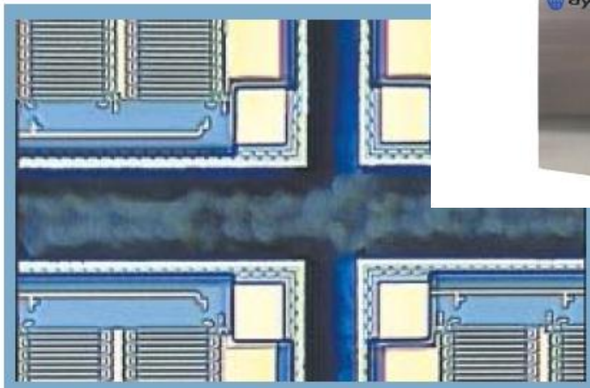
Industrial Applications of Laser-Scribing & Cleaving

SCIPP

HAMAMATSU

Dynatex International DTX-200-AB

AUTOMATED BREAKER PRODUCTION SYSTEM

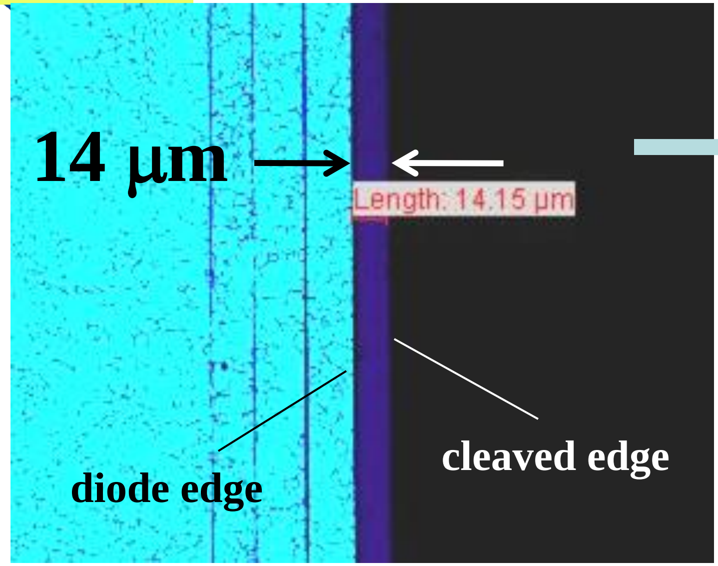


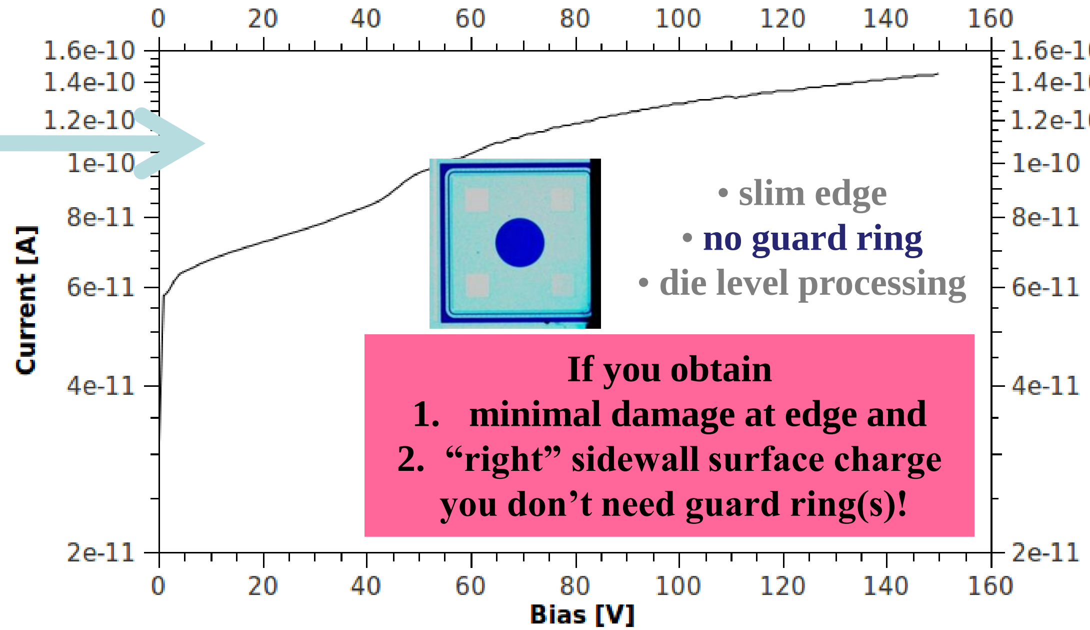
GaAs wafer, diced and expanded. Wafer dicing is well-suited for UV DPSS lasers with their highly focusable, pinpoint-bright beams

- laser-scribing and cleaving common in LED industry
- automated tools for scribing and breaking of devices on wafer-scale

Examples of Processed Devices

Device A

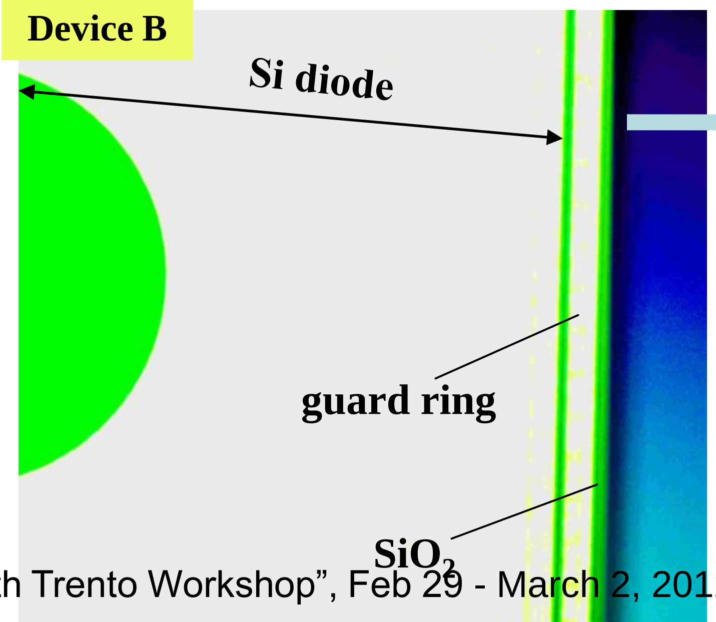


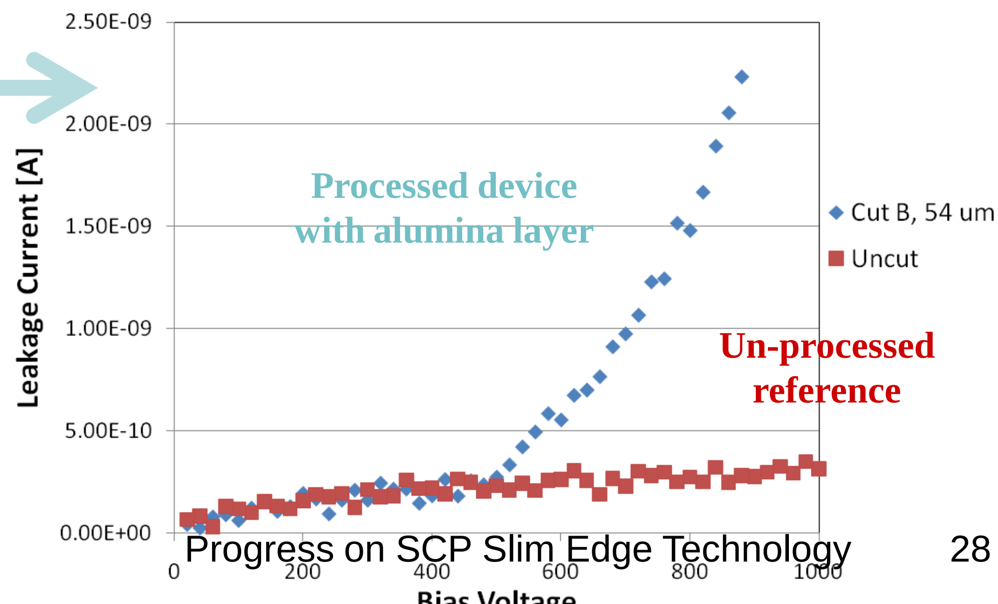


• slim edge
• no guard ring
• die level processing

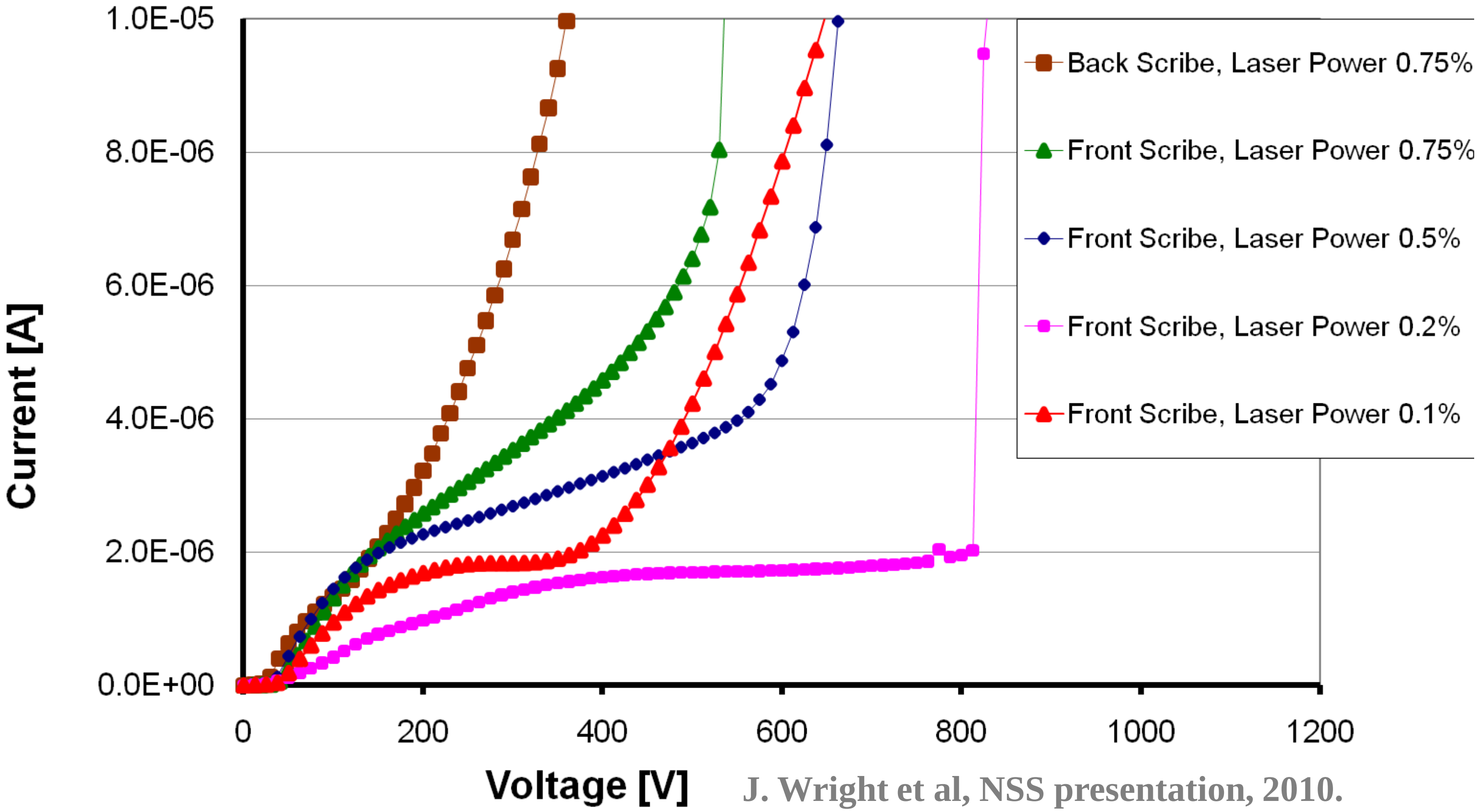
If you obtain
1. minimal damage at edge and
2. "right" sidewall surface charge
you don't need guard ring(s)!

Device B





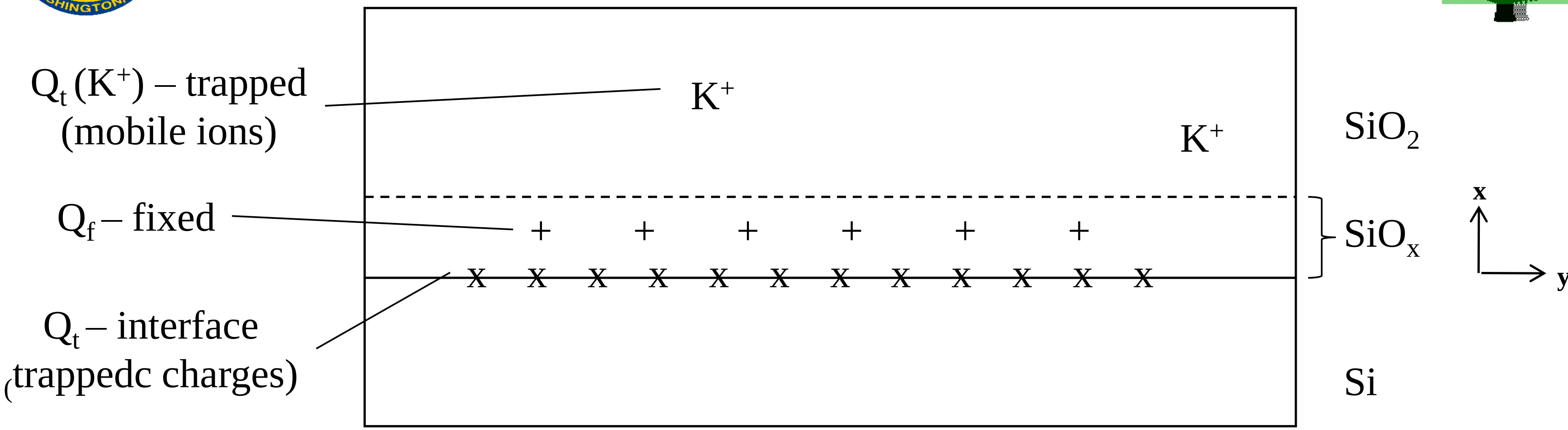
N-Type Sensor Results – NSS 2010



J. Wright et al, NSS presentation, 2010.

- scribe at 100 um from the guard ring.
- front-side scribe seems to be preferential to back-side one.
- lower laser power is preferential.

SiO_2 – Si Interface Charges



"*Origin*" of excellent passivation for **n-type Si:**

-Thermally grown oxides typically have from ~ 10^{10} to 1-2x10^{11} **positive** charges per cm^2, localized within about 35 Å of the Si/SiO_2 interface [Silicon Processing for the VLSI Era (Vol I), S. Wolf and R. Tauber, Lattice Press 1986, p. 223].

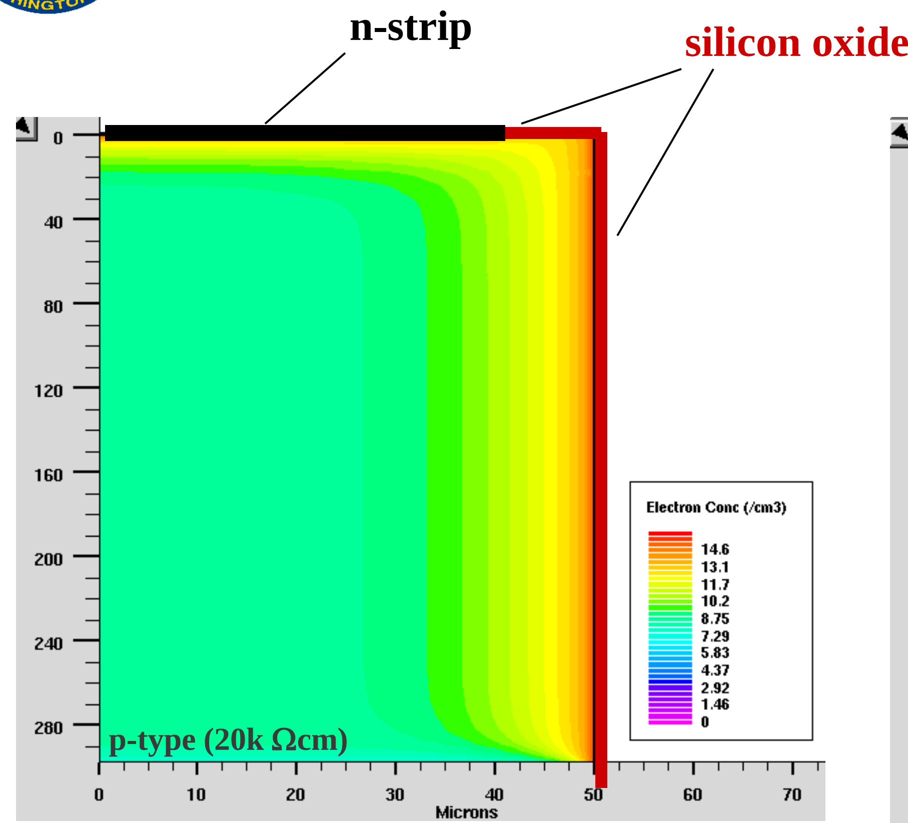
- surface recombination rate: FZ n-type Si (10 Ωcm): ~ 60 cm/s

Introduction - ALD

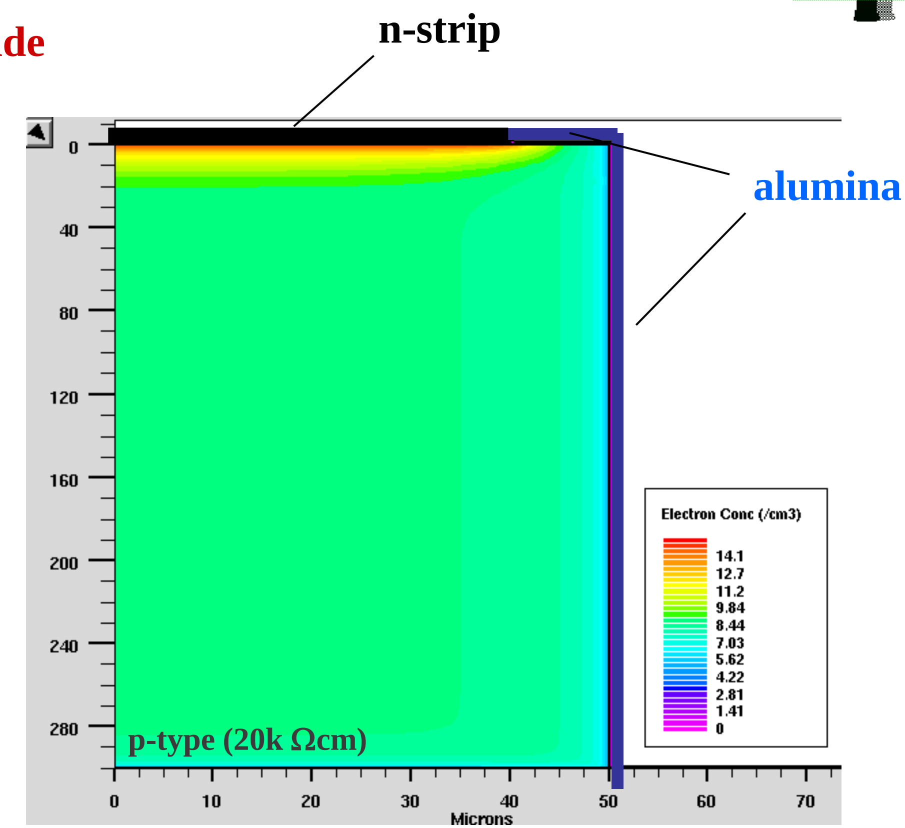
- Similar in chemistry to CVD (chemical vapor deposition), except that the ALD (**atomic layer deposition**) reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction.
- ALD film growth is **self-limited and based on surface reactions**, which makes achieving atomic scale deposition control possible.
- Perfect 3-D conformality, 100% step coverage: uniform coatings on flat, inside porous and around particle samples.

- **Origin of negative interface charge**: Functional surface groups on the silicon wafer are not optimal for an adsorption of the TMA (trimethylaluminium) precursor molecules, which leads to an incomplete reaction of the TMA and, consequently, an increased relative oxygen concentration at the interface (F. Werner et al., 25th European Photovoltaic Solar Energy Conference, Valencia, Spain, 6-10 September 2010).

Equilibrium Electron-Concentrations for SiO_2 and Al_2O_3



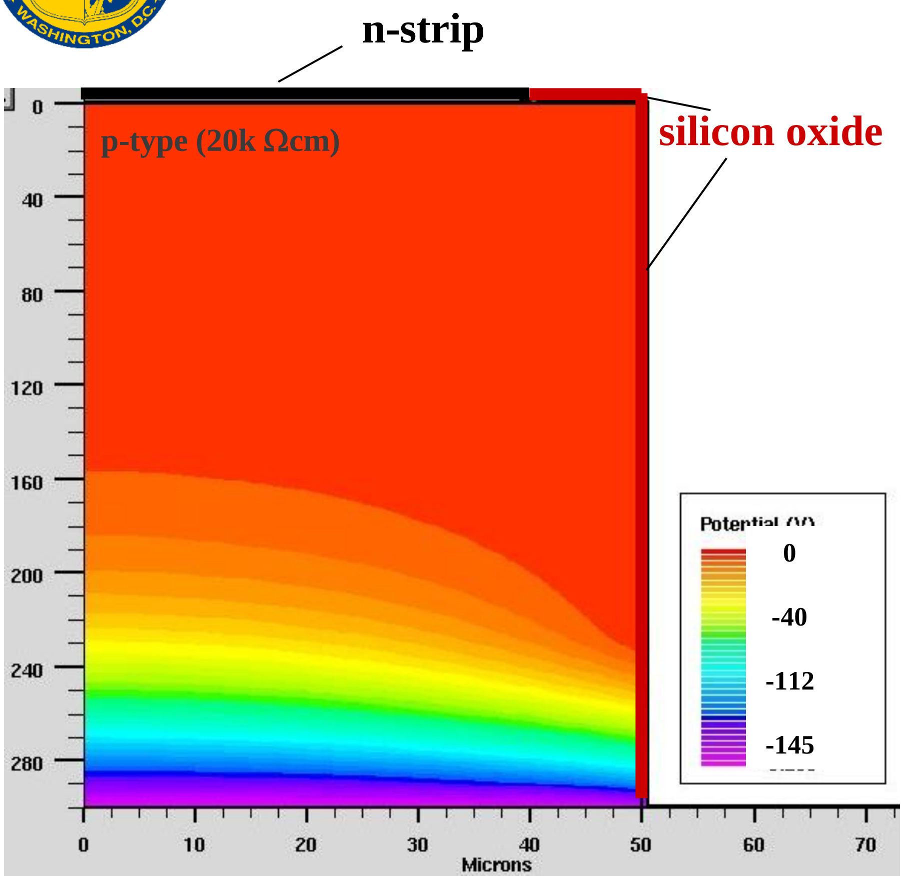
Positive charge (+1E11 cm^{-2}), no bias (V=0)



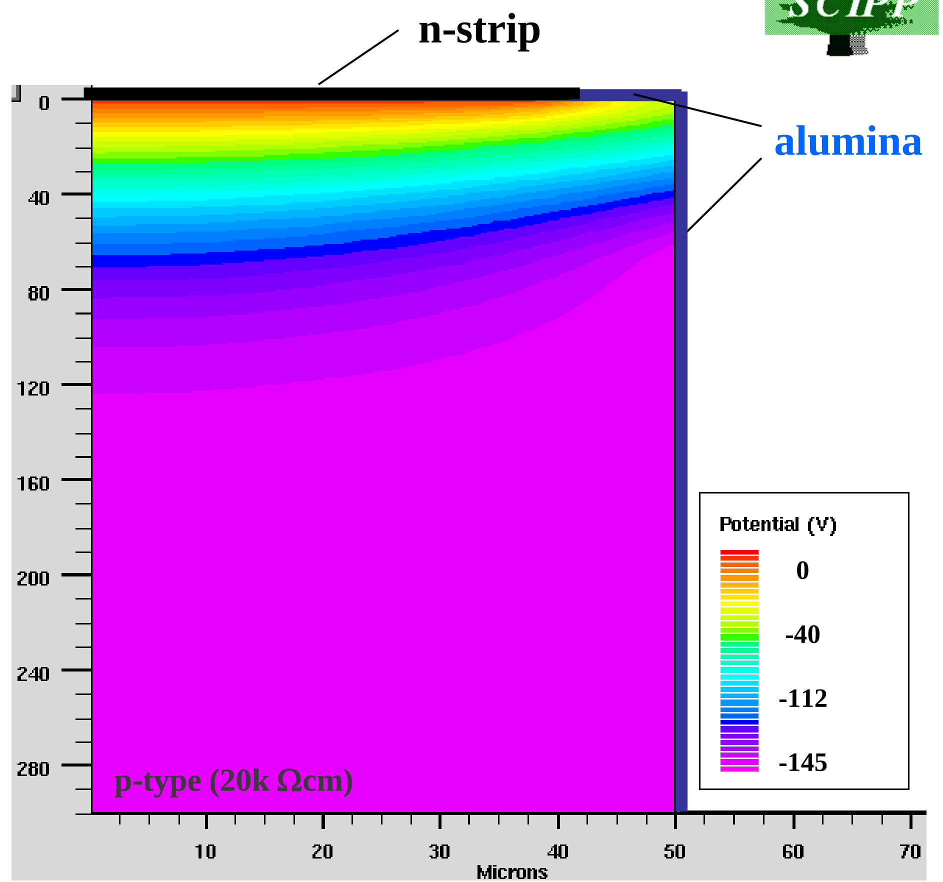
Negative charge (-1E11 cm^{-2}), no bias (V=0)

- silicon oxide → electrons path from n-strip to sidewall
- alumina → electrons "pushed away" from sidewall

Potential Distributions for SiO_2 and Al_2O_3 Passivation



Positive charge (+1E11 cm^{-2})

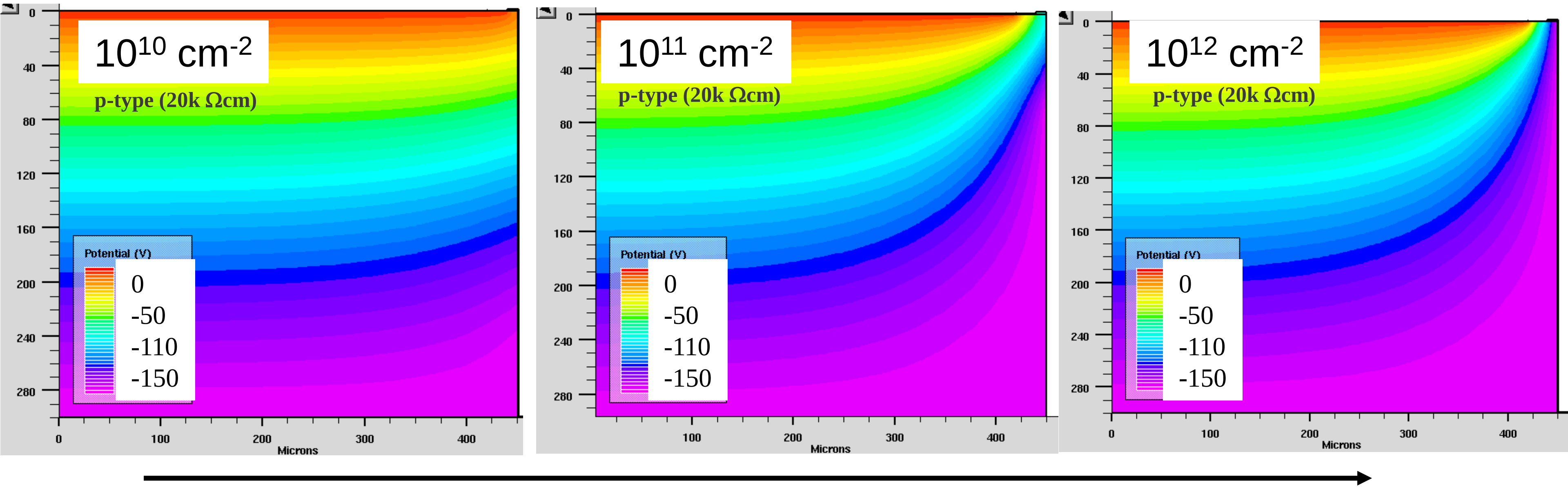


Negative charge (-1E11 cm^{-2})

Oxide passivation leads to:
- high electric field at trench edge,
- no control potential drop towards the cut edge

Alumina passivation leads to:
- high electric field strip edge,
- partially controlled potential drop towards the cut edge.

Influence of Surface Charge Concentration: P-Si/Al_2O_3

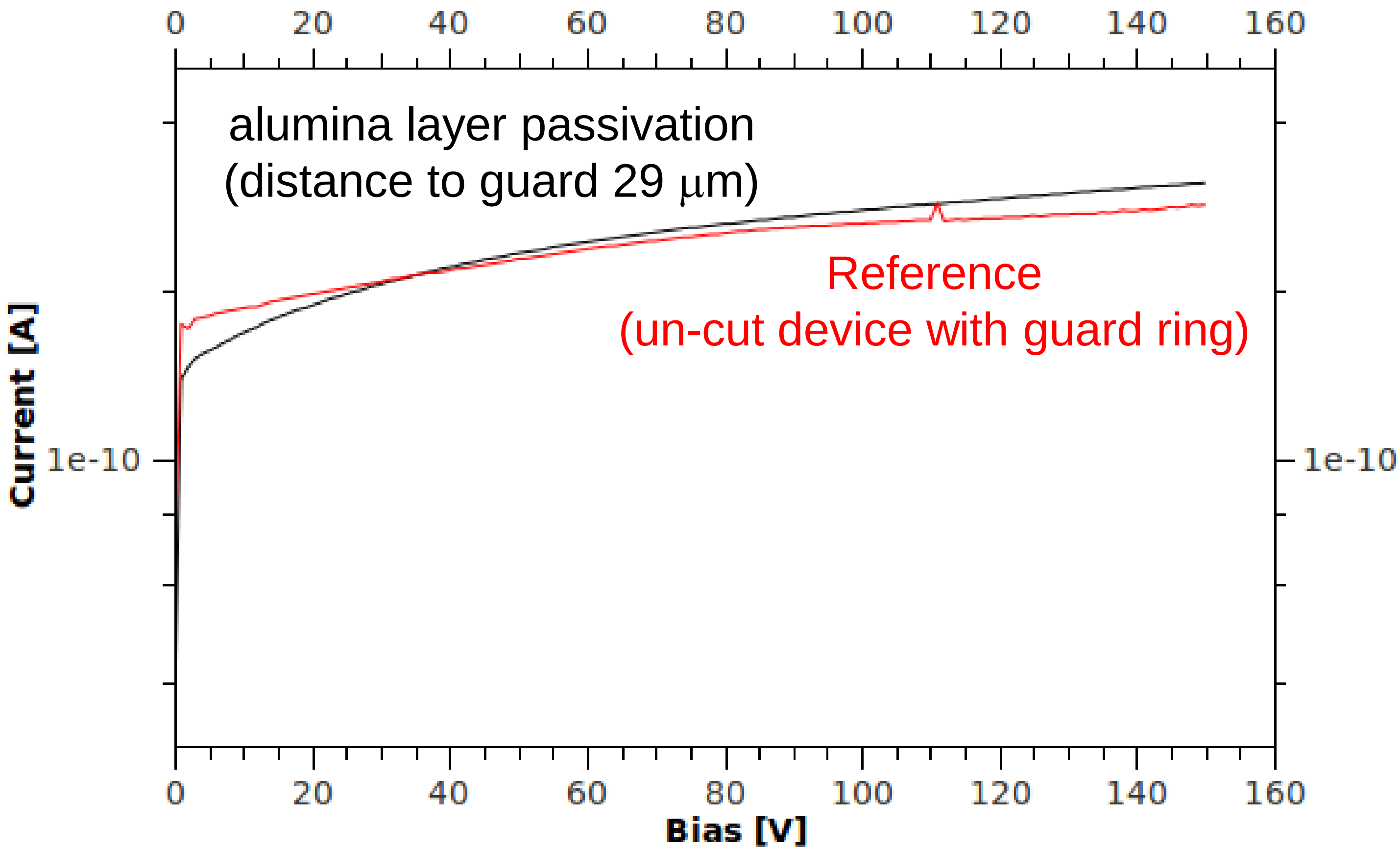


increasing negative surface charge

Typical literature values for alumina are ~ $10^{11} – 10^{13}$ cm^{-2} depending on deposition conditions. BUT most research is focused on increasing (*not decreasing*) surface charge.

The potential drop at edge depends strongly on surface charge density.

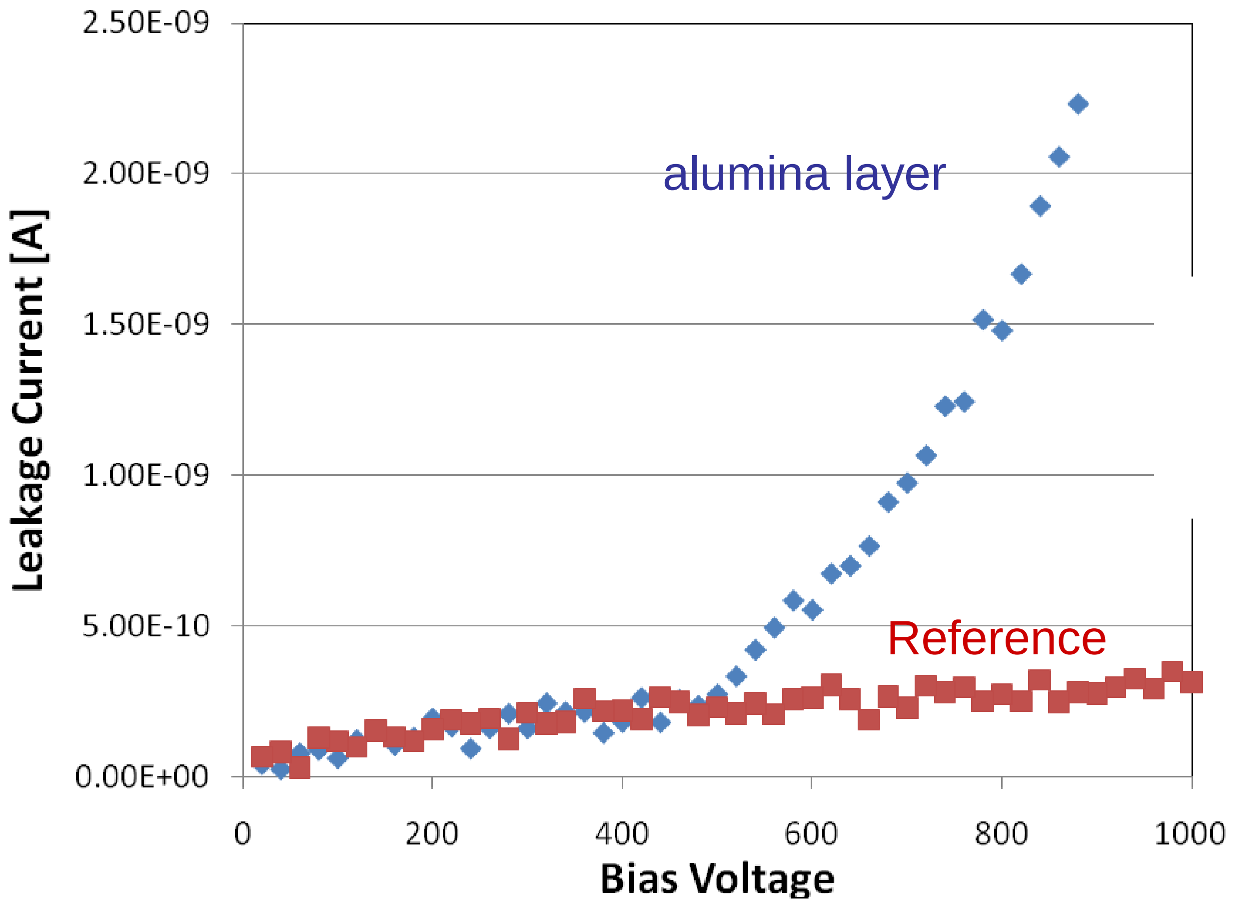
ALD Alumina Passivation for P-Type Silicon



Leakage for sample with Al_2O_3 passivation comparable to un-cut device with full guard ring structure.

Device I (HPK)

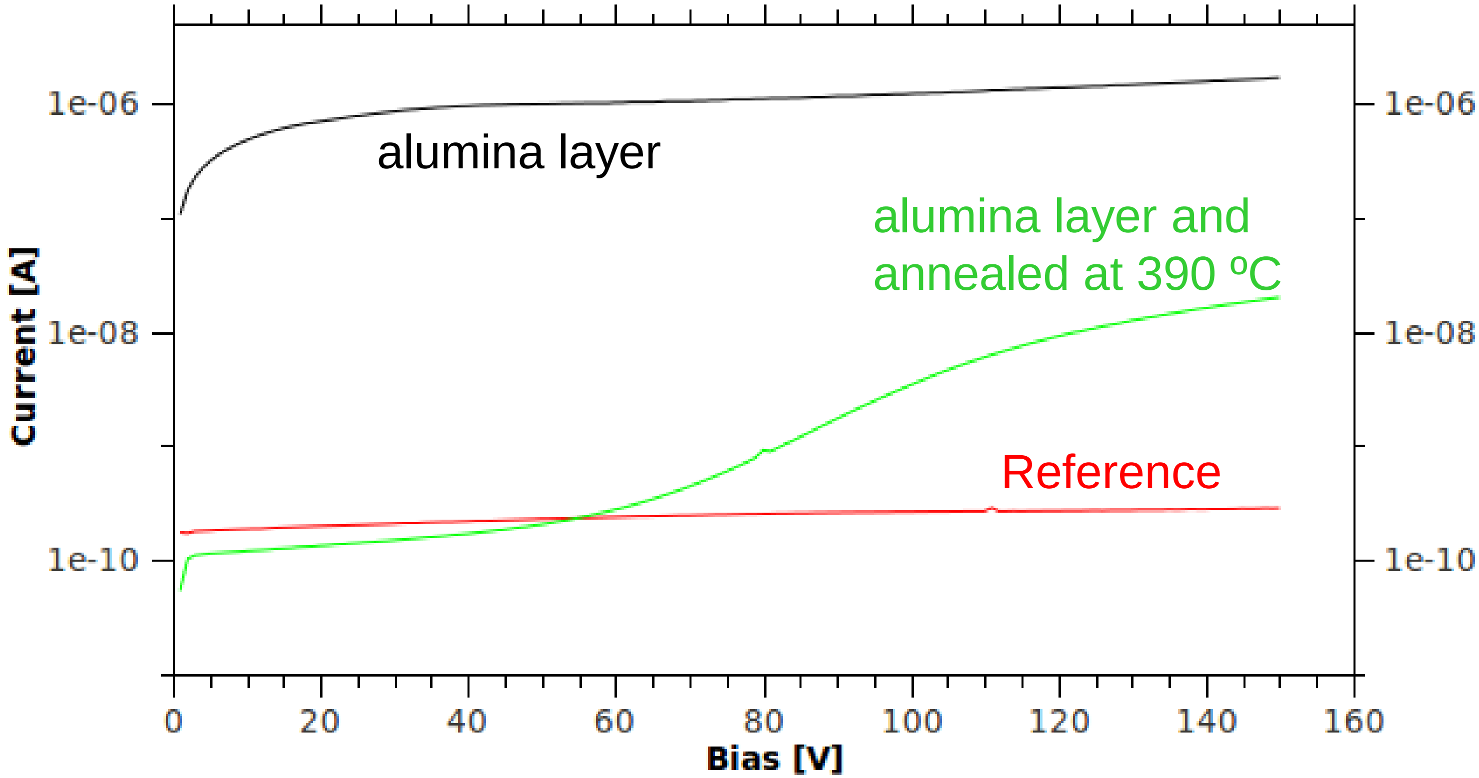
Low Leakage Currents up to 1,000 V



Leakage is low for voltages up to 1,000 V.

Device II (HPK)

Effect of Annealing and Native Oxide

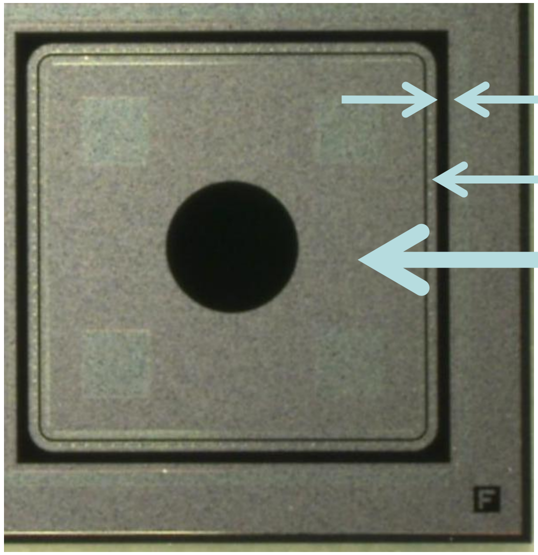


- annealing of alumina layer reduces leakage current (same effect as seen for solar cells, see slide #14).
- formation of native oxide (wrong surface charge) ↑ leakage current.
- native oxide forms rapidly (within seconds/minutes) in air.
- native oxide: ~ 2 nm thick, high charge trap density.

Device III (HPK)

Devices I-IV: HPK Samples

- Using a pad diode from HPK test structure meant to provide control over key sensor parameters for ATLAS07 sensors (*).
- It features a classic HPK single-guard ring design.
- Simple DC-coupled n-on-p pad. Vdepl ~ 180 V. Thickness 320 um.



(*) ATLAS07 strip sensors have been developed for ATLAS tracker upgrade for higher luminosity. They served as test vehicle for inter-strip isolation, punch-through protection, and other studies.

References:

Y. Unno et al., “Development of n-on-p silicon sensors for very high radiation environments”, NIM A, doi:10.1016/j.nima.2010.04.080 .

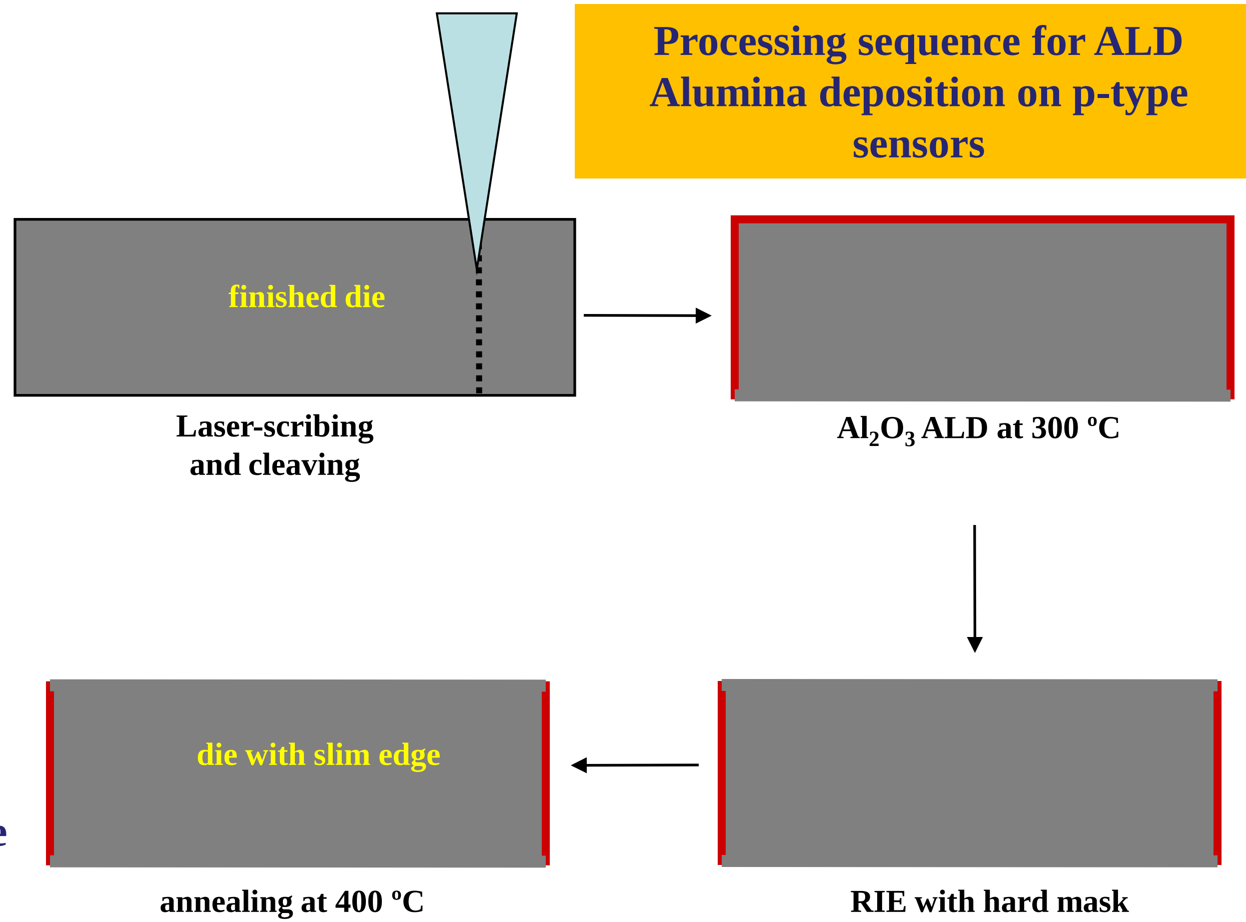
S. Lindgren et al., “Testing of surface properties pre-rad and post-rad of n-in-p silicon sensors for very high radiation environment”, NIM A, doi:10.1016/j.nima.2010.04.094 .

J. Bohm et al., “Evaluation of the bulk and strip characteristics of large area *n*-in-*p* silicon sensors intended for a very high radiation environment “, NIM A, doi:10.1016/j.nima.2010.04.093 .

Treatment Sequence

There are three key steps of the process:
1) Scribing on front-side
2) Cleaving, which leaves the surface with low defect density
3) Surface passivation to make the sidewall resistive.

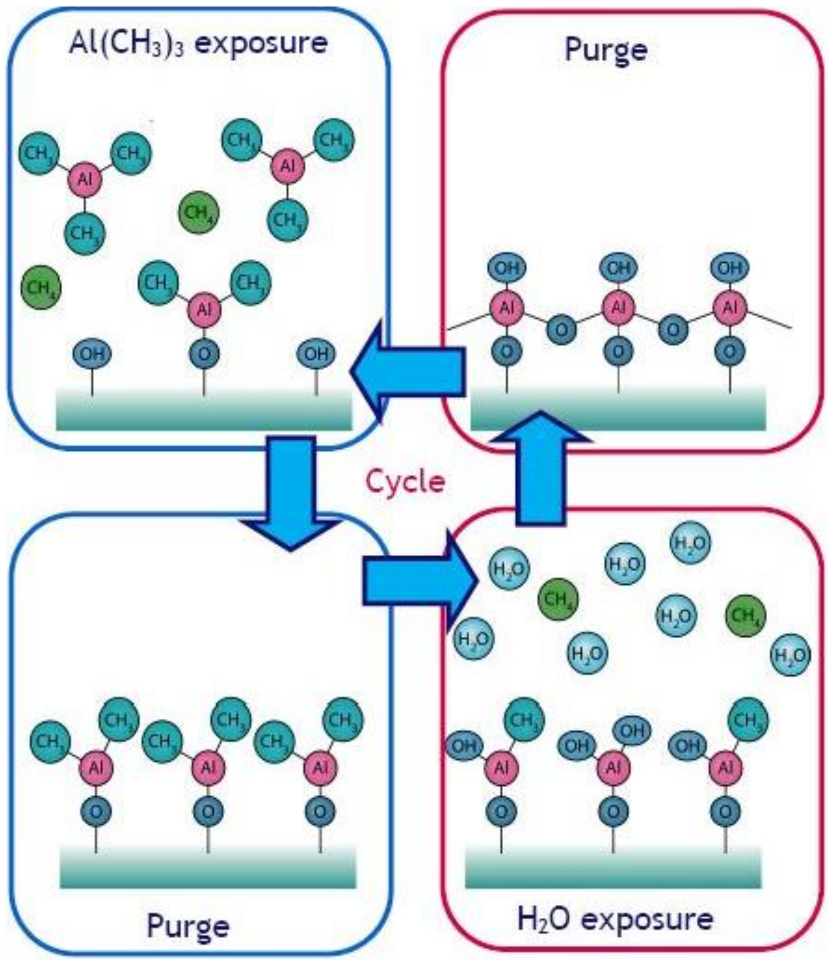
N- and p-type devices require different passivation technologies:
○ For n-type devices one needs a passivation with positive interface charge. Silicon Oxide SiO_2 layer works well, Silicon Nitrite Si_3N_4 layer works even better.
○ For p-type material a passivation with negative interface charge is necessary. We found that ALD with Alumina Al_2O_3 works in this case.



U.S. Naval Research Laboratory's FlexAL®

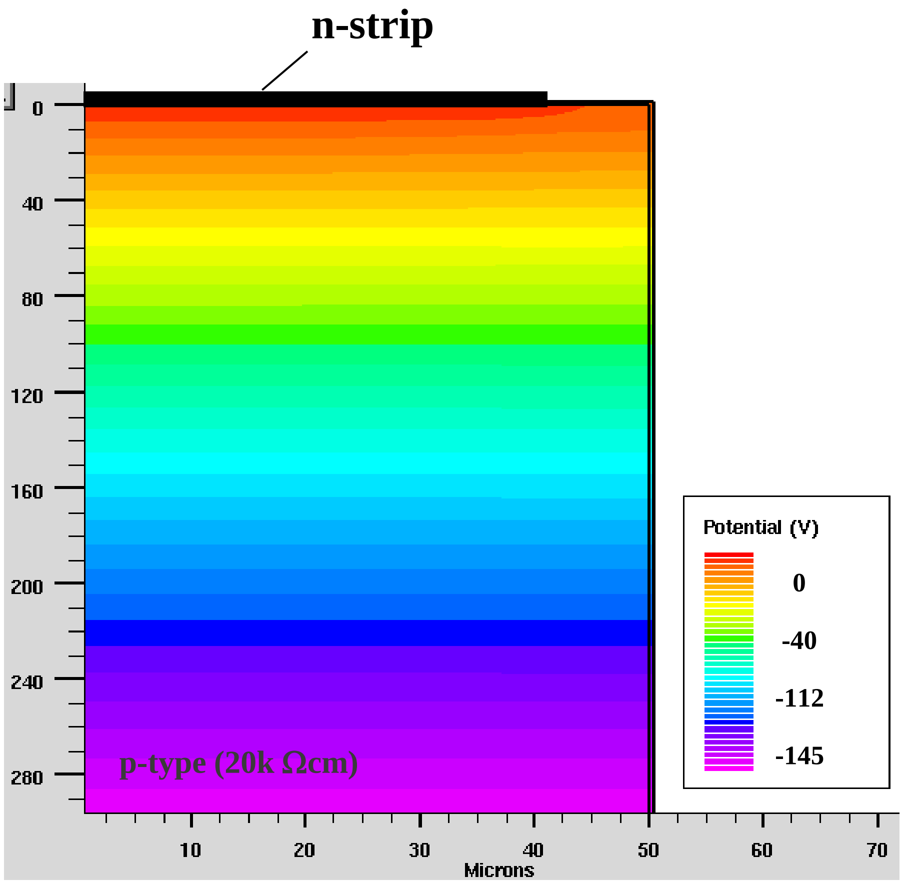
- FlexAL® from Oxford Instruments.
- plasma & thermal ALD in one flexible tool.
- stage temperature: 100 – 400 ºC.
- installed at NRL's Nanoscience Institute.

Alumina ALD Deposition Cycle



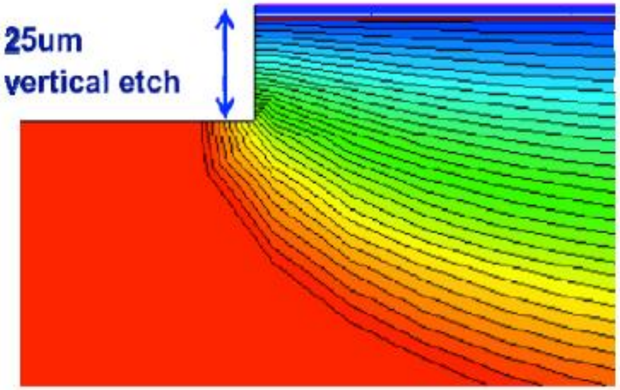
ALD Growth of Al_2O_3 from $Al(CH_3)_3$ and H_2O

Potential Distribution Without Surface Charge

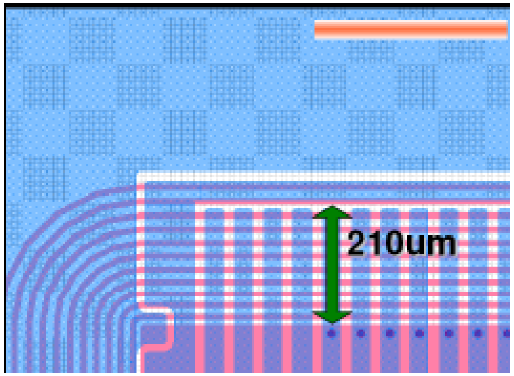


Not considering surface charges leads to *wrong* potential distribution at sidewall.

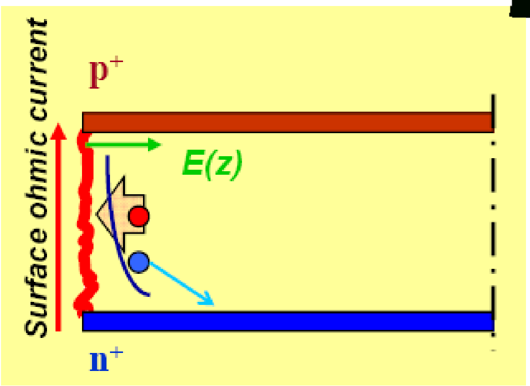
Slim Edges - Approaches



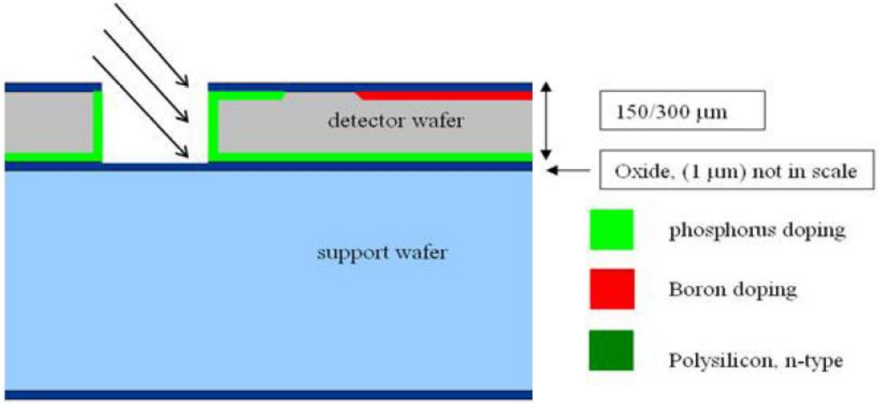
J. D. Segal, et al., NSS 2010



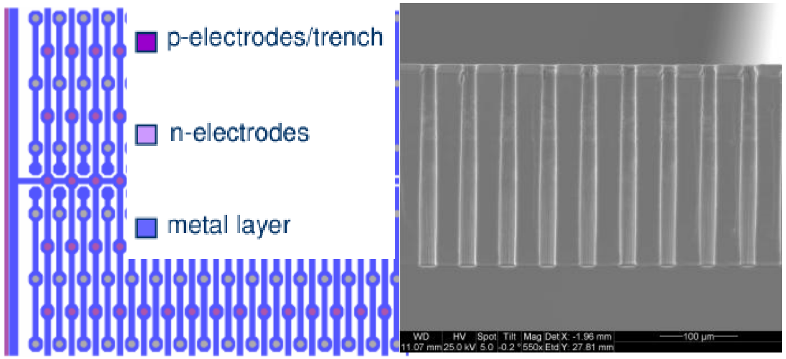
A. Rummler et al., 2010



E. Verbitskaya et al., 13 RD 50 workshop, 2008



J. Kalliopuska, NSS 2010



T.-E. Hansen et al., 2009

Goal of our research:
- **slim edges with finished devices on die level**
- **slim edges on p- and n-type devices**