POCPA3 – DESY, May 21-23, 2012

Elettra digital control PS

Bipolar digital control 30 A – 20 V PS

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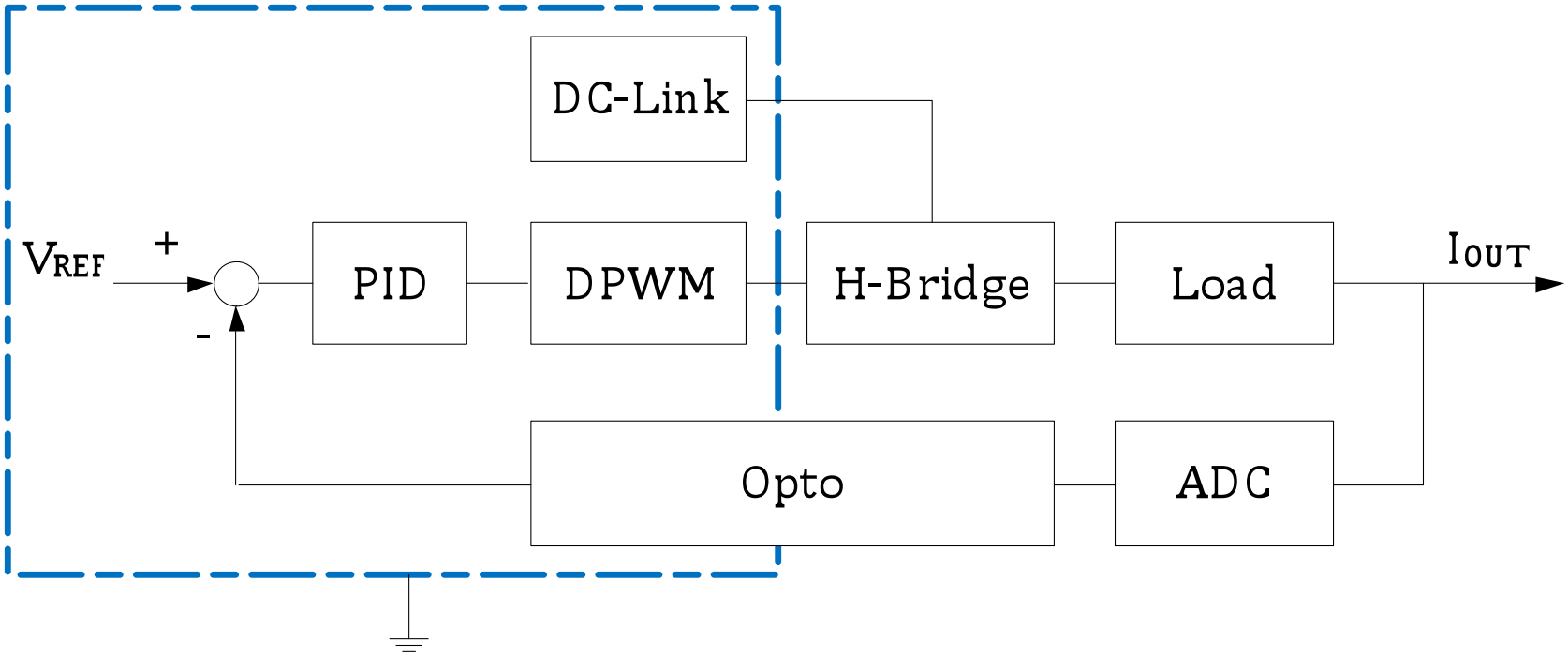
- Fermi@Elettra low current PS requirements
- Why digital?
- Resolution & Limit cycles
- DPWM Resolution
- H-Bridge Toggle Technique
- ADC Synchronization
- Fermi@Elettra 20 A and 5 A PS
- INFN Frascati, SPARC PS
- Conclusion & Consideration

Fermi@Elettra's PS requirements

- Four-quadrant: ±5 A, ±10 V and ±20 A, ±20 V
- Max Ripple: 30 ppm/FS
- Long term stability (8h): ±50 ppm/FS
- Standard Ethernet interface
- Output current resolution: 16 bit
- Current set point update rate: 50 Hz (for feedback)
- Load range: 0.5 – 2 Ω and 0.5 – 400 mH
- Number of channels: more than 300

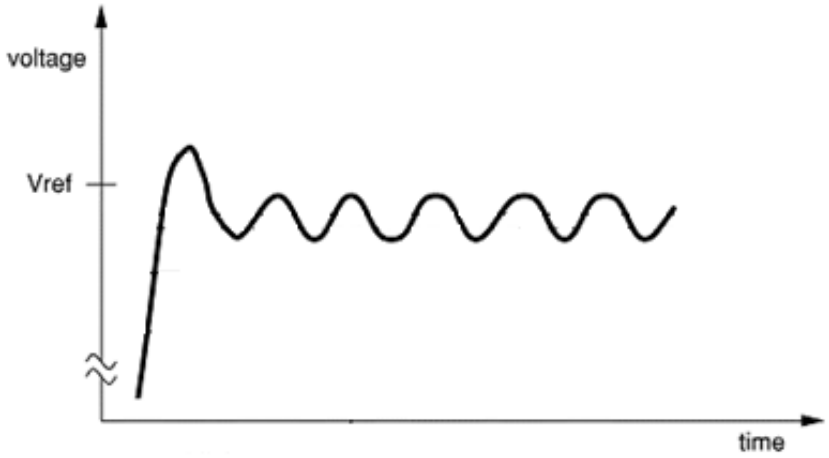
Why digital?

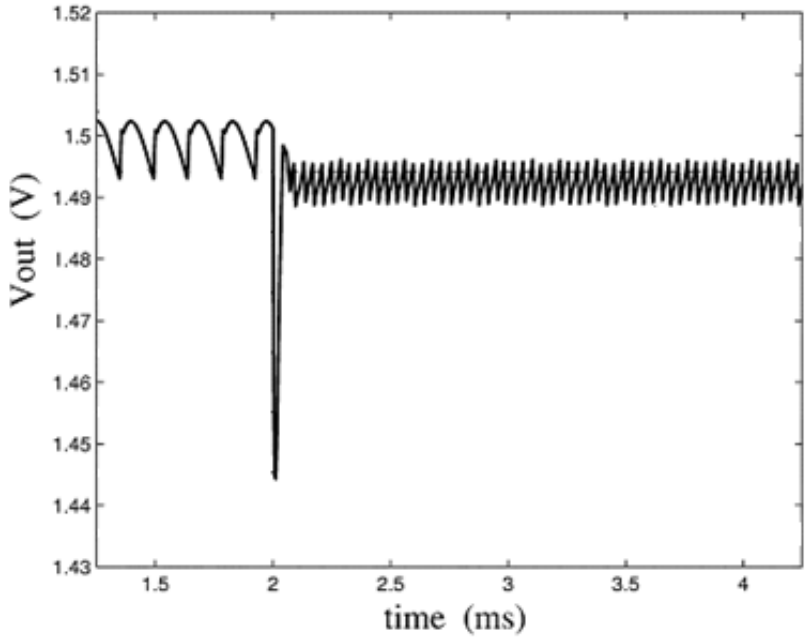
- Easy of PID modification (wide load range for the same current range)
- Step response optimization for all PS-magnet combination.
- Galvanic isolation between current sensor and control electronics



Resolution & Limit Cycles

Digital controls are affected by limit cycles





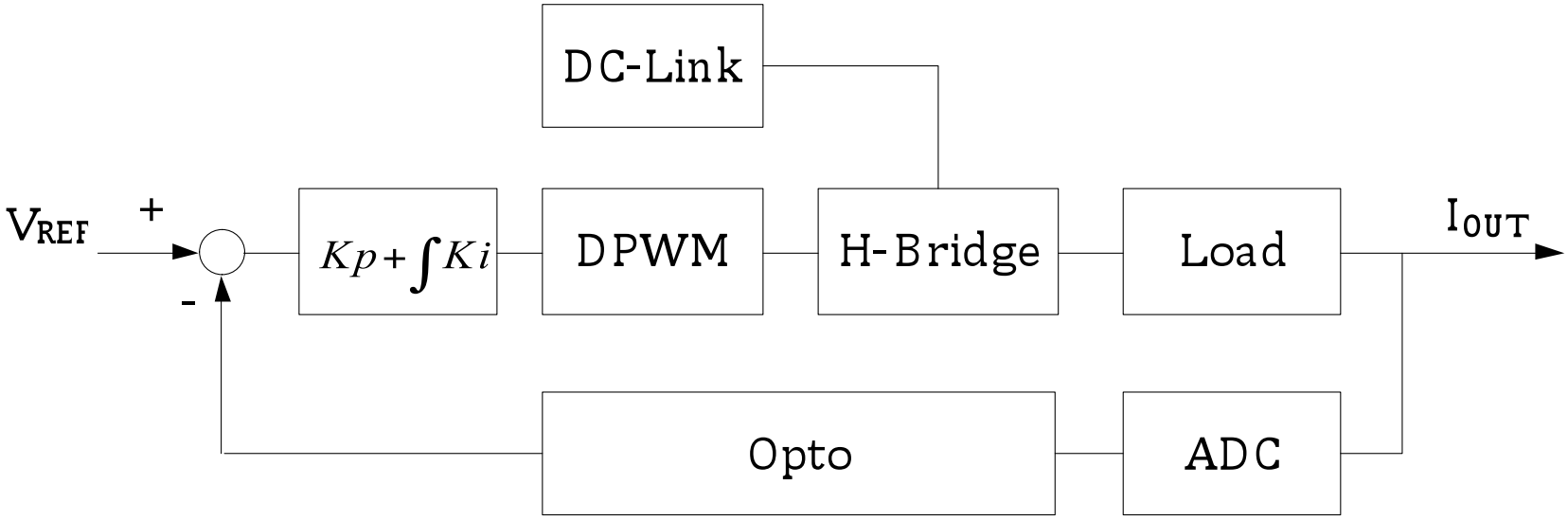
Resolution & Limit Cycles

Three conditions are required to avoid Limit Cycles[1]

- Output min step < reading min step
  (i.e. output resolution > reading resolution)
- 0 < Integral Gain (Ki) < 1
- Loop stability (with ADC gain)

Hardware

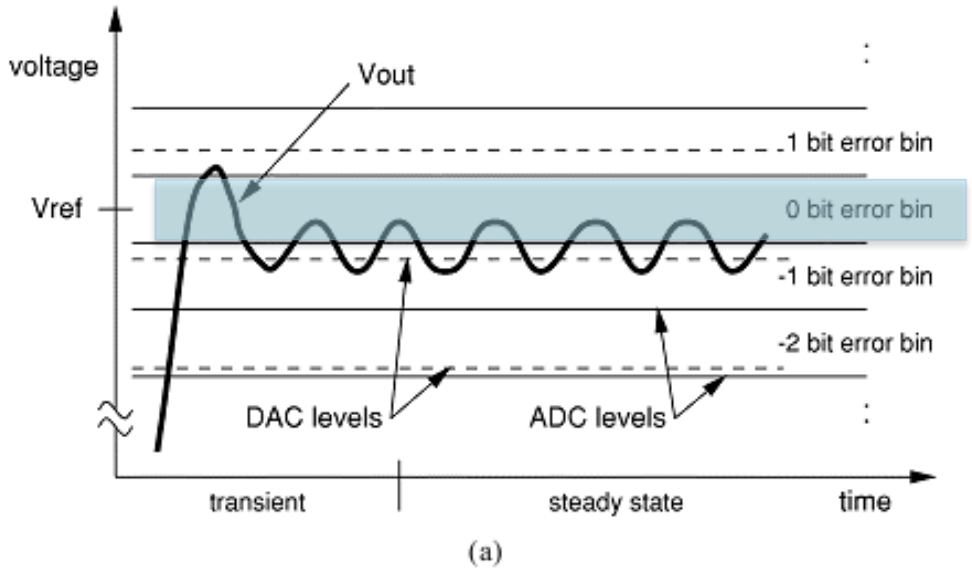
PID parameters



[1] A.V. Peterchev, S.R. Sanders: Quantization resolution and limit cycling in digitally controlled PWM converters IEEE Transaction on Power Electronics, Volume 18, Issue 1, Part 2, Jan. 2003, pp. 301-308

Resolution & Limit Cycles

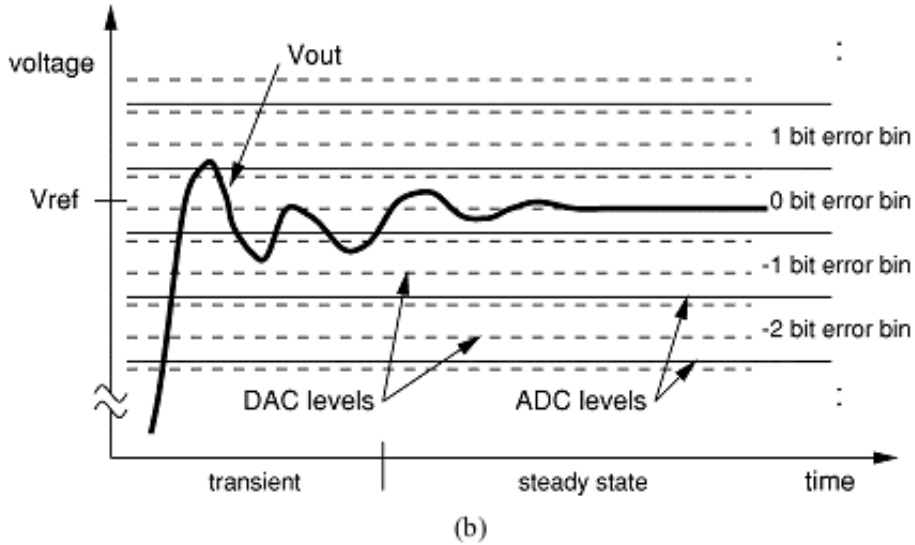
When output min step **>** reading min step →



Limit cycles

Resolution & Limit Cycles

When output min step < reading min step →



Stady state stable

Resolution & Limit Cycles

Output min step (H-Bridge):

$$Iout_{MIN-STEP} = \frac{2 \cdot V_{DC-Link}}{R_{LOAD} \cdot \left(2^{DPWM-RES} - 1\right)}$$

Reading min step:

$$Iread_{MIN-STEP} = \frac{Iout_{RANGE}}{2^{ADC-RES}}$$

Example (±5A PS):

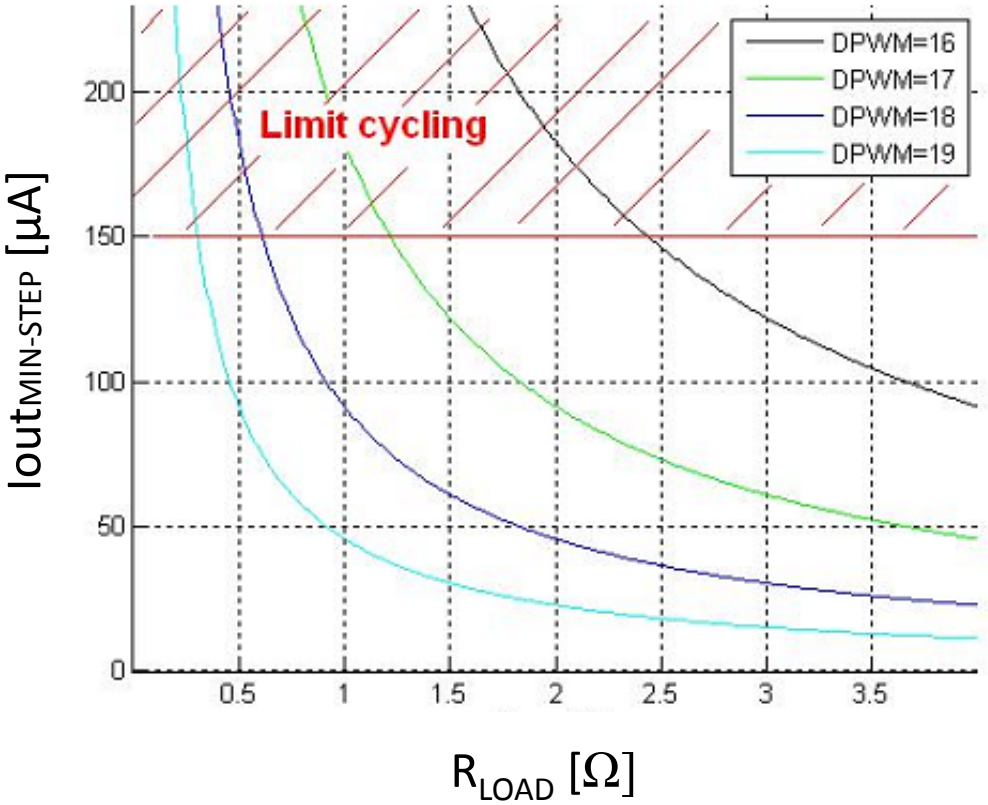
$V_{DC\text{-}Link}$ = 12 V

$Iout_{RANGE}$ = 10 A

ADC-RES = 16 bit

Resolution & Limit Cycles

Limit cycle condition for $V_{DC\text{-}Link}$= 12 V, $Iout_{RANGE}$ = 10 A and ADC-RES = 16 bit



$$I_{ADC-RES} = \frac{10}{2^{16}} = 153\ \mu A$$

Due to wide range of resistive load a 19 bit of DPWM resolution is required

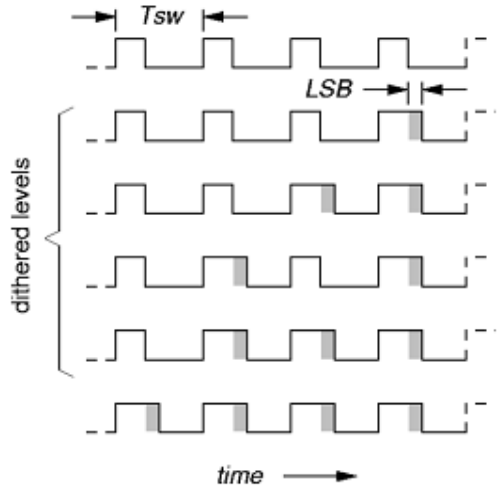
DPWM Resolution

- Delay-line DPWM has been used (TMS320F2808)

PWM Freq (kHz)	Regular Resolution (PWM)		High Resolution (HRPWM)	
	Bits	%	Bits	%
20	12.3	0.0	***18.1***	0.000
50	11.0	0.0	***16.8***	0.001
100	10.0	0.1	***15.8***	0.002

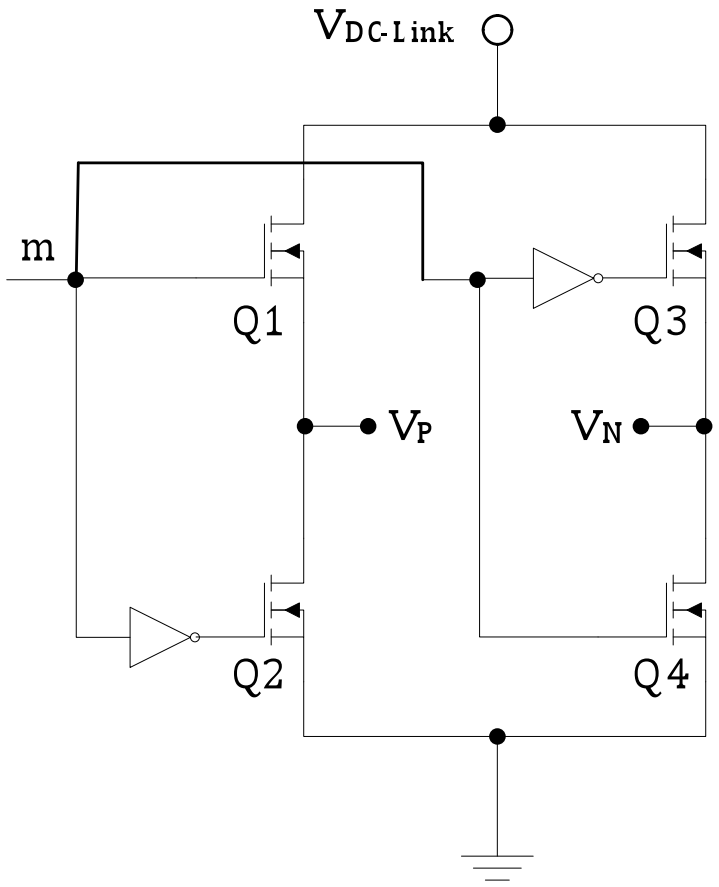
- Using 4 PWM cycles of dithering

  17.8 bit resolution has been achieved



H-Bridge Toggle Technique

- A further bit of resolution has been added by a Toggle Technique (Patent Pending) between the two legs of the H-Bridge.



$$m \in \{0,1\}$$

$$Iout = \frac{V_P - V_N}{R_{LOAD}} = \frac{(2m-1)\cdot V_{DC-Link}}{R_{LOAD}}$$

$$Iout_{MIN-STEP} = \frac{2 \cdot m_{LSB} \cdot V_{DC-Link}}{R_{LOAD}}$$

For instance with

$V_{DC\text{-}Link}$=12, R_{LOAD}=1 and $m_{LSB}=1/2^{17.8}$

$$Iout_{MIN-STEP} = 105\ \mu A$$

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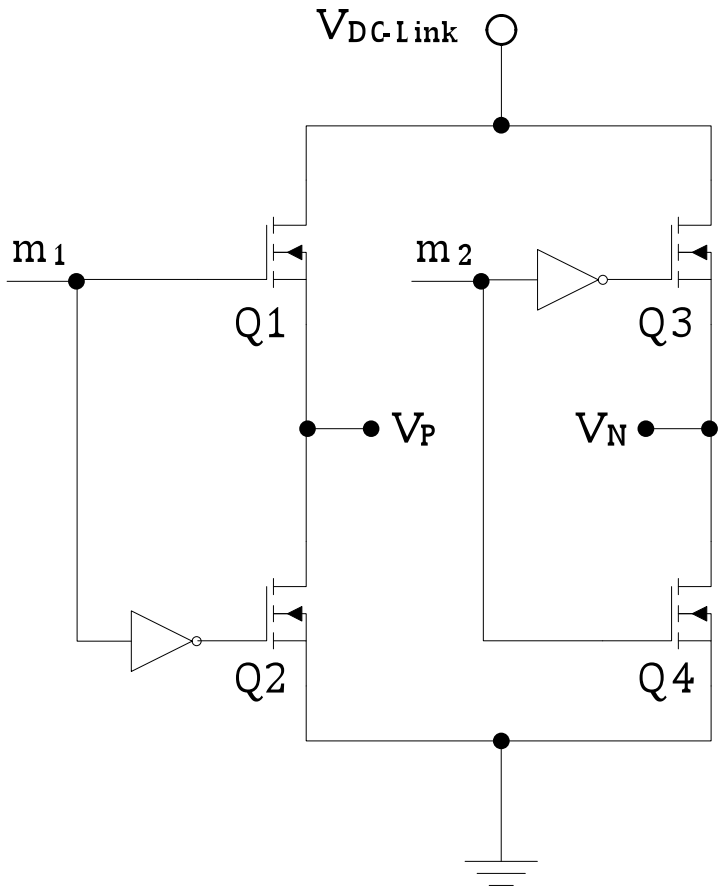


$$For: m_1 \neq m_2$$

$$Iout = V_P - V_N = \frac{(m_1 + m_2 - 1)\cdot V_{DC-Link}}{R_{LOAD}}$$

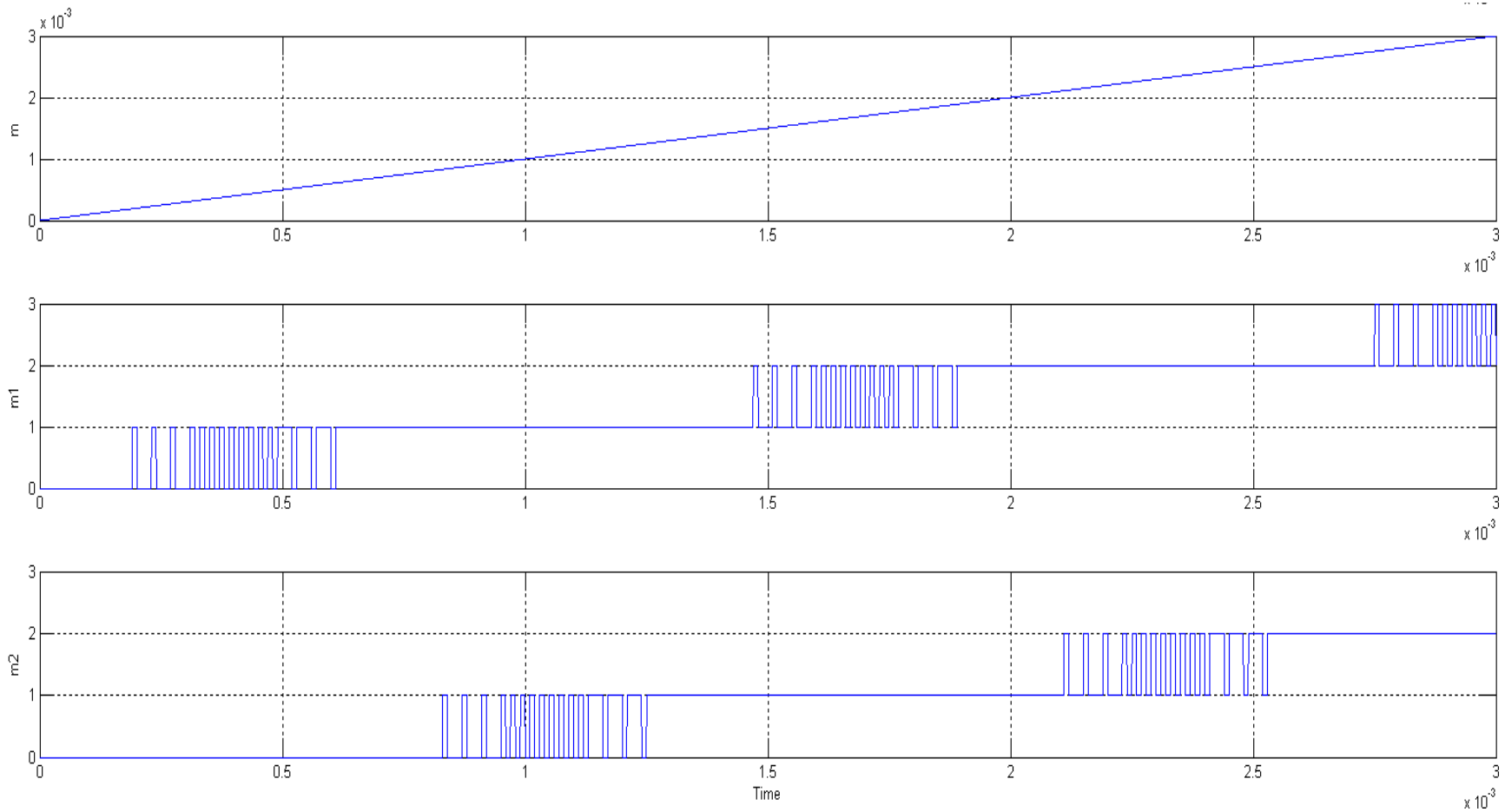
$$Iout_{MIN-STEP} = \frac{m_{LSB} \cdot V_{DC-Link}}{R_{LOAD}}$$

Keeping m_1 constant, varying m_2 (or vice versa)
$V_{DC\text{-}Link}$=12, R_{LOAD}=1 and $m_{LSB}=1/2^{17.8}$

$$Iout_{MIN-STEP} = 52.5\ \mu A$$

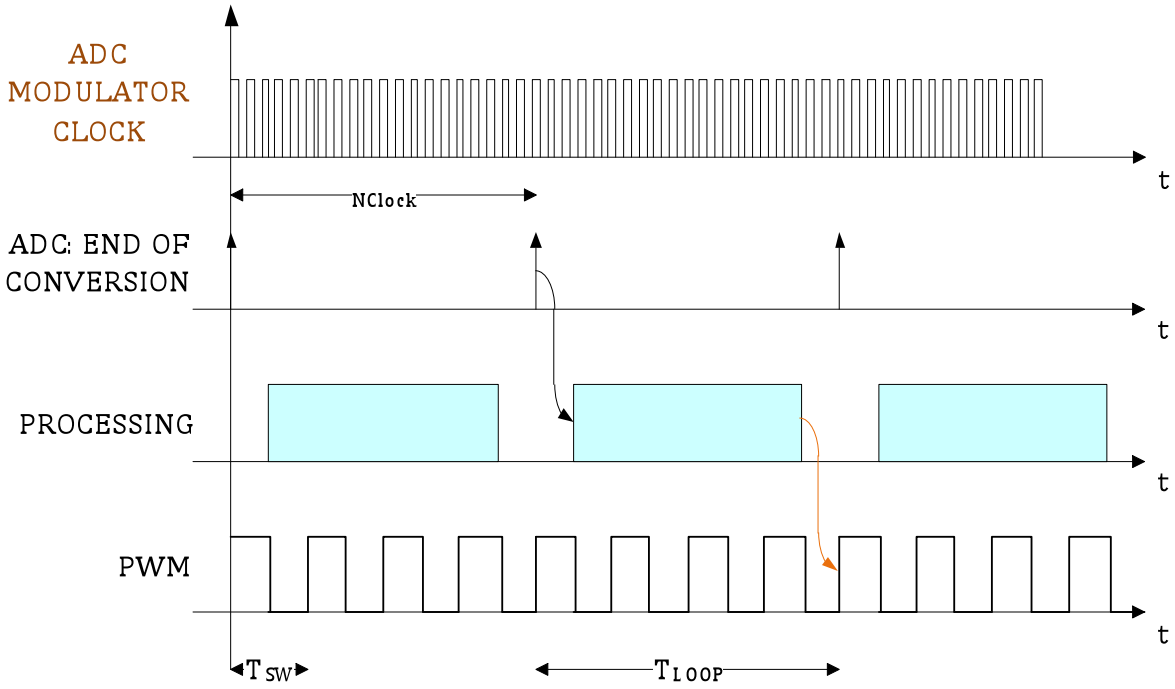
H-Bridge Toggle Technique

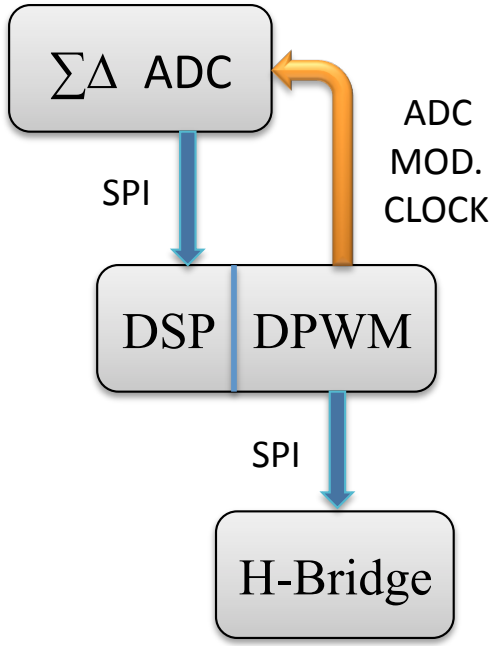
- Example of Toggle Technique with 2 bit of dithering.



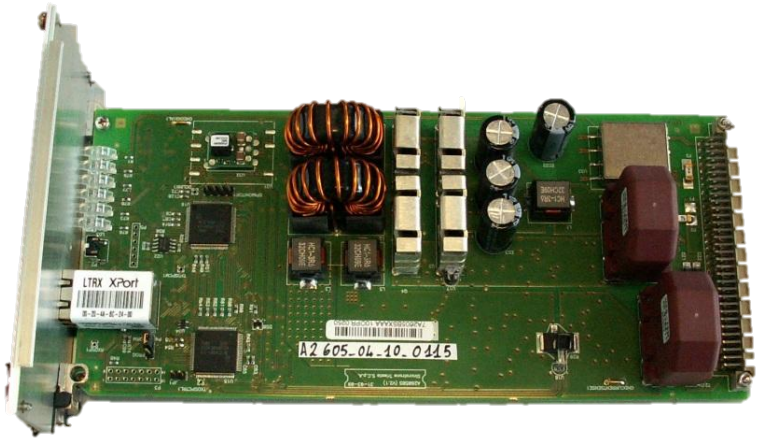
ADC Synchronization

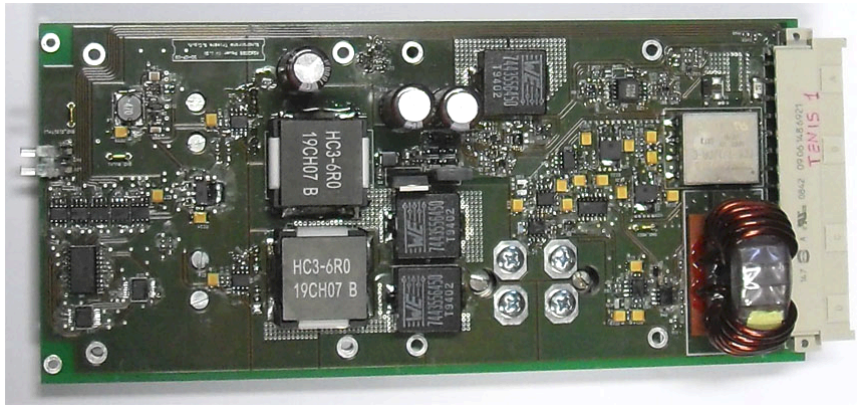
- ∑Δ converter has been used (ADS1252: 24 bit, SPI, SOIC 8 package)
- Problem: ADC hasn't a start of conversion

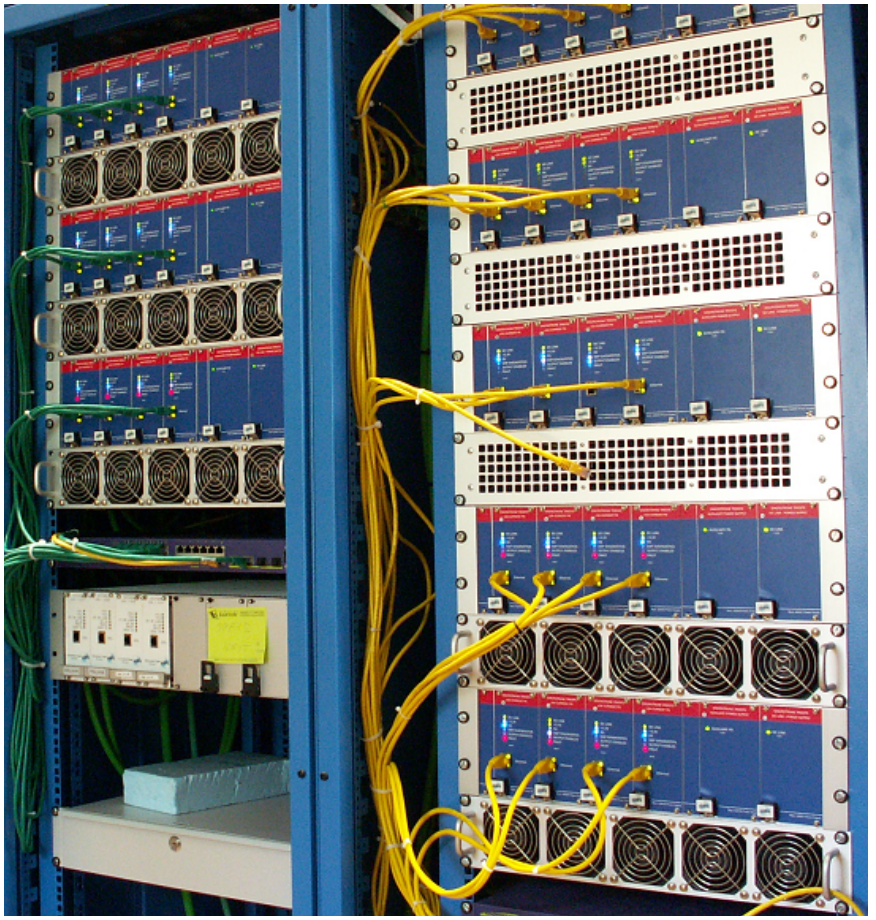




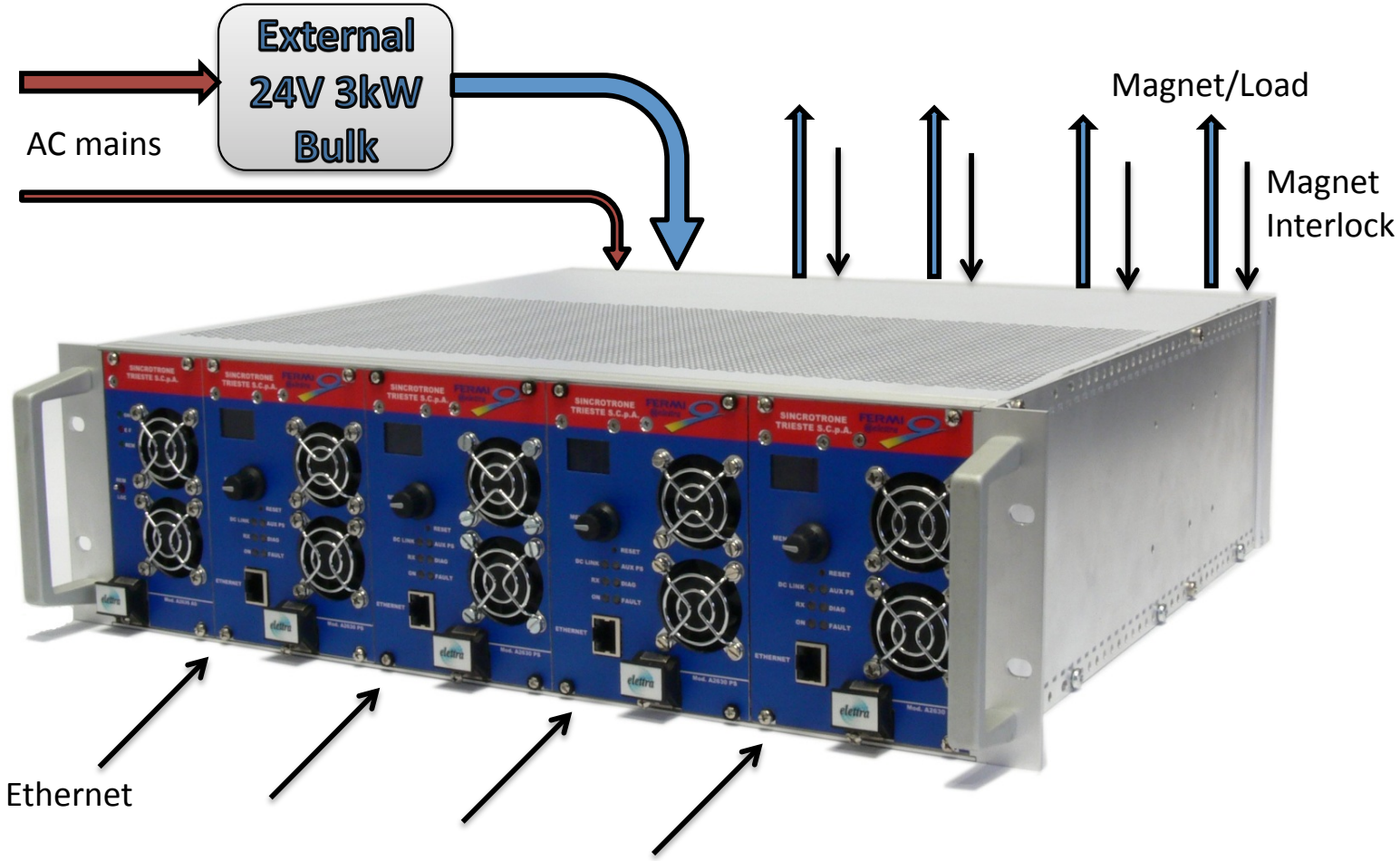
Fermi@Elettra 5A and 20A PS



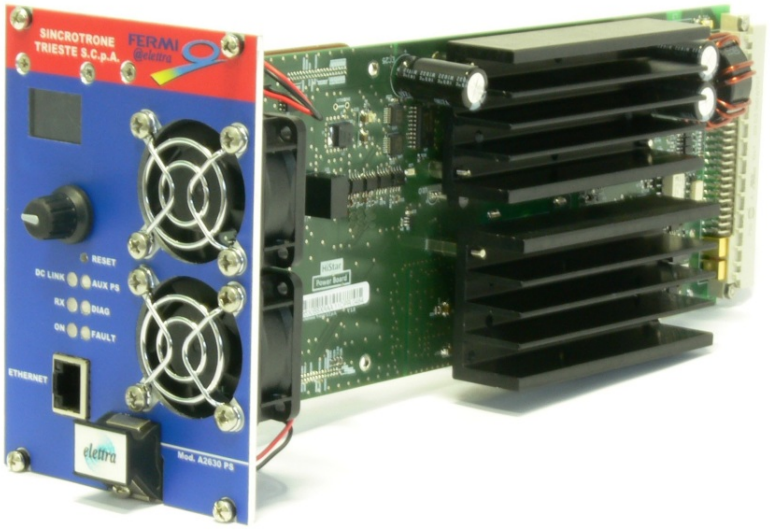




INFN Frascati - SPARC 30A PS



INFN Frascati - SPARC 30A PS



Output Current	**± 30 A**
Output Voltage	**± 20 V**
Output Current Resolution	**16 bit**
Output Current Ripple	**30 ppm / FS**
Output Current Stability	**50 ppm / FS**
DC/DC efficiency (full load)	**95%**
Switching frequency	**104 kHz**
Close Loop Bandwidth	**1,5 kHz**
Accuracy	**0.05 %**
Max set point update rate	**300 Hz**

INFN Frascati - SPARC 30A PS

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Close Loop Bandwidth	1,5 kHz
Accuracy	0.05 %
Max set point update rate	300 Hz

Local Control / Monitor	Graphic Color Display, 6 LEDs and Encoder
Extra-Features	Hot-Swap Point-by-Point Current Waveform Loading User-definable interlock thresholds, active levels and timings Remote Updates
Auxiliary ADC	DC Link Voltage Ground Leakage Current MOSFETs Temperature Shunt Temperature
Hardware protection	Input Fuses Earth Fuse Over-Voltage
Internal Interlocks	DC Link Under-Voltage MOSFETs Over-Temperature Shunt Over-Temperature Over-Current Over-Voltage Earth Fault Current Regulation Fault Excessive Current Ripple
External Interlocks	8 Inputs: "dry" contacts 3 Outputs: relay-type
Cooling	Self-Regulated Fans

Conclusion & Consideration

•Digital control is very useful for standardize different range of PS

•Simplifies the additions of extra features (communication, waveforms...)

BUT

•Requires digital hardware and software experts for development and modifications

•Introduces electronic components not easy to repair-replace (FPGA)

SO

•Could we roll back to the old and simple POWER SUPPLY and not waveform generator with OLED display, please?

That's all Folks!

Thank You