Session Program

29 June 2026 to 3 July 2026

5th DRD3 week on Solid State Detectors R&D

WG1 (WP1)

Institute of Space Science & National Institute of Materials Physics
National Institute of Statistics

Wednesday 1 July

10:30

WG1 (WP1): CMOS technologies

Session |
Location: Institute of Space Science & National Institute of Materials Physics, National Institute of Statistics

10:30–10:40 **Introduction to WG1/WP1 sessions**

Speakers
Eva Vilella Figueras, Heinz Pernegger, Jerome Baudot

10:40–10:55
Latest TCAD Results for the Optimization of Internal-Gain CACTUS Sensors in the 150 nm LFoundry Process

Speaker
Juan Ignacio Drovandi

11:03–11:18 **A fully digital TDC for the CACTUS monolithic timing detector**

Speaker
Raimon Casanova Mohr

11:26–11:41
Recent Testbeam Results of MiniCACTUSV2 and Novel Gain-Layer Sensor Prototypes

Speaker
Stefano Terzo

11:49–12:04
Infrared and 90Sr characterization of LFoundry 150 nm test structures with intrinsic gain for the Cactus development line

Speaker
Prof. Philippe Schwemling

12:12–12:27 **Recent results of the CASSIA project**

Speaker
Leena Diehl

12:35–12:50 **The MOSFET Gain Tuning Idea**

Speaker
Ioannis Kopsalis

13:00

Thursday 2 July

14:00

WG1 (WP1): CMOS technologies

Session |
Location: Institute of Space Science & National Institute of Materials Physics, National Institute of Statistics

14:00–14:15 **DMAPS for space applications**

Speaker
Haris Lambropoulos

14:25–14:40 **Monstera Large tracking detector volumes**

Speakers
Ingrid-Maria Gregor, Lennart Huth

14:50–15:05 **Development Status & Plans of Serial Powering at IHEP**

Speaker
Hui Zhang

15:15–15:30 **Early results with the asynchronous architecture of SPARC**

Speaker
Jerome Baudot

15:40–15:55 **Status of the MANTA project**

Speaker
Michael Deveaux

16:00–16:20 **Coffee break**

16:20–16:35 **Optimizing the MALTA3 readout design for the 65 nm TPSCo node.**

Speaker
Dumitru-Vlad Berlea

16:45–17:00 **Status update on OCTOPUS**

Speaker
Lennart Huth

17:10–17:25 **R&D program proposal focused on the SK hynix 90 nm CIS process for future vertex detector**

Speaker
Zhijun Liang

17:35–17:50 **Development of COFFEE, HVCMOS sensors using 55nm process**

Speaker
Yiming Li

17:55