Paul Scherrer Institut

Swiss Light Source BPM System & Upgrade Plans/Activities

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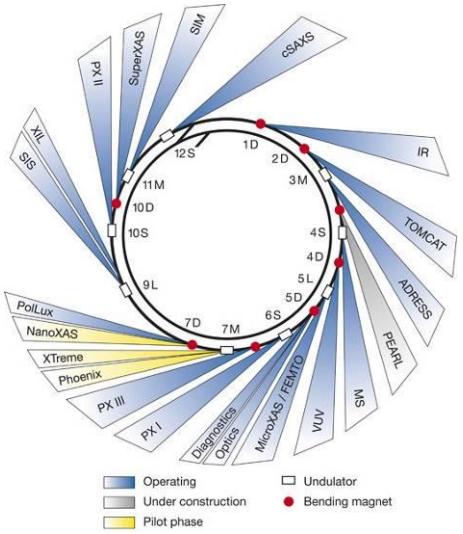
Contents

Introduction: SLS

- 2000: 1st Beam.
- 2001: User Operation.
- 400mA top-up, 2.4GeV, 500MHz.
- Ring: L=288m, f_{rev} ~ 1MHz.
- 2011: Start with developments for new BPM system.



Introduction: SLS (Cont'd)

SLS Features Affecting BPM Requirements

- Global Fast orbit feedback (FOFB):
  → Any drift & noise of BPM electronics & pickups immediately modulated onto beam (if within FB bandwidth & if no X-ray BPM feedback).

- Top-up operation: I=400mA ± ~1%
  → beam-current dependence of BPM less critical.

- Filling pattern feedback (keeps charge in bunches 0...N const.)
  → filling pattern dependence of BPMs less critical.

- X-Ray BPM feedbacks (correction ~ Hz, move FOFB ref. orbit)
  → Position drift of RF BPMs less critical.

Accelerator design & features important for orbit stability, not only pure BPM system performance.

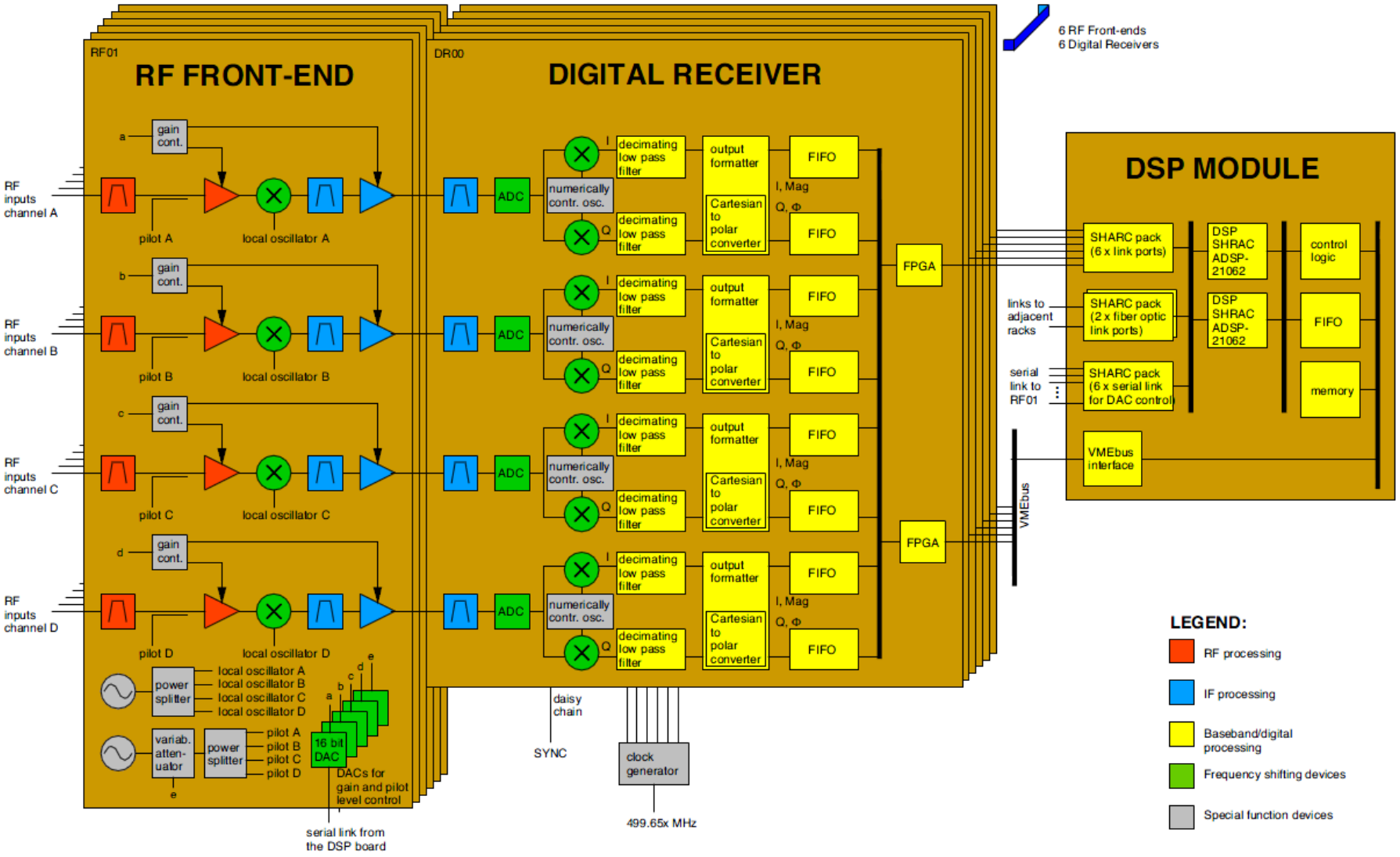
Contents

Present SLS BPM System

History & Status

- Same “DBPM” electronics for booster & ring (buttons), linac & transfer lines (resonant striplines). Licensed to I-Tech (=PSI spin-off), predecessor of Libera electron. 1st beam: 2000.
- Digitally programmable bandwidth & data rate (MHz ... Hz), using DDC ASICs (Intersil HSP50214B). Standard setting (ring):
  - tune BPM: 1MSPS / 0.5MHz BW
  - other BPMs: 4KSPS / 0.8kHz BW (FOFB)
- Annual failure rate: Dropped over the years, still at “bottom of bathtub” (year 2011: Highest SLS uptime ever ...). But: Want new system before this changes.
- Ring: 73BPMs. Booster: 54 BPMs (only few needed). No spare problem (yet). In-house maintenance.

Present SLS BPM System



Present SLS BPM System

RFFE

- Mix 4 500MHz button signal to 36MHz IF.
- Free-running LO.
- Pilot for initial calibration & test.

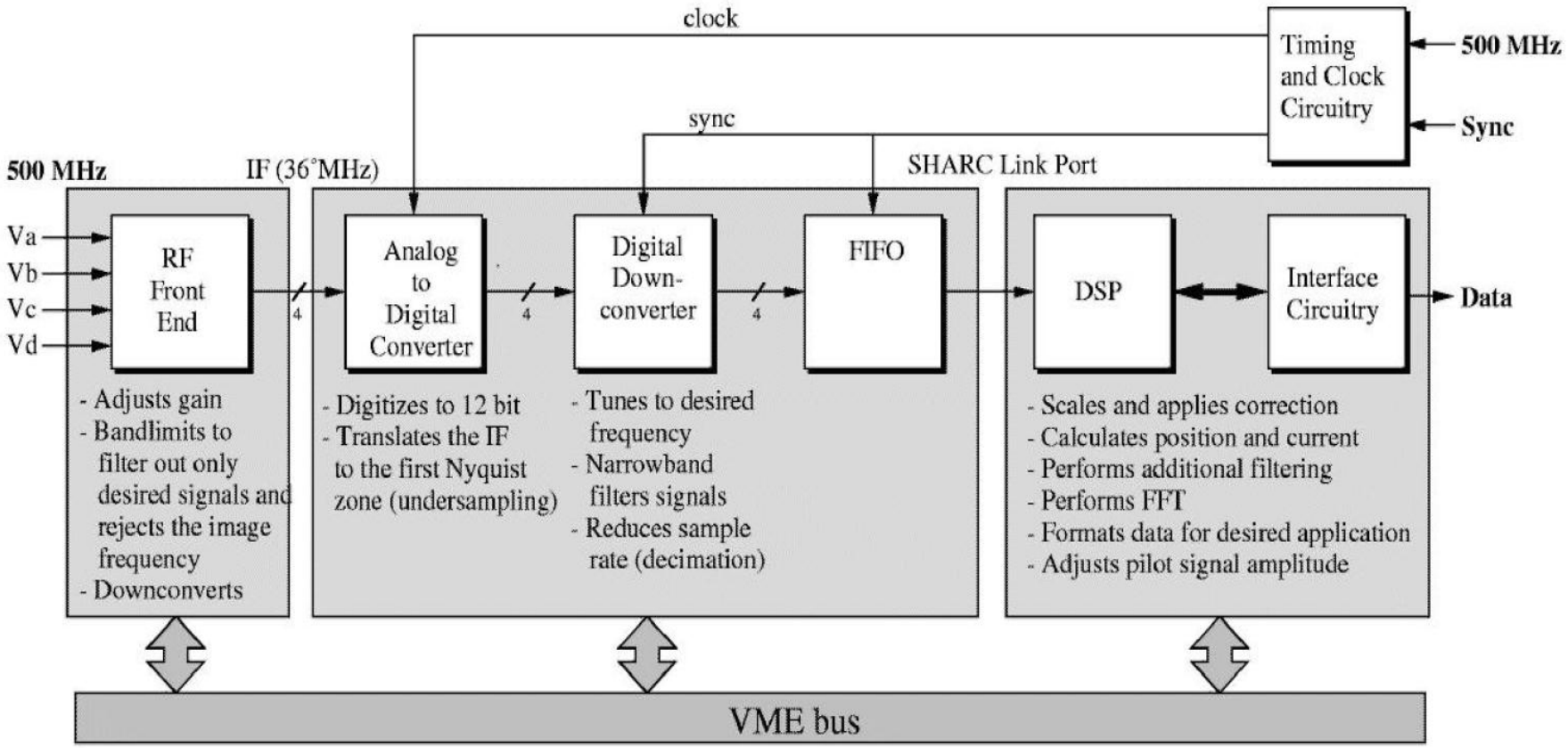
Digitizer/DDC (“QDR”)

- 12-Bit ADC, 28/32MSPS.
- Four 1-channel DDC ASICs (Intersil HSP50214B).
- VME interface (booster) + LVDS DSP interface (ring).

DSP Board

- 12 VME crates, 1 DSP board + 6 BPMs each.
- DSPs receives DDC output (button amplitudes), calculate position etc., perform FOFB algorithm.

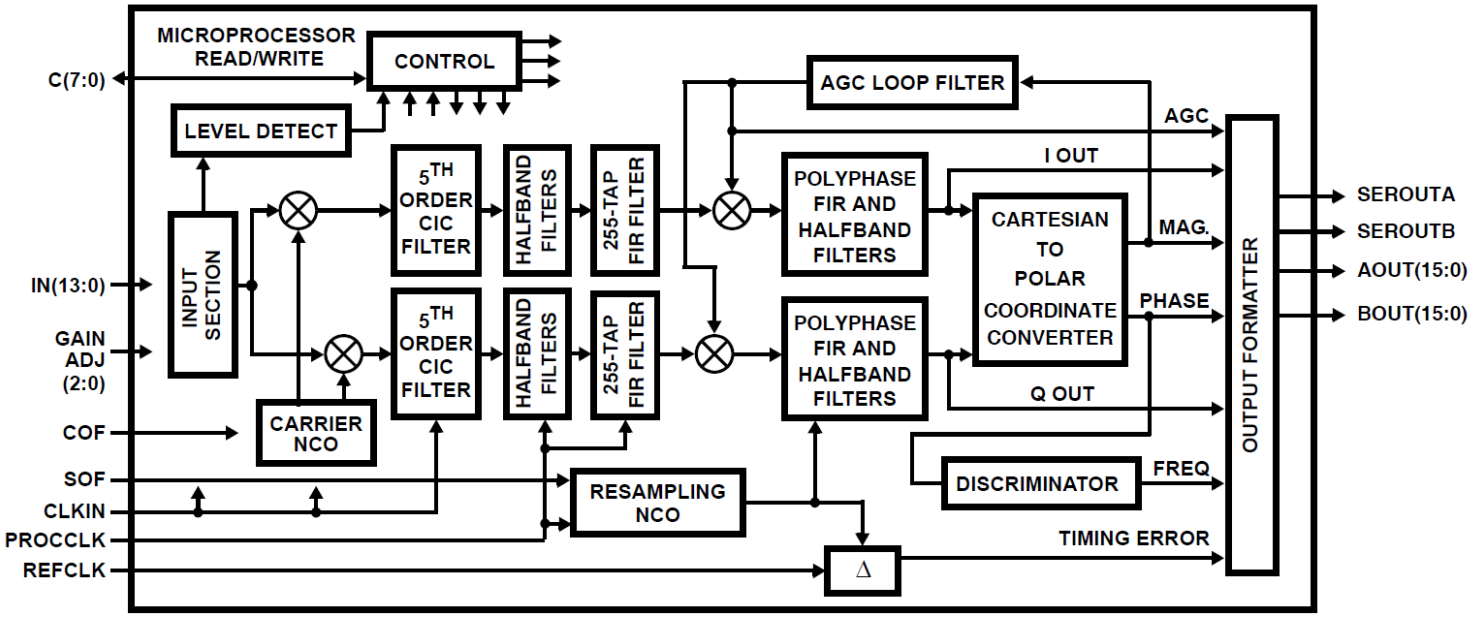
Present SLS BPM System



Present SLS BPM System: DDC

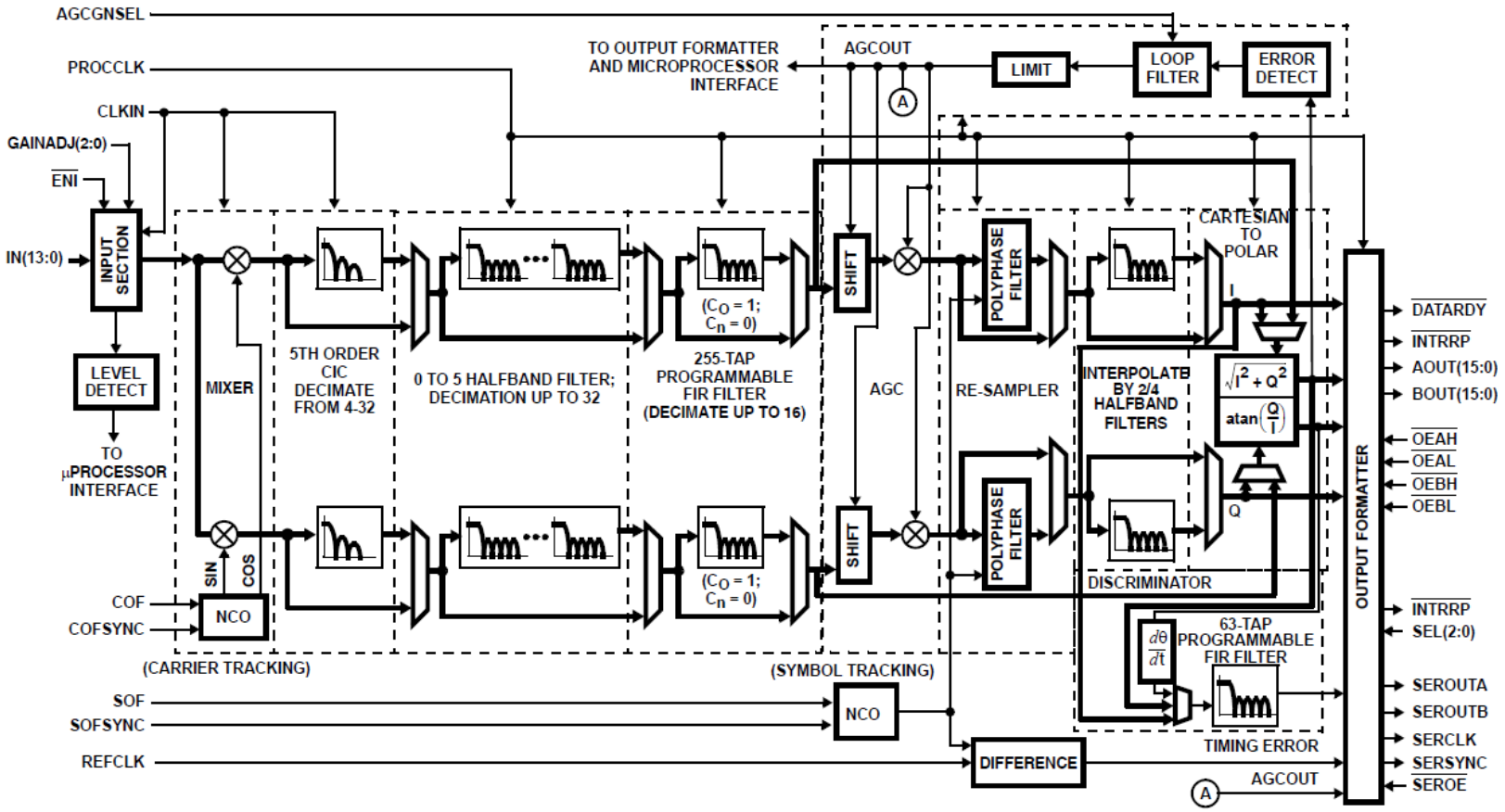
DDC Block Diagram

- ASIC with 1 Channel (Intersil_HSP50214B)
- Future SLS BPM Upgrade: Want same flexibility (full filter reprogramming during operation, no hard-coding of filter coefficients in FPGA firmware …)

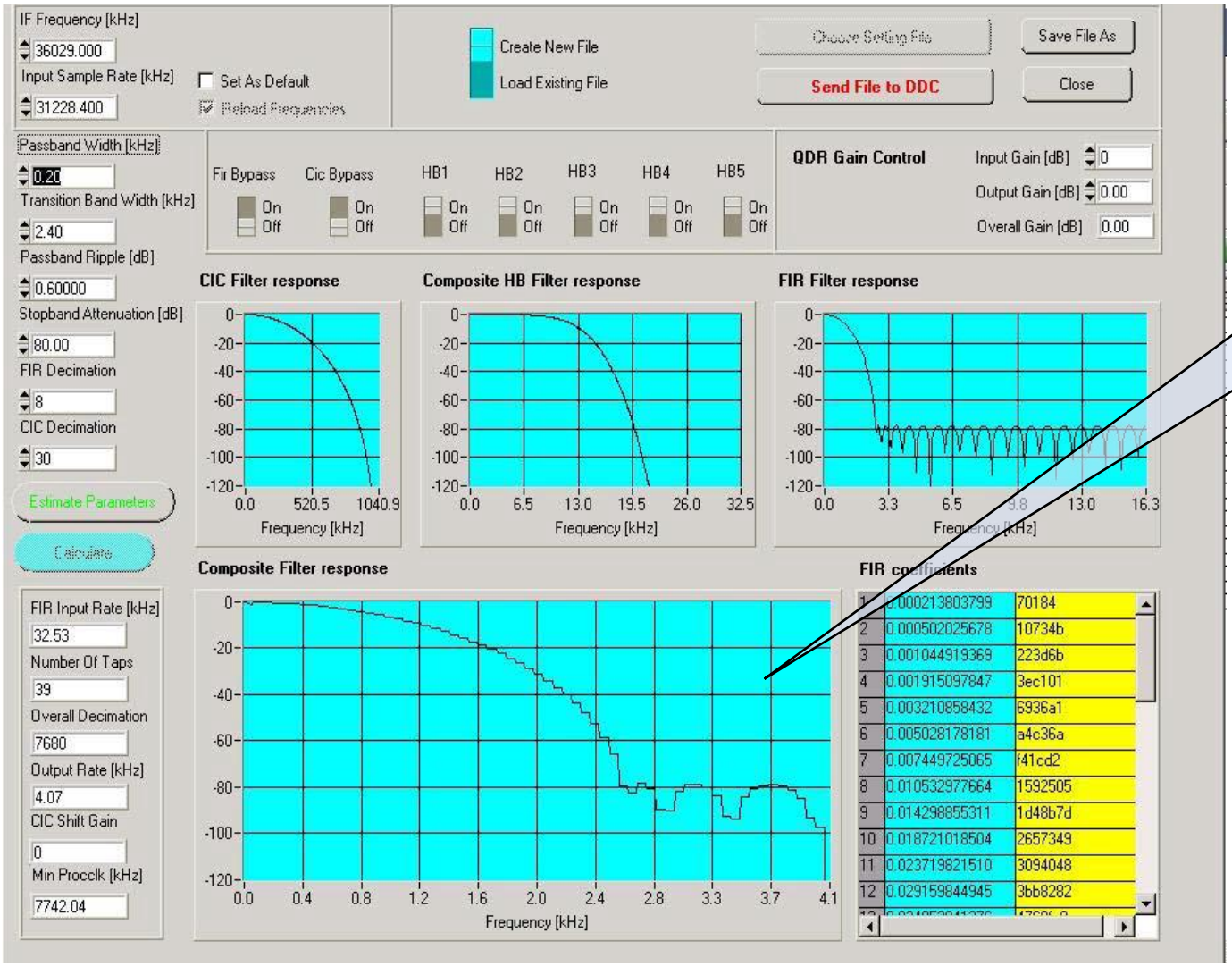


Present SLS BPM System: DDC

DDC Block Diagram (Cont'd)

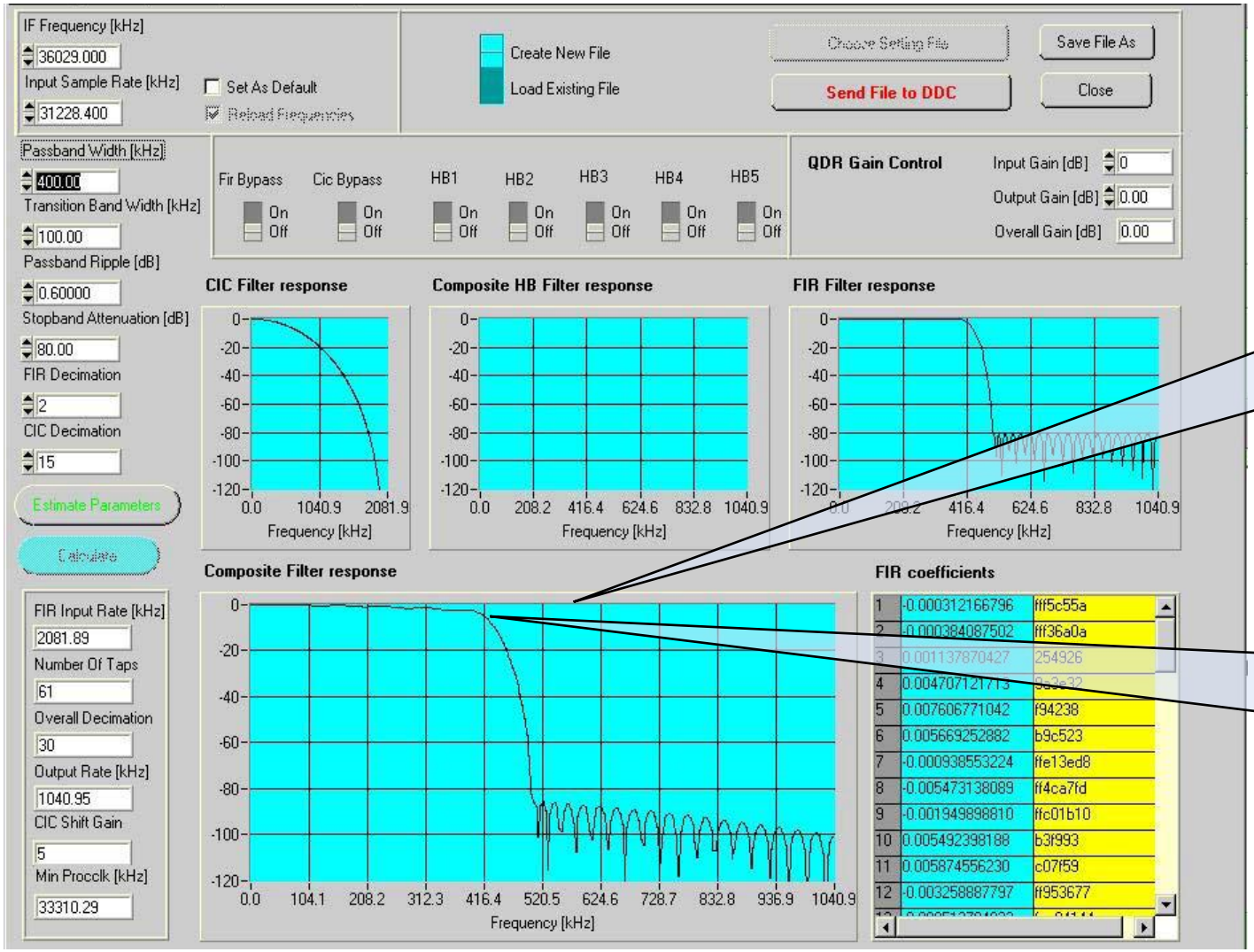


Present SLS BPM System: DDC



DDC filter response for orbit feedback mode (4 KSPS data rate)

Present SLS BPM System: DDC



DDC filter response for turn-by-turn mode (1 MSPS data rate)

Future BPM upgrade: Would like to have flat passband

Present SLS BPM System: Specs

Parameter	Value for FOFB mode (4 KSPS)	
	Original Spec	**Achieved**
Dynamic range	1-500 mA	0.1-500 mA
Beam current dependence • Full range • Relative 1 to 5 range • Differential @ 400 mA (typ.)	 < 100 µm < 5 µm -	 < 100 µm (I > 42mA) <35 µm <0.1 µm/mA
Bunch pattern dependence (typ.)	-	1.5 µm (FPFB off)
Temperature drift (electronics)	-	2 µm/°C
Resolution @ 0.8 kHz BW (-3 dB)	< 1 µm	0.8 µm

- DBPM Resolution = 0.8 µm (0.8 kHz BW):

  < σ(y)/10 @ mini-beta ID BPMs (5 nm, 1% coupling: σ = 10 µm = original spec.)

  = σ(y)/5 @ mini-beta ID BPMs (5 nm, 0.13% coupling, σ = 4µm)

But: FOFB needs only ~ 100 Hz BW, and average beta functions @ BPMs are larger than @ mini-beta ID BPMs → DBPMs not above, but close to the usual σ /10 resolution requirement for 0.13% coupling.

12/2011: SLS achieved 1pm rad vert. emittance. σ~1.5µm in low-beta IDs

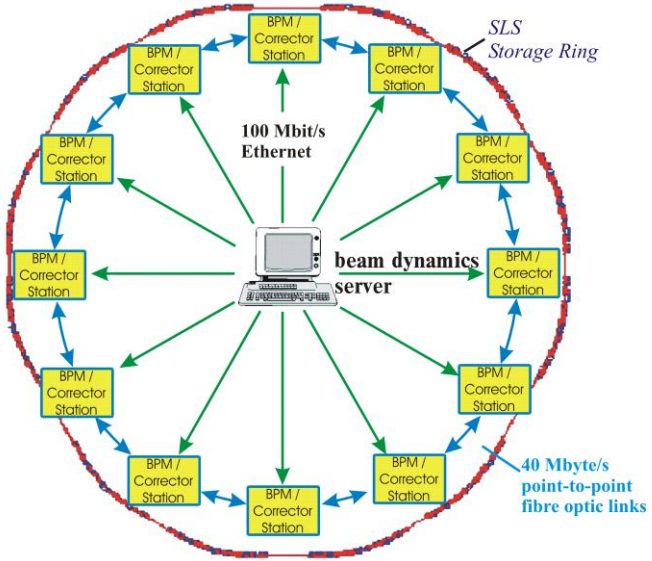
Present SLS BPM System: FOFB

Orbit Stability Requirements:

- Angular stability: < 1 µrad (typ. < 10 µm at experiment)
- Position stability: σ/10 at Insertion Devices (ID)
  → low beta ID: vertical beam size @ BPM ~10 µm (1% coupling)
  → 1 µm RMS in vertical plane (0.13% coupling: 0.4 µm RMS)
- Suppression of orbit perturbations up to 100 Hz by factor of >5
- Fast compensation of orbit distortions due to ID gap changes

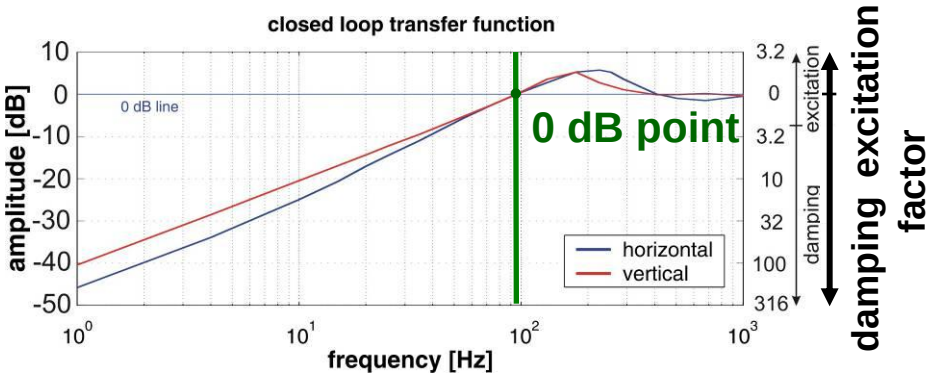
Fast Orbit Feedback (FOFB) Features:

- 73 BPMs / 73 horizontal and 73 vertical correctors
- Decentralized data processing (12 sectors)
- Sampling and correction rate: 4 kHz
- Point-to-point fiber optic ring for
  next-neighbour (not global) data exchange
- Initialization by beam dynamics application
- FOFB in user operation: since Nov. 2003



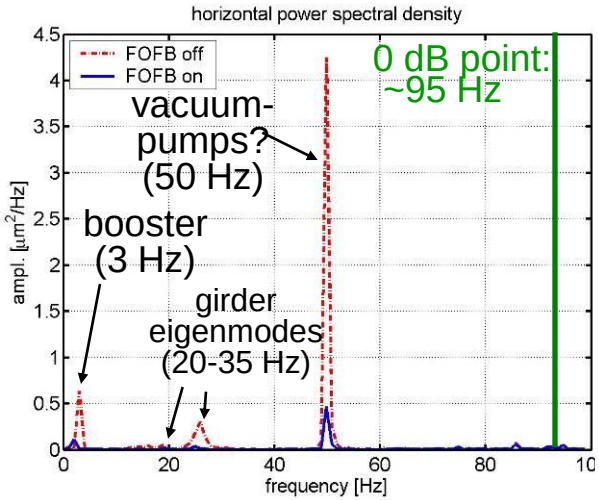
Present SLS BPM System: FOFB

Distortion suppression function

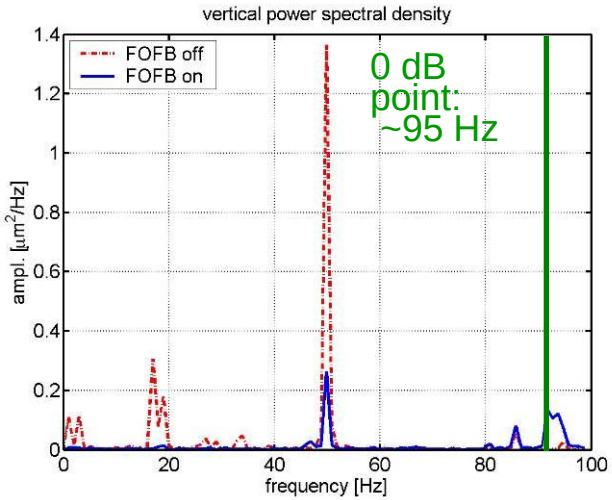


- Suppression up to 95 Hz
- Bandwidth limited by electronics loop delay (technology: 1999)

Spectral power density (1–150 Hz)



horizontal



vertical

Global Orbit Stability

(1 – 150 Hz):

Horizontal:

0.41 µm · $\sqrt{\beta_x}$ (FOFB on)

(0.83 µm · $\sqrt{\beta_x}$ (FOFB off))

Vertical:

0.29 µm · $\sqrt{\beta_y}$ (FOFB on)

(0.41 µm · $\sqrt{\beta_y}$ (FOFB off))

Contents

Upgrade Plans & Activities

Motivation for New BPM/FOFB System

- Long-term maintenance, spare part availability.
- Performance (BPM resolution, drift, computing power for better FOFB algorithms, …).
- Want upgrade before reaching rising edge of bath-tub reliability curve.

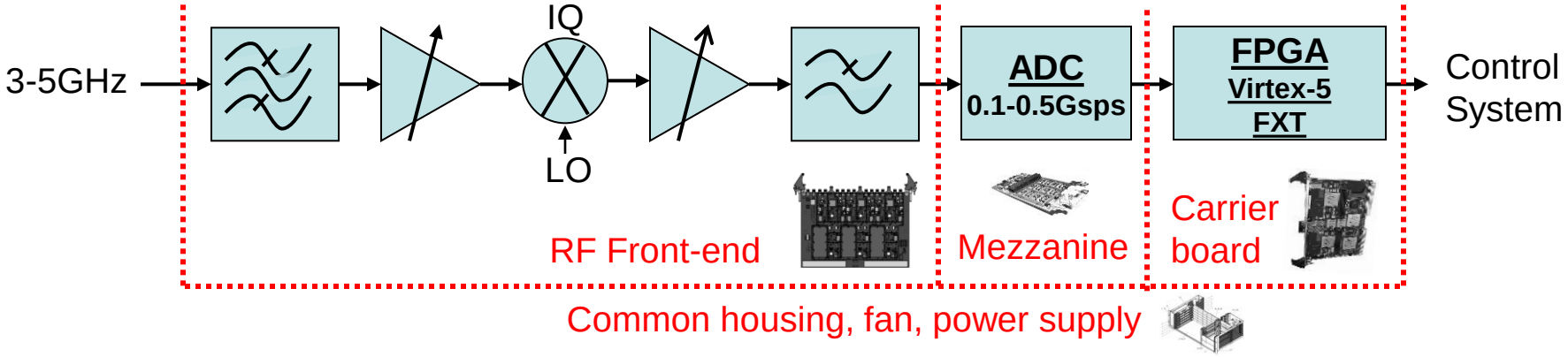
Strategy:

- PSI develops cavity BPM system for European XFEL & SwissFEL.
- New SLS BPM system can use same platform.

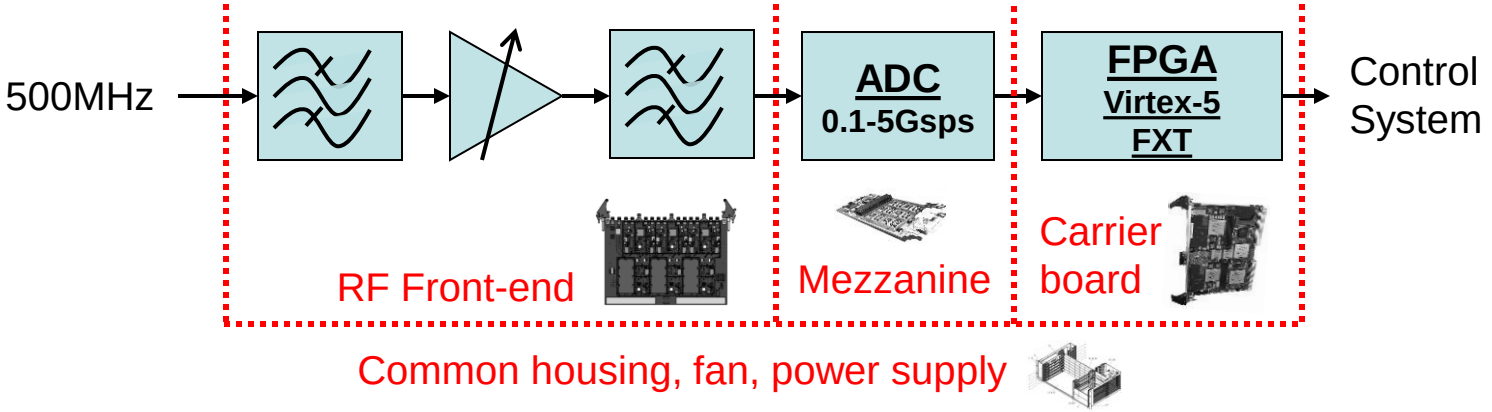
Upgrade Plans & Activities

Modular BPM/Diagnostics Platform Architecture

- E-XFEL / SwissFEL Cavity BPM Electronics (Simplified)



- New SLS BPM Electronics (Simplified)



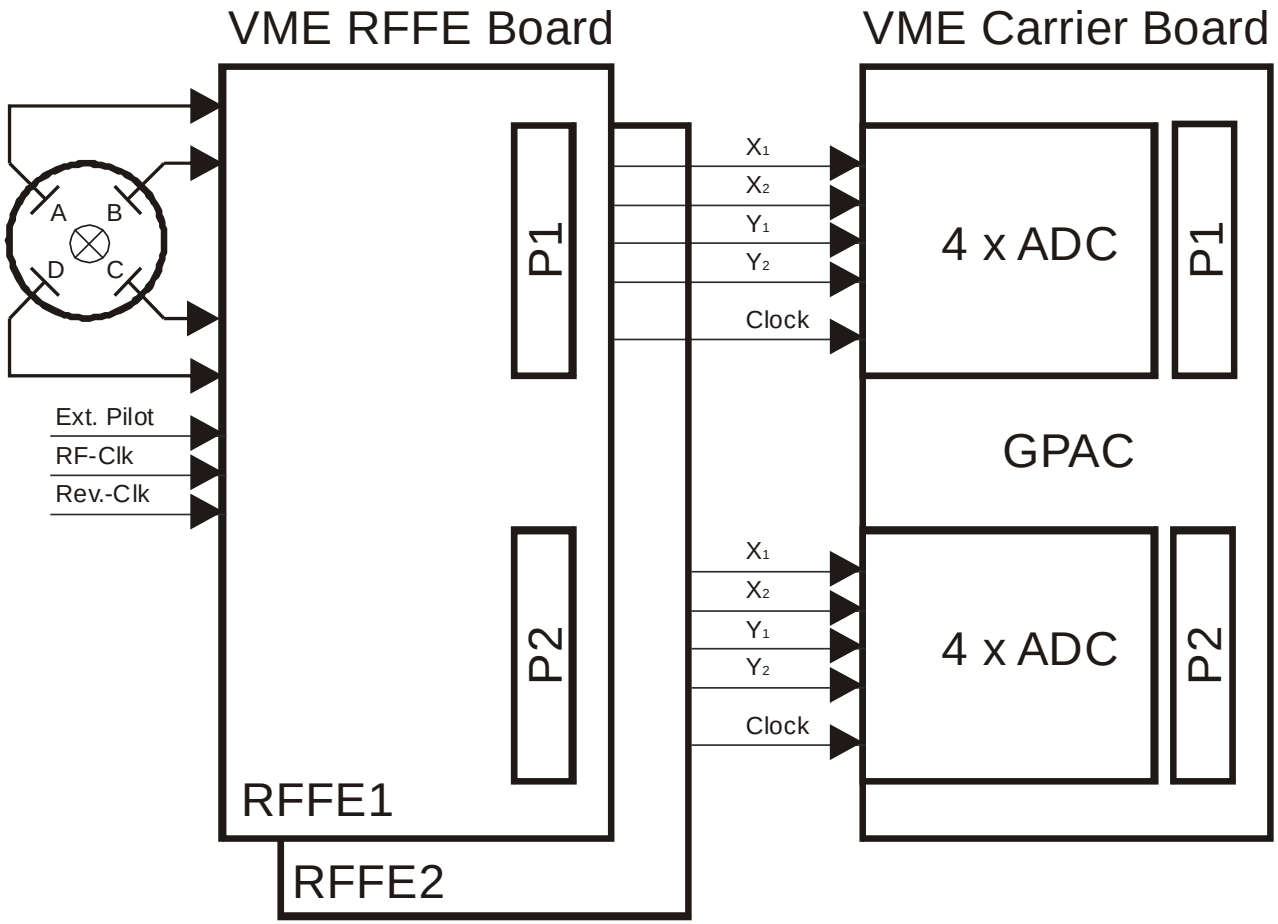
Upgrade Plans & Activities

SLS & FEL BPMs: Platform Strategy

- Modular design: RF front-end, ADC mezzanine, FPGA carrier board. Standardized interfaces.
- SLS BPMs can use same FPGA carrier board as E-XFEL & SwissFEL.
- ADC mezzanine: Requirements for SLS BPMs & FEL undulator BPMs also very similar (16-bit, >100MSPS, …). Synergies save development time.
- Need new SLS-specific RF front-end.
- SLS Goal: Improve noise (>3x, ideally <100nm @ 2kHz), drift (active temperature stabilization, ...), latency, ...

Upgrade Plans & Activities

New SLS BPM Electronics: Prototype Block Schematics



Upgrade Plans & Activities

Advantages of SLS BPM In-House Design

- Estimate: Less expensive (incl. man power) compared to commercial solution.
- Synergies SLS ↔ E-XFEL / SwissFEL: Less man power for development & long-term maintenance.
- No “black box”. All documentation (source codes, board schematics, …) available. Reduces time & costs to integrate systems, fix problems, add new features. Ensures high SLS availability / uptime.
- Avoids dependence on companies.

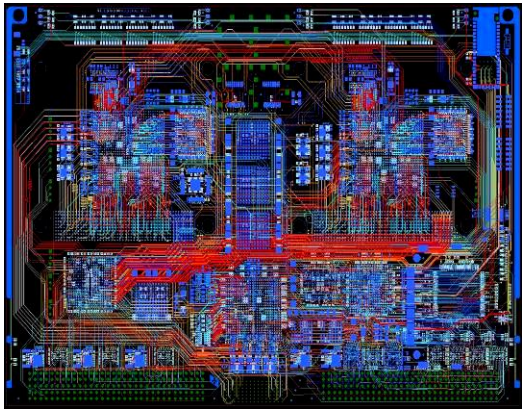
Upgrade Plans & Activities

Design Status of New SLS BPM System:

- FPGA Carrier Board: Prototype successfully tested. SLS-specific FPGA firmware (digital filters, …) under development: DDC + position calculation working.
- ADC mezzanine: First beam tests use E-XFEL BPM mezzanine. Then: Make design optimized for SLS (different no. of ADCs, jitter optimization, …).
- RF front-end: Concept & schematics draft finished. PCB layout, production & first tests until mid 2012.
- EPICS: Access of FPGA board (via VME IOC) working (medm ADC data GUI, DDC config. GUI, …).

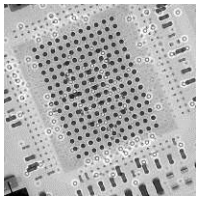
Upgrade Plans & Activities

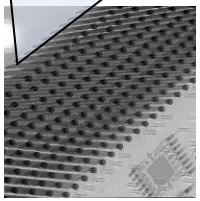
Generic PSI FPGA ADC Carrier Board ("GPAC")

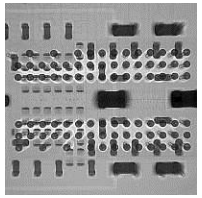


- Prototype tested, works fine.
- SLS: One carrier board for two BPMs (2 mezzanines with 4 ADCs each).
- Present prototype uses Virtex-5 FPGAs. (we are currently evaluating which type to use for the final version: Artix/Kintex-7?).

X-ray quality control (RAMs, connector)



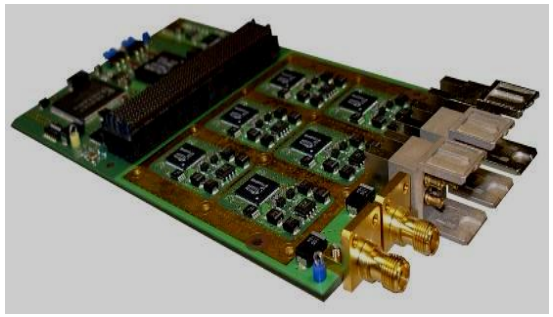
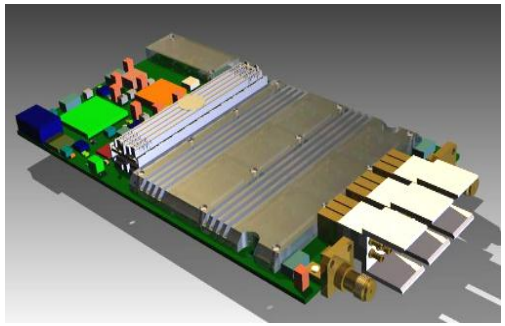
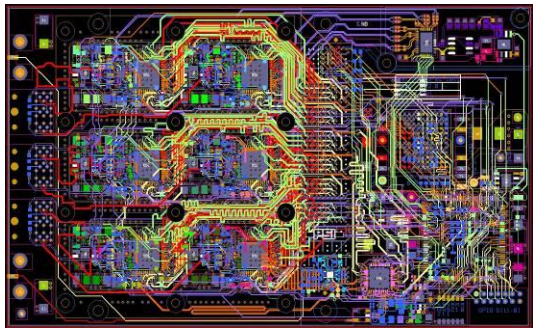




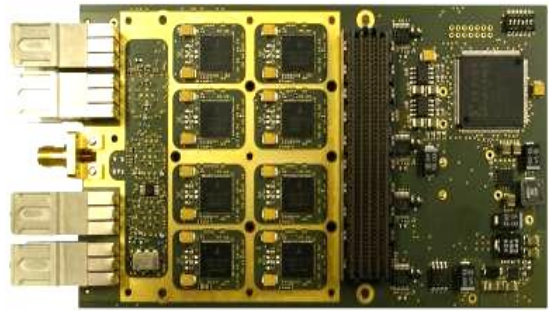
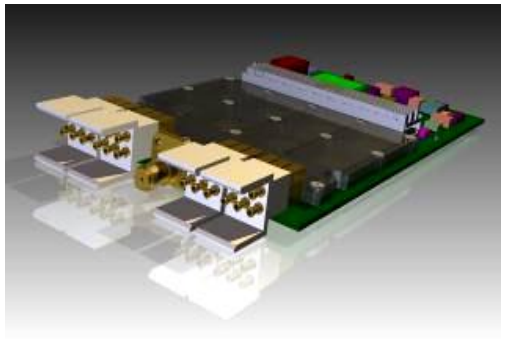
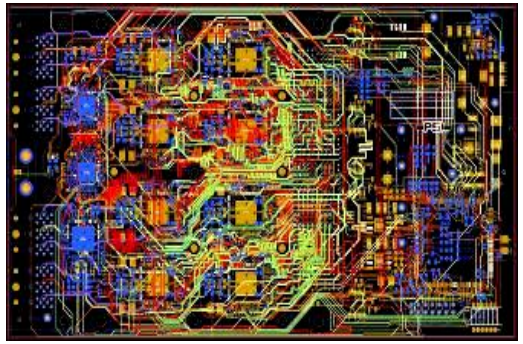
Upgrade Plans & Activities

E-XFEL Undulator & Button BPM ADC Mezzanines

Cavity BPMs: 6-channel, 16-bit, 160MSamples/s.

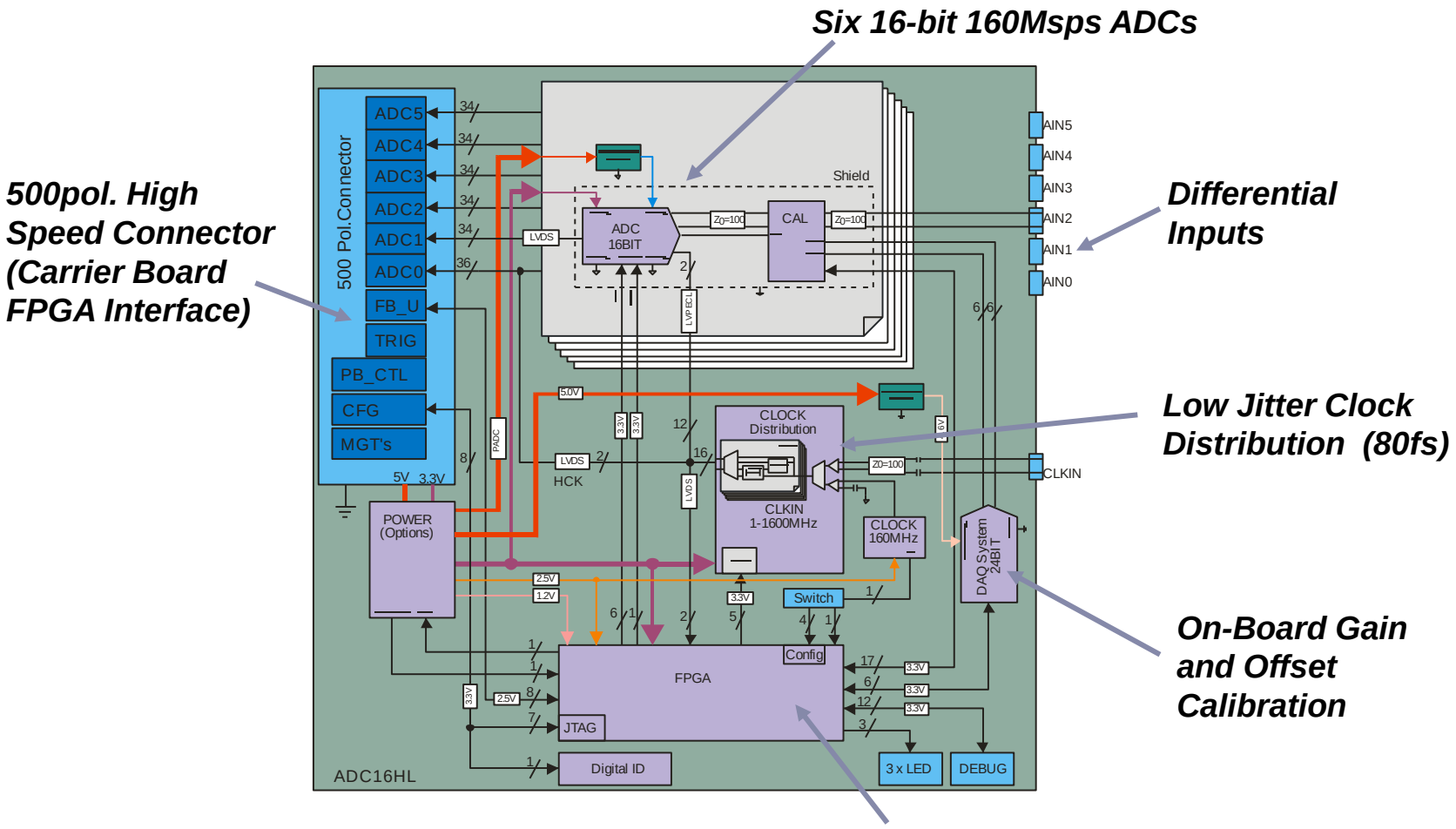
Button BPMs: 8-channel, 12-bit, 500MSamples/s.

Both types: Low-noise differential coax inputs.

Upgrade Plans & Activities

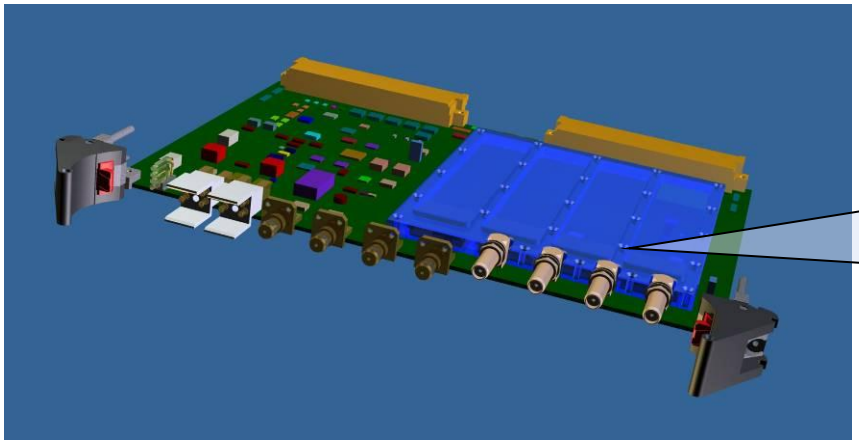
Using Cavity BPM ADC for 1st SLS DDC Tests ...



Upgrade Plans & Activities

New SLS BPM RF Front-End

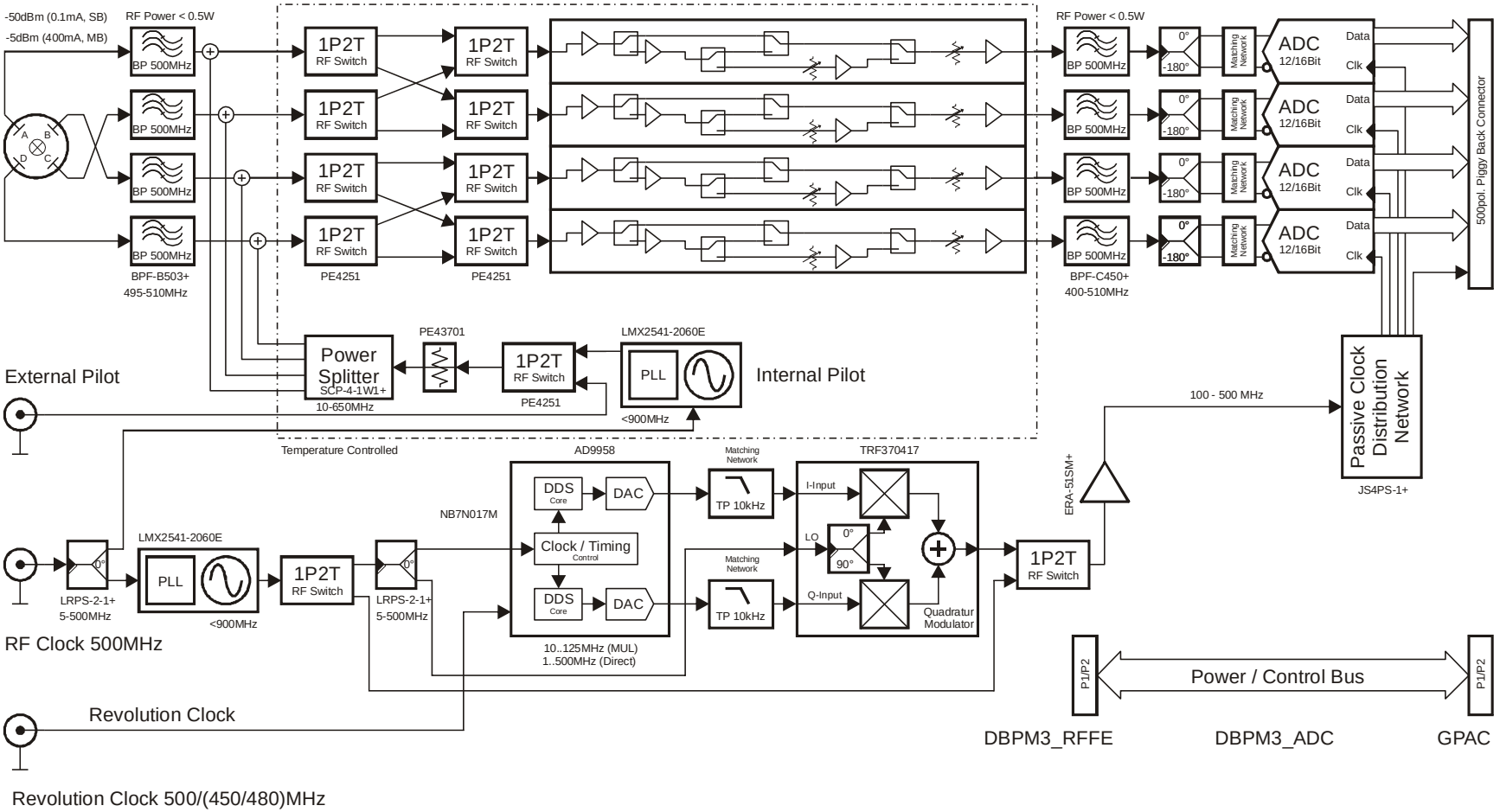
- Active local multi-point temperature stabilization of drift-sensitive electronics components on the PCB, for lowest beam position drift. Present SLS BPMs: No temperature stabilization, but temperature sensor.



PCB layout of new prototype has started, production & 1st SLS beam tests until mid 2012.

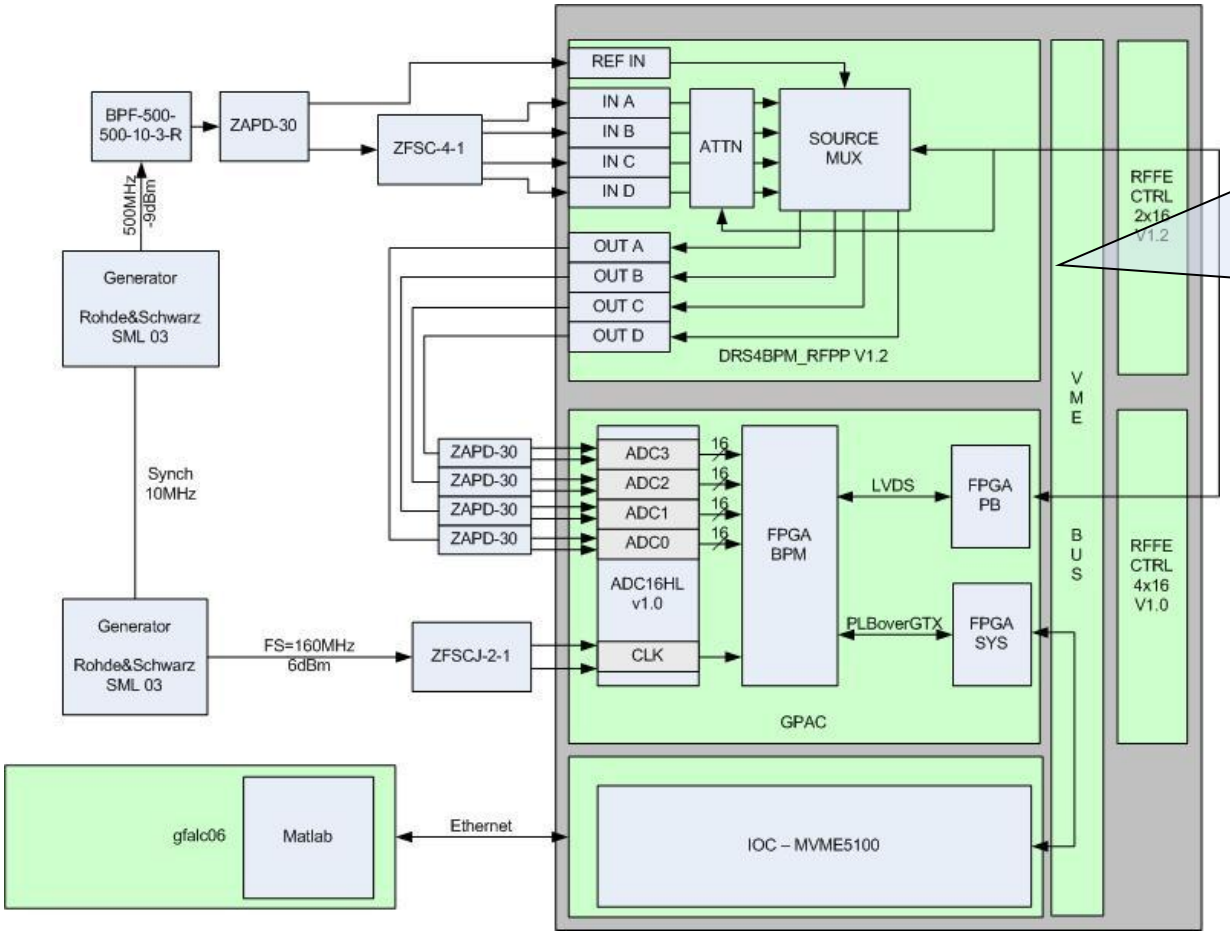
Upgrade Plans & Activities

New SLS BPM RF Front-End: Block Schematics

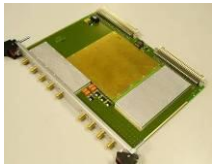


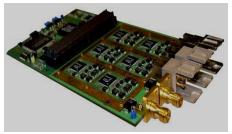
Upgrade Plans & Activities

Lab Test Setup For DDC Tests



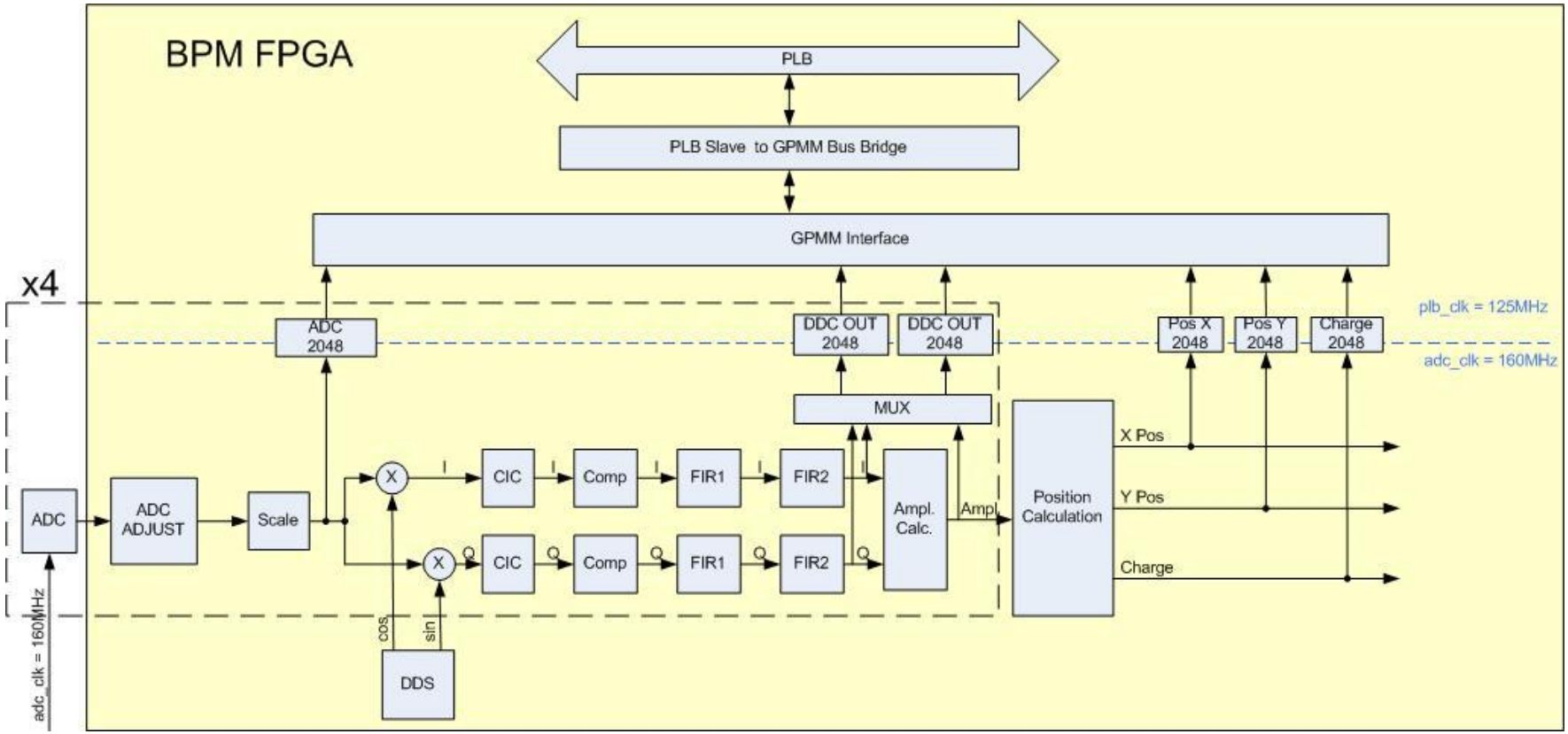
PSI modular BPM electronics: Using SwissFEL test injector 500MHz resonant stripline RFFE & E-XFEL cavity BPM ADC for tests (DDC, ...), until dedicated new SLS ADC & RFFE is ready.





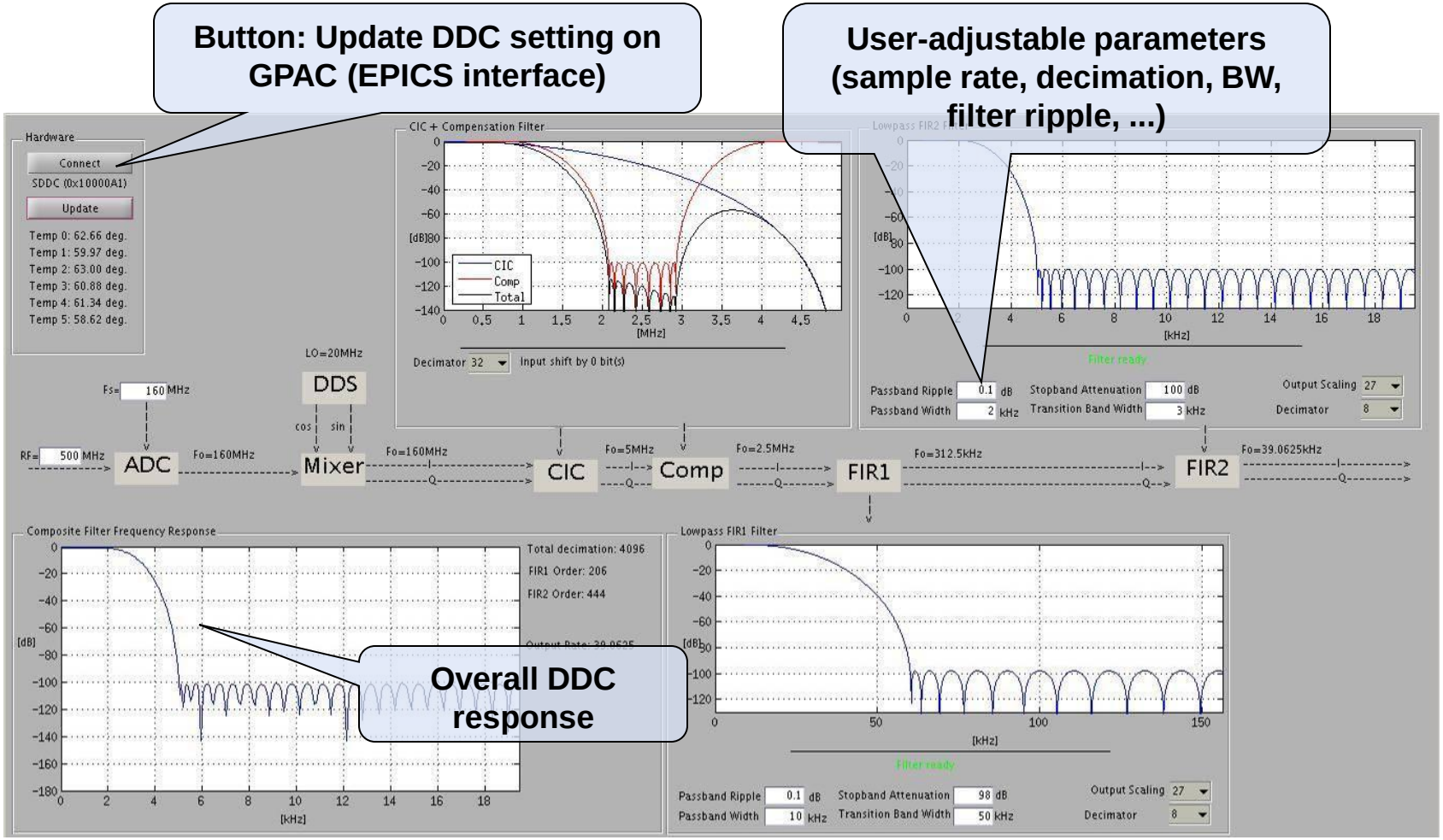
Upgrade Plans & Activities

New DDC: VHDL, Optimized for Speed & Space



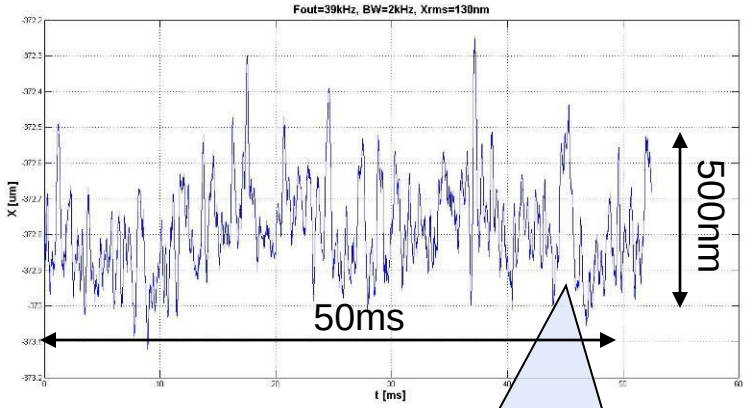
Upgrade Plans & Activities

GUI: Full DDC Reconfiguration During Operation

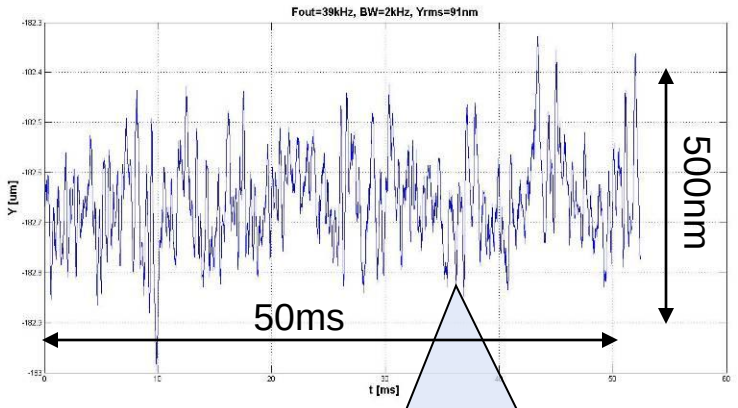


Upgrade Plans & Activities

DDC Test Results (Stripline RFFE + Cavity ADC + GPAC)



X: 130nm RMS (2kHz BW, 10mm geometry factor, 50ms)



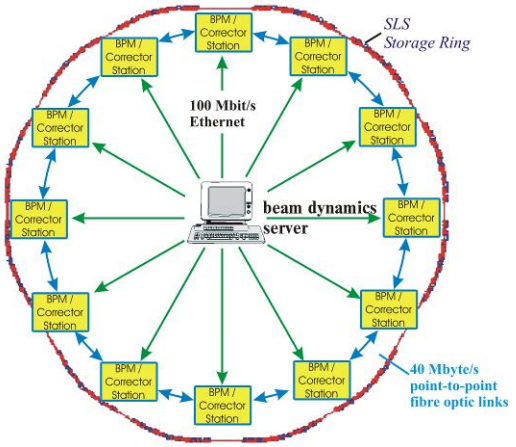
Y: 91nm RMS (2kHz BW, 10mm geometry factor, 50ms)

- Data presently stored in internal FPGA BRAM (50ms).
- To do: Store data in larger ext. RAM, for long-term (hours, days, ...) tests & low-frequency noise / drift analysis.
- Results promising: RFFE + ADC were not made for SLS but FEL. Expect better performance with dedicated new SLS RFFE & ADC.

Upgrade Plans & Activities

Fast Orbit Feedback: DSP Boards

- Present System: FOFB algorithm performed on 12 VME DSP boards.
- New FOFB System: Algorithm can be implemented on single (few) DSP(s).
- Data transfer between BPMs & DSP board via multi-gigabit fiber optic links of the new BPM board. Also to be used for beam-based SwissFEL feedbacks.



Evaluation board for new FOFB DSP: 160 GFLOPS. 55x faster than all 24 DSPs of present FOFB system together. Easy connection to new BPM system / GPAC via PCI Express (4 wires …).

Upgrade Plans & Activities

Fast Orbit Feedback: Corrector Magnets

Present FOFB

- DSP boards receive BPM data
- Calculate corrections
- Set currents of corrector power supplies (PS) via VMEbus & Hytech VME boards

Corrector power supplies: So far no good reason for upgrade.

New FOFB

- Sets currents of corrector PS via long-range multi-gigabit fiber optic links: Faster correction/latency, decoupling of DSPs & PS (quantities, location), …
- Required electronics: Prototype available (final version may use newer FPGA …).

Contents

Summary

- Long-term failure statistics: SLS BPM/FOFB upgrade not urgent. Still high reliability. Performance: No pressure from users, still happy with beam stability.

- Development of new BPM/FOFB system already started: Takes time, should be ready before reliability reaches rising edge of “bath tub curve” & spares run out of stock.

- Platform strategy: Maximize synergies with E-XFEL & SwissFEL, minimize overall costs, maximize performance & availability. Ensure efficient long-term maintenance by full in-house know-how of all system details.

PSI Team & Credits

Present SLS BPM Electronics (Design in 2000):
Patrick Pollet (QDR)
Thomas Schilcher (DSP)
Volker Schlott
Rok Ursic
Et al. (see e.g. DIPAC 2001, CT03)

New SLS BPM Electronics:
Raphael Baldinger (GPAC HW)
Robin Ditter (stripline RFFE)
Waldemar Koprek (DDC / GPAC FW)
Goran Marinkovic (GPAC FW / HW)
Markus Roggli (ADC & RFFE schem./layout)
Markus Stadler (RFFE)
Daniel Treyer (RFFE)

And:
Thanks also to support from other PSI/GFA groups.

Paul Scherrer Institut

PSI

Thank you for your attention!