Session Program

28 September 2026 to 2 October 2026

TWEPP26 Topical Workshop on Electronics for Particle Physics

Poster 2

Castelldefels, Barcelona, Spain
Hotel Rey Don Jaime

Thursday 1 October

17:40

Poster 2

Poster Session | **Location:** Castelldefels, Barcelona, Spain, Hotel Rey Don Jaime

Mighty-ASIC-Readout-System for the LHCb Upgrade 2 Mighty Tracker

Speaker
Dr Dirk Wiedner

Wafer probing for the LHCb Mighty-Pixel Tracker

Speaker
Jonas Malte Ronsch

DCDCUTS: A Universal Test System for Qualification of CERN DC–DC Converters

Speaker
Joel Daricou

Burn-in and System-Level Validation of Phase-2 CMS Outer Tracker Backend Electronics in a Full ATCA Setup

Speaker
Mark Pesaresi

Development of COFFEE3: A 55 nm HV-MAPS for In-Pixel Readout Architecture Exploration

Speaker
Dr Yang Zhou

Validation and Operational Studies of CMS Inner Tracker Pixel Modules under HL-LHC Conditions

Speaker
Amrutha Samalan

Production test system for FoCal-E pixel layer qualification

Speaker
Mr Bendik Husa

The OBDT Electronics for the CMS Drift Tube Upgrade at the HL-LHC

Speaker
Muhammad Bilal Kiani

FLAXE, a SoC readout ASIC for ECALp calorimeter at LUXE experiment

Speaker
Jakub Moron

Commissioning the CMS Phase-2 Outer Tracker: DAQ, Software, and System Integration toward LS3

Speaker
Matteo Magherini

PHOCA: Cryogenic photon readout ASIC for silicon photomultiplier (SiPM) and photomultiplier tube (PMT) sensors

Speaker
Llorenç Fanals-i-Batllori

THRIGLAV: 100 x 100-pixel sub-10ps resolution time-resolved 28nm readout ASIC for 3D-integrated LGAD sensors

Speaker
Bojan Markovic

Performance of the ICECAL65 ASIC for energy measurement in the LHCb Calorimeter Upgrade II

Speaker
Mr Alberto López

Design and Characterization of a Low-Noise Wide Dynamic Range Analog Channel in 65 nm CMOS Technology for Silicon-Strip Detector Readout

Speaker
Luca Ghislotti

Improving linearity and bandwidth of Time-over-Threshold circuits for amplitude measurement

Speaker
Jesus Pena Rodriguez

VertexPix: A HV-CMOS Pixel Detector with Fully Synthesized Readout in 130 nm SiGe BiCMOS Technology

Speaker
Bowen Xu

Characterization of EICROC, the AC-LGAD readout ASIC for the Electron-Ion Collider (EIC)

Speaker
Adrien VERPLANCKE

Radiation hardness testing and bench characterization of the FastRICH ASIC for future LHCb RICH detectors

Speaker
Vlad-Mihai Placinta

A Self-Triggered, Event-Driven Readout ASIC for the eXTP PFA X-ray Polarimeter

Speaker
wangna@ihep.ac.cn wangna

CPRE64 - a Low-Noise 64-Channel Readout ASIC for 3D CZT Compton Imaging

Speaker
Dr Ke WANG

First Test Results From A Shunt-LDO for the Electron Ion Collider in a 110nm CMOS Process

Speaker
Iain Sedgwick

System-Level Validation of the Phase-2 CMS Outer Tracker Using a Multi-Layer Cosmic Telescope

Speaker
Giacomo Fedi

Optical Acceptance Testing of Serenity-S1 Boards for the CMS HGCAL Phase-2 Backend Electronics

Speaker
Ahmed Qamesh

Noise and shielding effectiveness measurements on the ATLAS HGTD demonstrator

Speaker
Laurent Royer

First Integration Test of a Two-Step Powering Scheme with bPOL48V using a CMS 2S Silicon Strip Module

Speaker
Joelle Savelberg

EMI/EMC characterization of the DAQ system of the micromegas detector of babyIAXO experiment.

Speaker
Alberto Arcusa Puente

Testing and validation of custom step-down DC/DC converter system for the ATLAS ITk Strip detector

Speaker
Krzysztof Cieśla

Power Board Design for the ALICE FOCAL-E Pixel Upgrade

Speaker
Bilal Hasan Qureshi

Design of a 10.24 Gbps Data Serializer and Wireline Transmitter for the readout of the ALICE ITS3 detector.

Speaker
Vladimir Gromov

A 25 Gbps VCSEL Driving ASIC Design in a 55nm CMOS technology for Detector Front-end Readout

Speaker
Mr Longkai Li

A Compact Standard-Cell Single-Shot TDC with 8 ps LSB in 16 nm FinFET Technology

Speaker
Alexander Friedrich Elsenhans

A 12-bit sigma-delta DAC in 28nm CMOS process for global threshold setting in pixel detector chips

Speaker
Oi Ying Wong

Design of a 25.6 Gb/s Quarter-rate Radiation-Tolerant Serializer in 28 nm CMOS Technology

Speaker
Gabriele Ciarpi

A low jitter 2.56 Gbps reference-less CDR ASIC in 55 nm for HEP applications

Speaker
Prof. Di Guo

Timing performances of an asynchronous readout MAPS

Speaker
Willy Perrin

A novel sub-10ps event-driven TDC utilizing pulse-interleaved architecture

Speaker
Mr 铮 王

FATIC4: a prototype front-end ASIC for the uRwell readout of the LHCb Muon detector at upgrade II

Speakers
Flavio Loddo, Giuseppe De Robertis

A 20.48-Gbps PAM4 transmitter with 2-tap FFE in 55 nm for high-energy physics experiments

Speaker
Xiongbo Yan

A 5-ps Bin Size TDC Using RO Delay Line with Passive Interpolation

Speaker
Xiaoting Li

Design and Test Results of the SIPAC: A Prototype SiPM Readout ASIC for CEPC Calorimeters

Speaker
Dr Huaishen LI

A 10 Gb/s serialiser and transmitter for multichannel digitiser in 65 nm CMOS

Speaker
Miroslaw Firlej

Front End Readout Solutions for time-of-flight systems employing analog SiPMs

Speaker
Sara Portero Castillo

A multi-pixel TDC for the CACTUS monolithic timing detector

Speaker
Joaquim Pinol Bel

A Low-Power, High-Precision Self-Calibrated TDC with Multi-Timestamp Reconstruction for the barrel time-of-flight detector Readout in the ePIC experiment

Speaker
Datao Gong

Limits of Successive Approximation Register (SAR) ADC Architecture: First Silicon Validation of a 12-bit 65 nm Low-Power ADC for Detector Readout

Speaker
Miquel Ribalda Galvez

Jia WANG

Speaker
Jia WANG

RadPix1: A Monolithic Pixel Sensor Demonstrator with Low-Power Readout and Serial Powering for Future LHCb Upgrades

Speaker
Seddik Benhammadi

Modeling Method for Current-Steering DAC Reference Model of Front-End Readout System Using IEEE User-Defined Nettypes

Speaker
Mr Yuanhong Jiao

PACIFIC++ readout ASIC for the LHCb Mighty-SciFi

Speaker
Krzysztof Piotr Swientek

19:00