Latest generation of ASICs for photodetectors readout

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Orsay MicroElectronics Group Associated

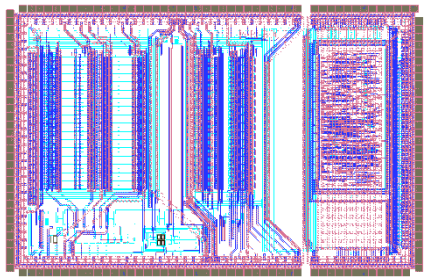
Outline

The OMEGA group has designed a new generation of ASICs, the "ROC" family in AMS (AustriamMicroSystem) SiGe 0.35 µm technology to read out signals from various families of photo-detectors

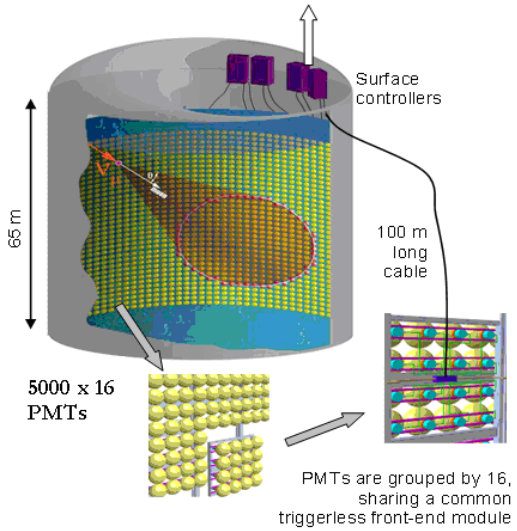
1. **MAROC** (Multi Anode ReadOut Chip) a 64 channels chip to read out Multi Anode Photomultipliers (MAPMT)

2. **SPIROC** (SiPM Integrated ReadOut Chip) a 36 channels chip for Silicon PhotoMultiplier (SiPM) readout

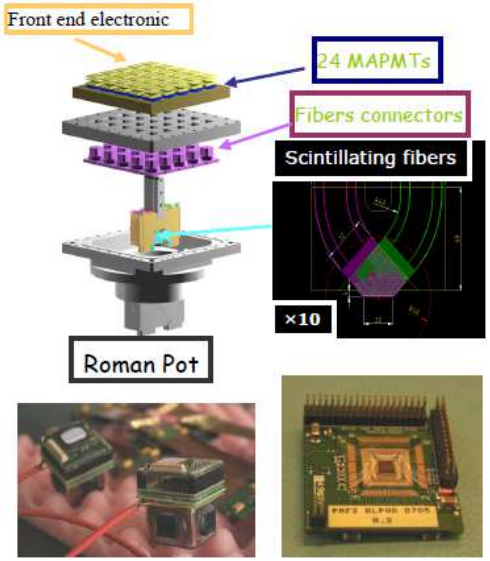
3. **PARISROC** (Photomultiplier ARray In SiGe ReadOut Chip) a 16 channels chip to read out array of Photomultipliers (PMT)



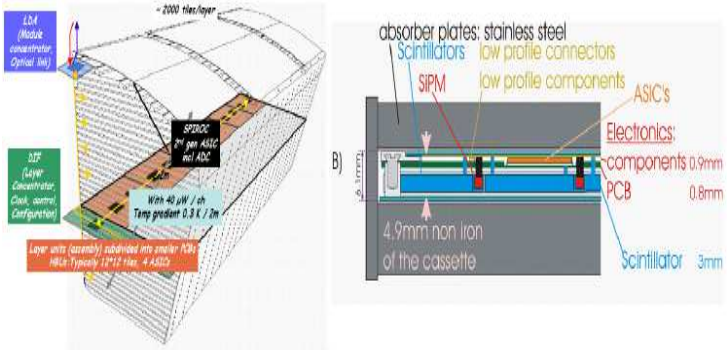
PARISROC layout



PARISROC:
PMm2 project



MAROC:
ATLAS luminometer Roman Pot



SPIROC:
ILC, Analog Hadronic Calorimeter prototype

MAROC for MAPMT

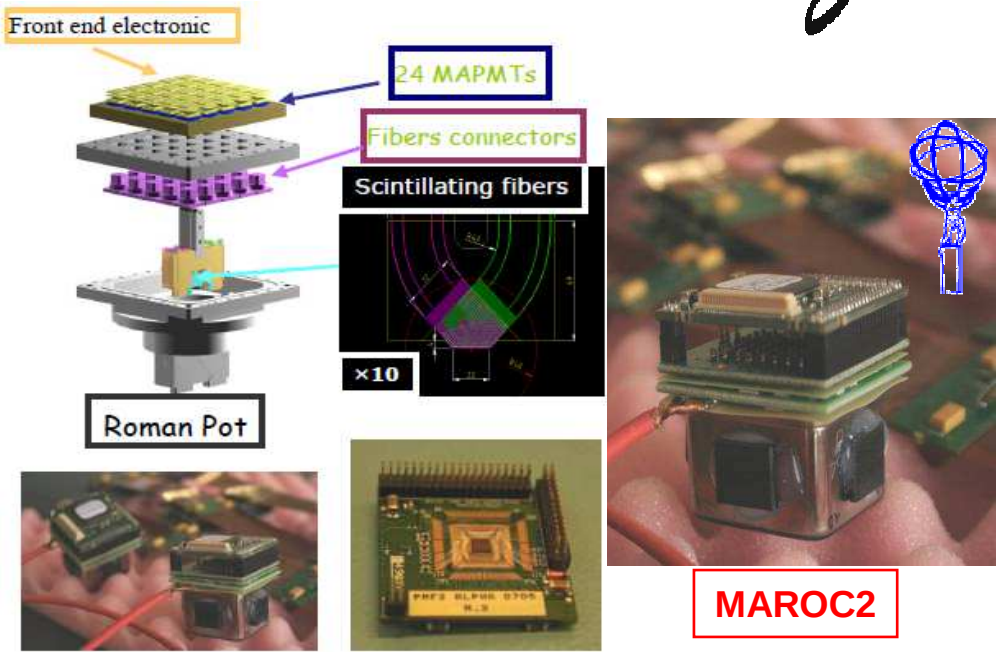
- MAROC stands for Multi Anode Read-Out Chip

- Started with OPERA_ROC (2001)
  - 32 Channels in BiCMOS 0.8 µm for H7500
  - 3000 chips produced in 2002
  - Equipped OPERA in Gran Sasso

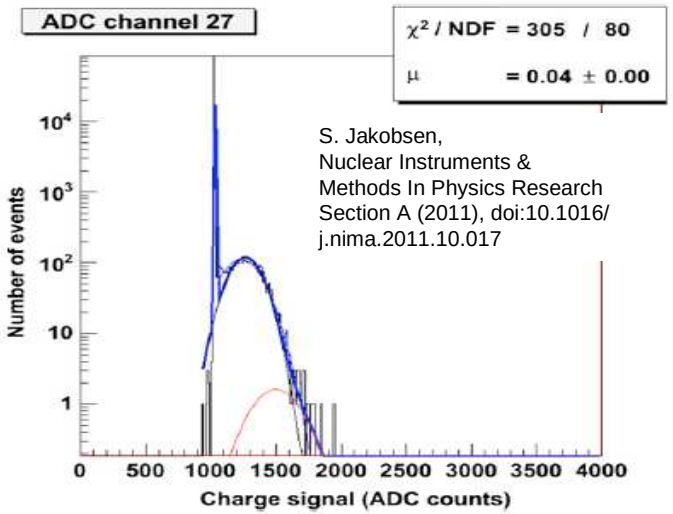
- MAROC1 (2004)
  - First prototype with 64 channels
  - AMS SiGe 0.35 µm (12 mm², Pw=5 mW/ch)

- MAROC2 (2006)
  - 1000 chips produced
  - 250 bonded on a compact PCB for **ATLAS luminometer (ALFA)**
  - Also equips **Double-Chooz, Memphyno, medical imaging…**

- MAROC3 (2009)
  - Lower power dissipation
  - Wilkinson ADC added
  - 1000 chips produced



MAROC2



S. Jakobsen, Nuclear Instruments & Methods In Physics Research Section A (2011), doi:10.1016/j.nima.2011.10.017

Charge spectrum of one MAPMT channel illuminated by a LED at low light level.

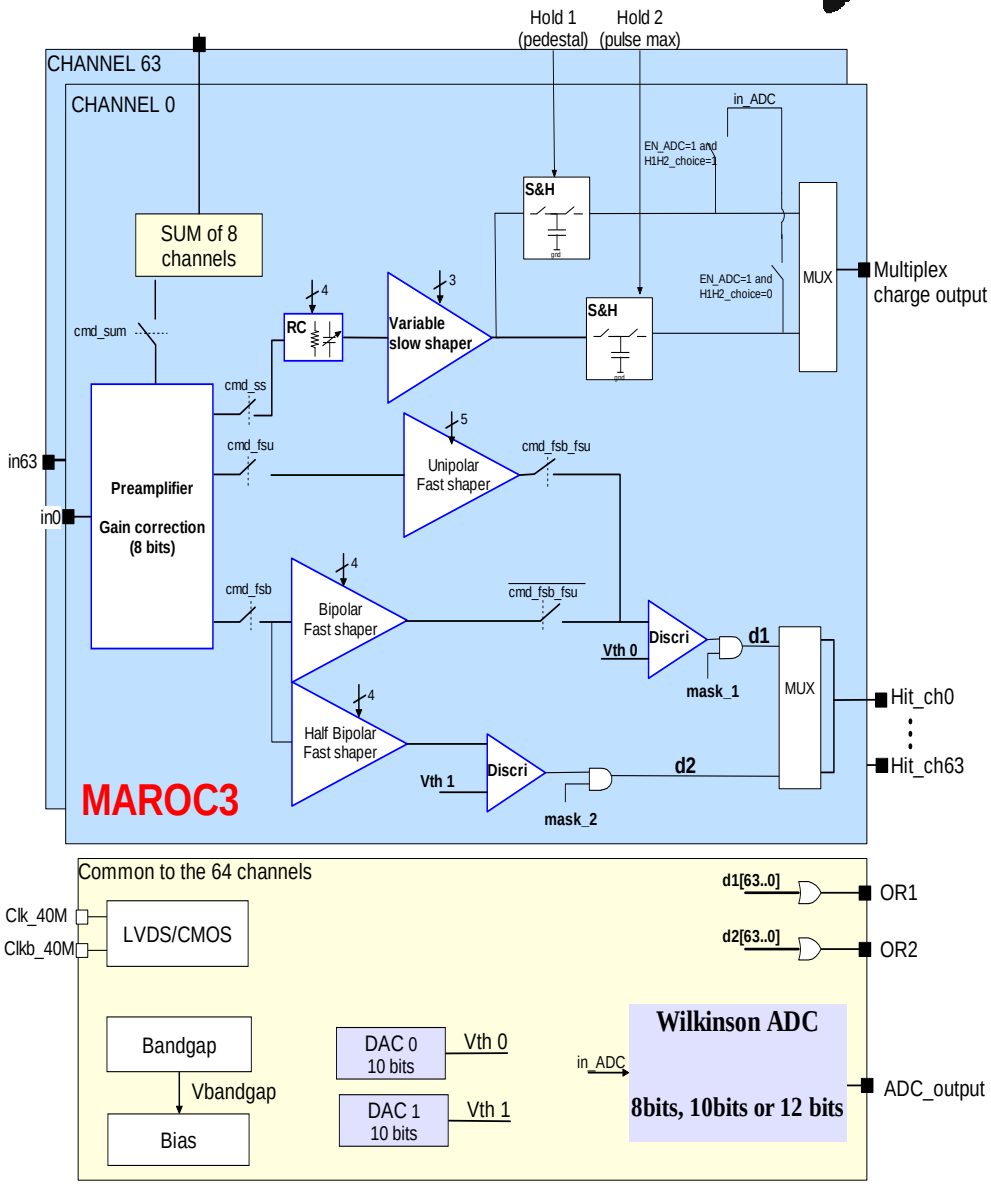
More information (MAROC): blin@lal.in2p3.fr ; barrillo@lal.in2p3.fr

MAROC3 - general architecture

- 64 channel inputs:
  Variable gain current preamps (8 bits/ch.)
- 64 trigger outputs + 2 OR outputs
- 1 mux. analog charge output
- 1 digitized charge output
  (8, 10 or 12 bits ADC)

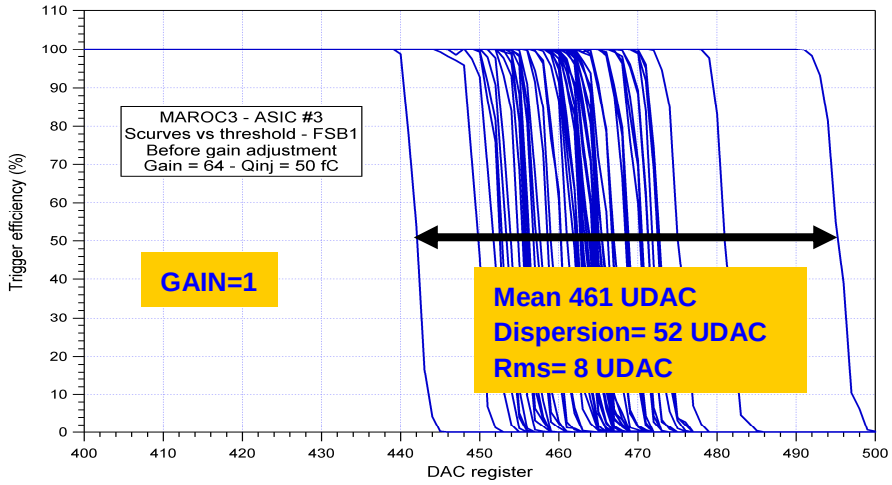
- Pw = 3 mW/ch
- Trigger efficiency= 5fC

- Low input impedance (50-100 Ω)
- Variable slow shaper (20-100 ns)
- 2 T&H (baseline and max.)
- 10 bits DAC as threshold
- Internal bandgap for voltage references
- 828 slow control parameters

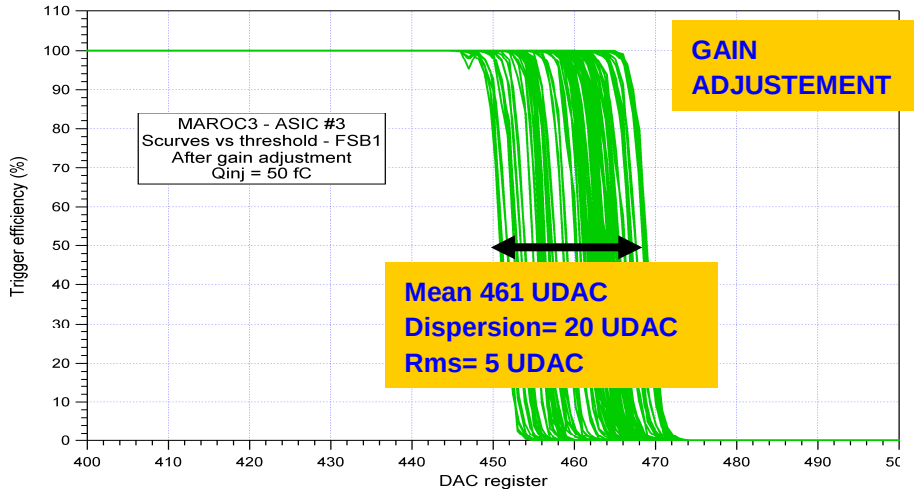


MAROC3 - characterization tests

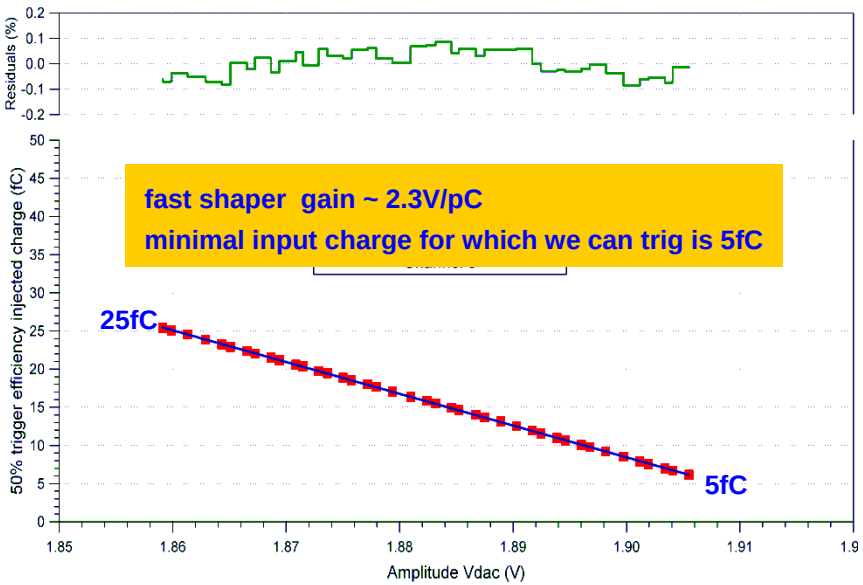
Trigger efficiency of the 64 channels as a function of the DAC value for 50fC injected charge and the same preamplifier gain



Trigger efficiency of the 64 channels as a function of the DAC value for 50fC injected charge and adjustment preamplifier gain



50% trigger efficiency as function of the threshold

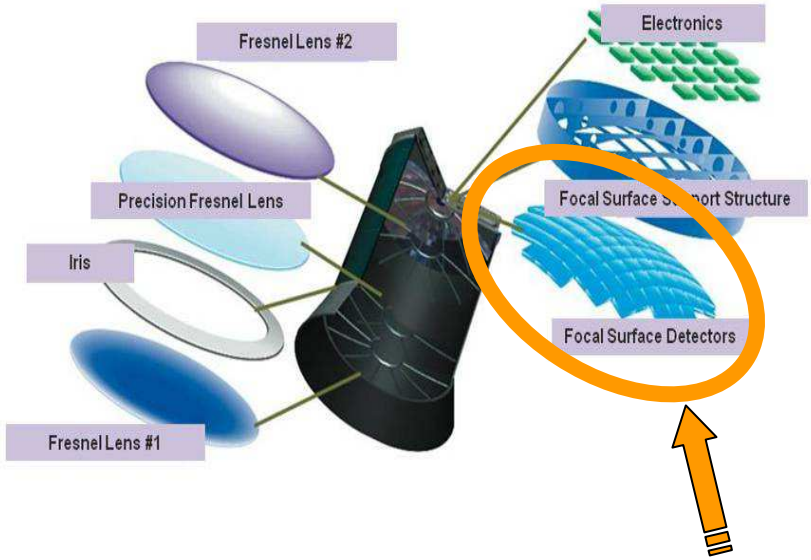


Variant (2010) : SPACIROC for JEM/EUSO

SPACIROC (Spatial Photomultiplier Array Counting and Integrating Read-Out Chip)

Main application: JEM-EUSO

- On board of the International Space Station (ISS)
- To study the ultra high energy cosmic rays.
- Detection system is a focal surface with around 5000 MAPMTs (64 ch)



ASIC Functions:

Analog part:

1. Photoelectron counting (20-50MHz)
2. Q-to-T converter (collab.JAXA/Riken)

Digital part :

1. Digitization,
2. Memory,
3. Send data to FPGA for triggering

Crucial points

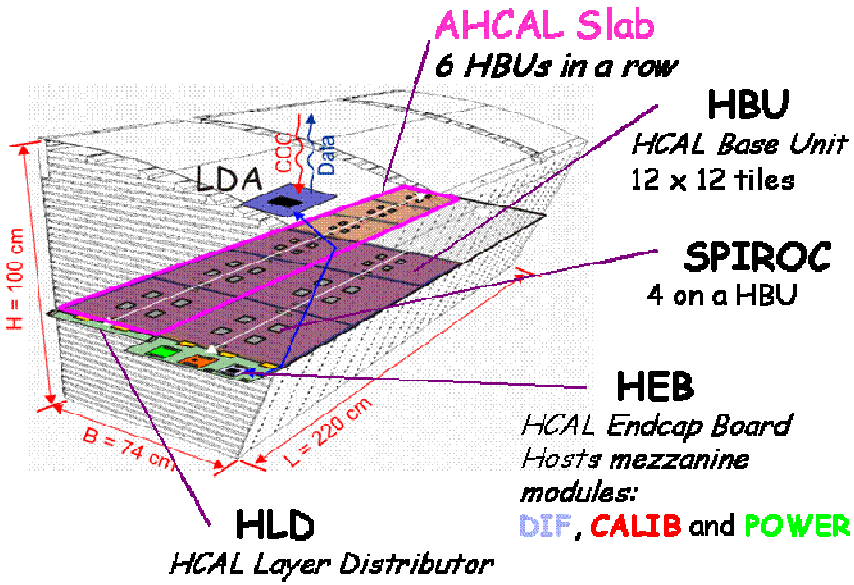
- **Power consumption < 1 mW/ch**
- data flow ~ 384 bits / 2.5 µs
- **Radiation tolerance** : triple voting
- Will be used on a balloon prototype

More information (SPACIROC): ahmad@lal.in2p3.fr

SPIROC for SiPM

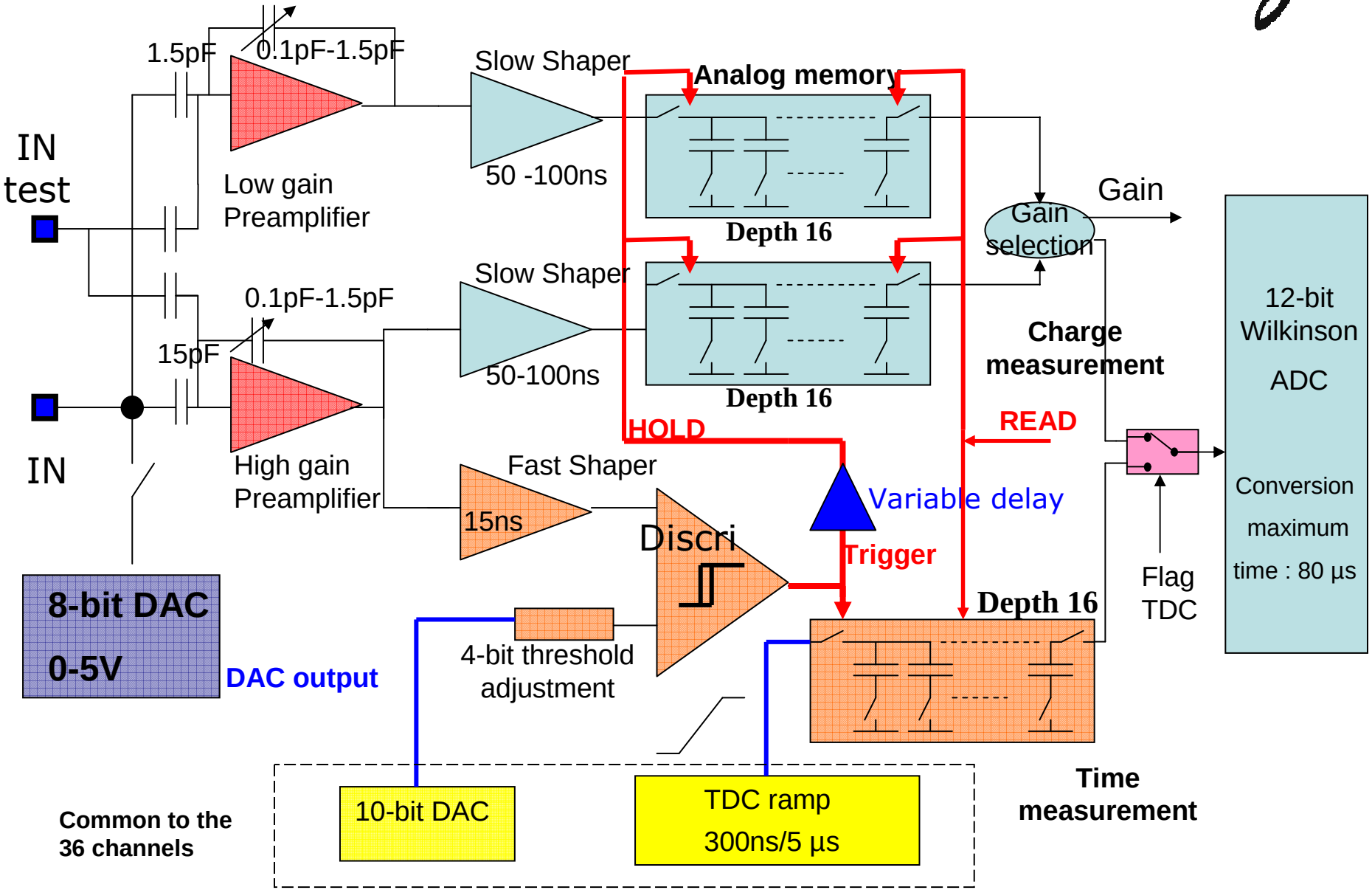
- SPIROC : Silicon Photomultiplier Integrated Read-Out Chip
- Developed to read out the Analog Hadronic CALorimeter (AHCAL) for CALICE (ILC)
- Prototype in development at DESY (EUDET/AIDA project)
- Large detector with huge number of channels (8 millions)
- Chip embedded in detector :
  → Power consumption is an important issue (25µW/ch)
  → few external components
- The first version in 2007 → First chip to readout SiPM detectors

(0.36m)² Tiles + SiPM + SPIROC (144ch)



More information (SPIROC): raux@lal.in2p3.fr; callier@lal.in2p3.fr

SPIROC general schematic

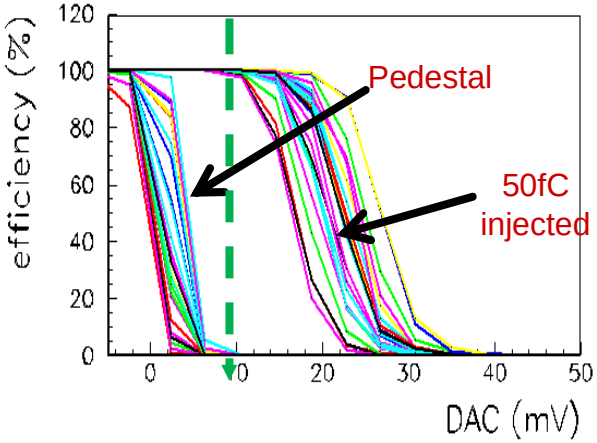


SPIROC - main features

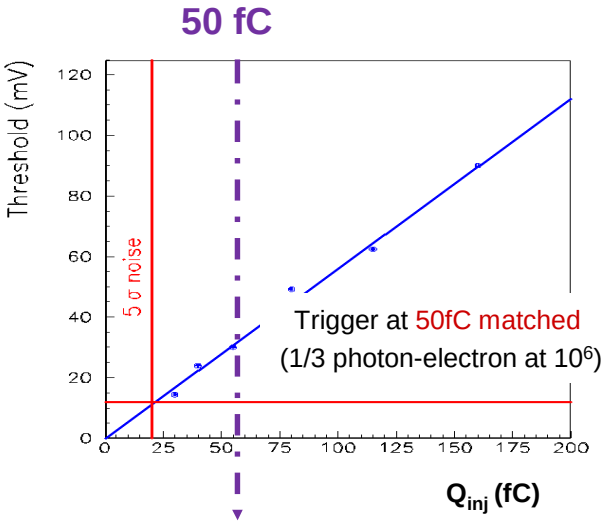
- SoC (System on Chip)
- 36-Channel ASIC
- Internal input 8-bit DAC (0-5V) for individual SiPM gain adjustment
- Energy measurement : 14 bits
  - 2 gains (1-10) + 12 bit ADC : 1 pe → 2000 pe
  - Variable shaping time from 25 ns to 175 ns
  - pe/noise ratio : ~11
- Auto-trigger on MIP or on single photo-electron
  - pe/noise ratio on trigger channel : ~24
  - Fast shaper : ~10 ns
  - Auto-Trigger on 1/3 pe (50fC)
- Time measurement :
  - 12-bit Bunch Crossing ID (coarse time)
  - 12-bit step ~ 1 ns TDC->TAC (fine time)
- Other features:
  - Analog memory for time and charge measurement : depth = 16
  - Low consumption : ~25 µW per channel (in power pulsing mode)
  - Embedded features (bandgap, 10-bit DAC, etc.)
  - Multiplexed analog output for physics prototype DAQ
  - 4 kbytes internal memory and daisy chain readout

SPIROC - measurements

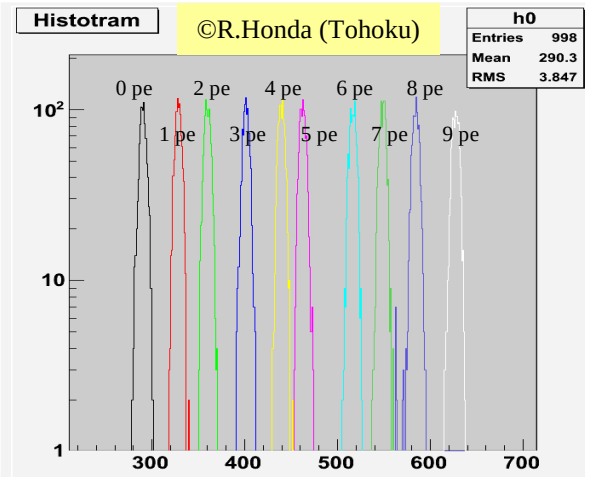
36-channel S-curves: trigger efficiency versus threshold (1 LSB = 2 mV)



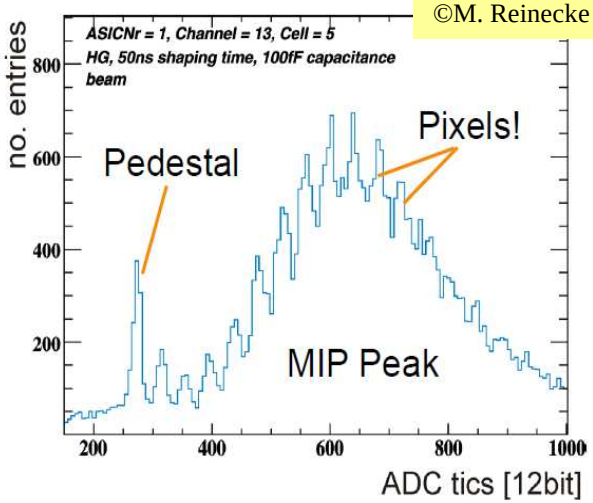
50 % Trigger efficiency point vs Q_{inj}

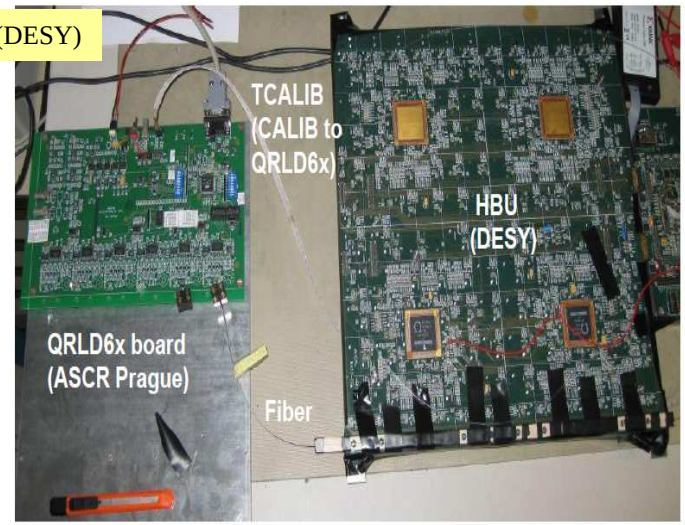


Response with different injected charges

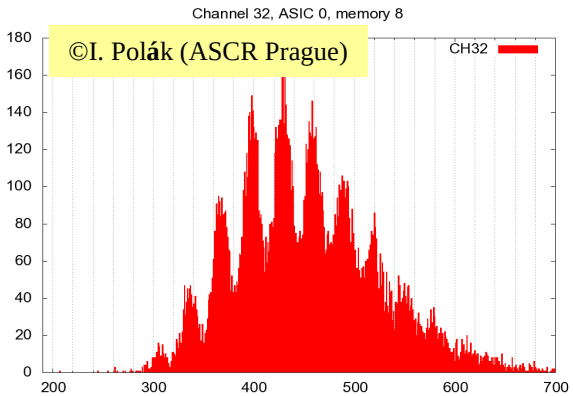


MIP response in DESY 6 GeV electron testbeam





Spectrum obtained with the LED calibration system

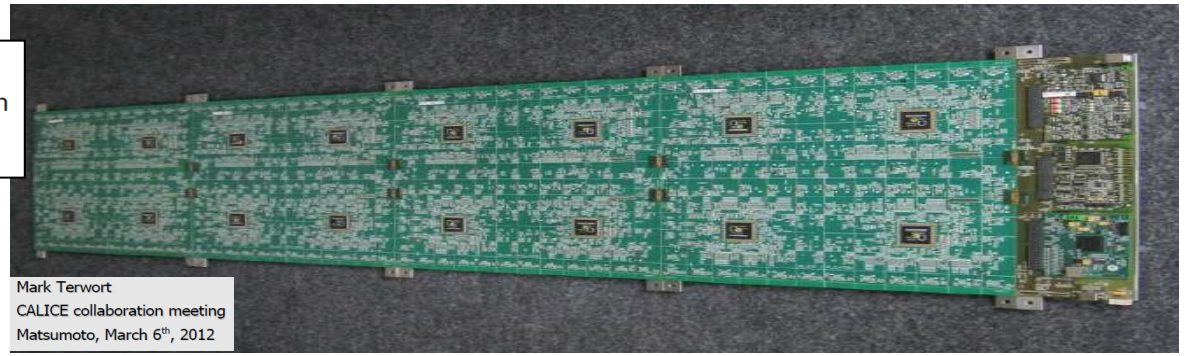


SPIROC - status

- 1000 chips produced in March 2010 to make a demonstrator (Large scale technological prototype)

4 **new HBUs** in DESY lab

→ 70 channels equipped with scintillator tiles, LEDs, SiPM readout, 4 ASICs

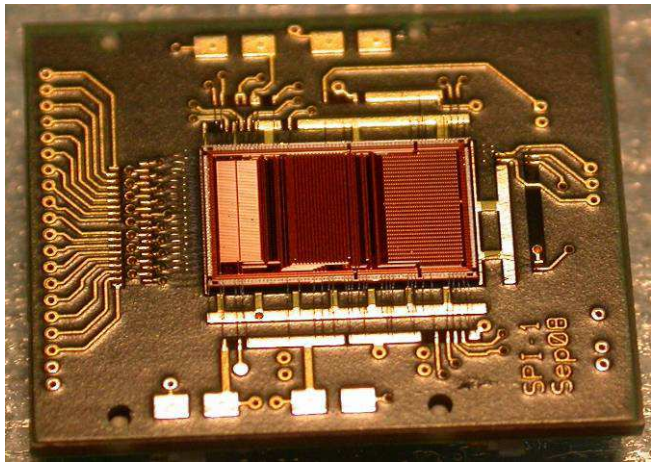


- Testbeam measurements (DESY) in May 2012 and next Fall

- A new version has been submitted in February 2012 and is expected in June 2012:
  SPIROC 2c: To study a new input stage + some improvements

- **EASIROC** : analog version of SPIROC in 2009

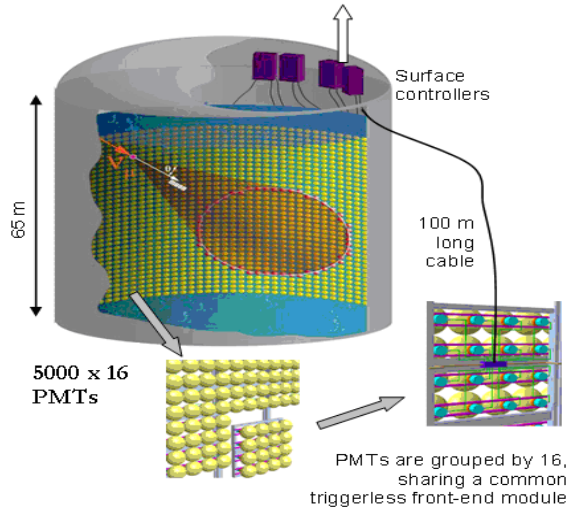
- **Many applications:**
  - **astrophysics PEBS (Aachen),**
  - **PET (Roma, Pisa, Valencia),**
  - **nuclear physics (KEK, Tohoku),**
  - **Vulcanology (Napoli,IPNL)**



PARISROC for large PMTs

- **PArISROC** stands for : Photomultiplier Array Integrated in SiGe Read-Out Chip
- Developed for PMm2 project
- A collaboration of 3 French laboratories (LAL, IPNO, LAPP) and the ULB Brussels (2009)
- Replace large PMTs (20”) by groups of 16 smaller ones (12”) **connected to an autonomous innovative front-end electronics.**
  - **Only one wire out (DATA + Supply)**
  - **Common High Voltage for PMTs**
- First prototype in 2008
- Second prototype in 2010 (to improve the performances)
- Main applications in large Water Cerenkov
- **Chip studied by LAGUNA (MENPHYS) (APC), LHAASO (IPNO and IHEP Beijing), HARPO (LLR), ATF2 (LAL).**

Demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu PMTs is **at APC now.**



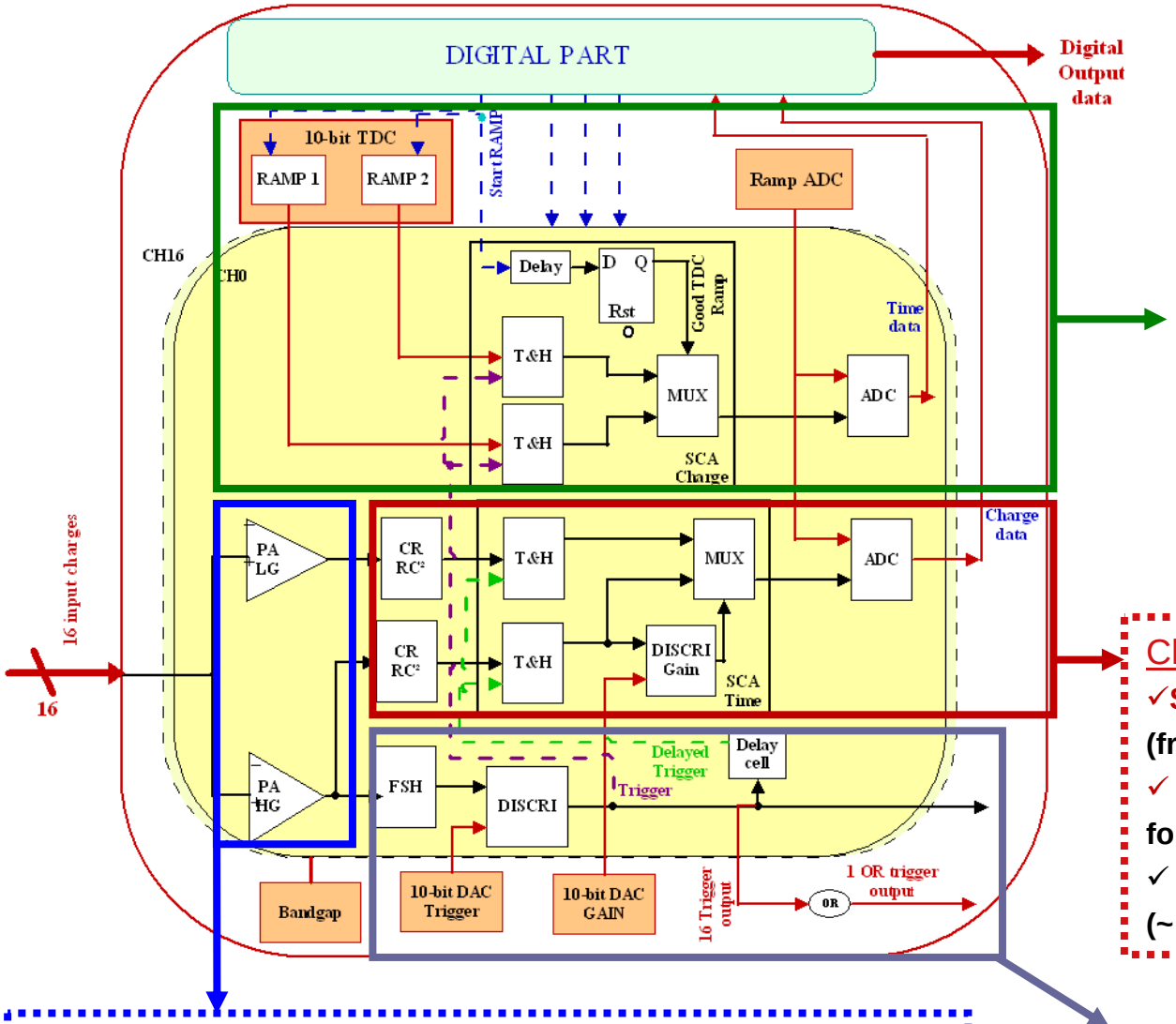
More information (PARISROC): conforti@lal.in2p3.fr; martin@lal.in2p3.fr

PARISROC - ASIC requirements

- SoC (System on Chip);
- Analog F.E. + charge and time digitization;
- 16 PMTs independent channels;
- 1/3 p.e. 100% trigger efficiency;
- Charge dynamic range 0 to 300p.e. (at PMT gain 10^6);
- 1 ns time stamping precision;
- Each channel has a variable gain to compensate gain vs HV spread for the 16 PMTs;
- Triggerless mode:

  All the PMTs signals above the threshold (1/3 p.e.) generate a trigger and are converted in digital data.
- 51 bits of data / hit channel that give information of: Channel #, coarse time, fine time, charge

PARISROC - general schematics



Time measurements

2 systems:

1. **Coarse time** by 24-bit gray counter (Digital part)
   - working at 10 MHz
   - with 1.67 s of dynamic
   - 100 ns steps
2. **Fine time** by analog **TDC**
   - ✓ 100 ns **dynamic range**
   - ✓ **Time resolution**: 170 ps
   - ✓ **Time precision**: +/- 1ns

Charge measurements

- ✓ **Shaper** with variable shaping time (from 25 ns to 100 ns) and gain
- ✓ **Charge resolution**: max 0.2 p.e. (32 fC) for 10-bit ADC
- ✓ **Dynamic range** from 1/3 pe to 600 pe (~ from 50 fC to 100 pC)

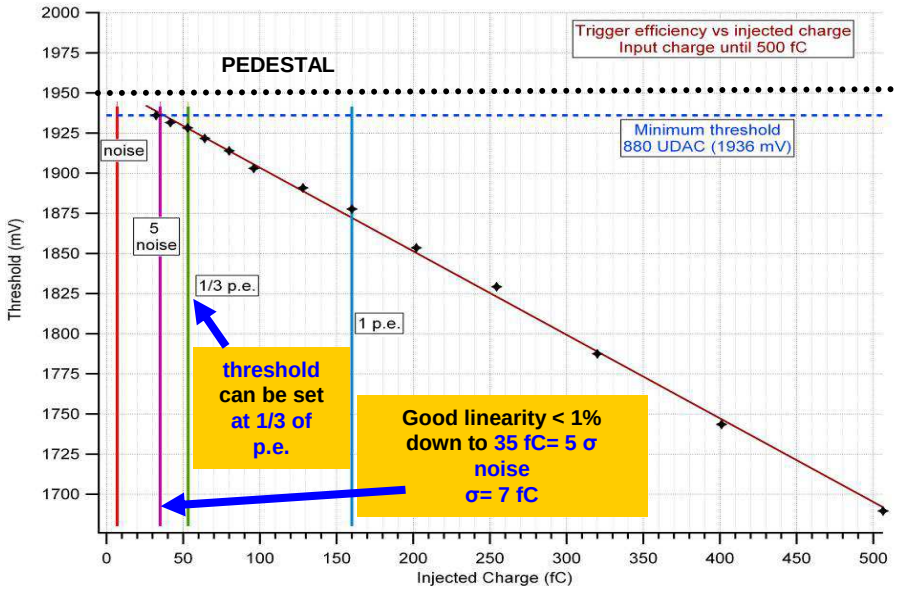
Input stage

- ✓ **Two gain channels** to cover the large input dynamic range
- ✓ 2 input preamplifiers with **adjustable gains** (on 8 bits)

Trigger channel

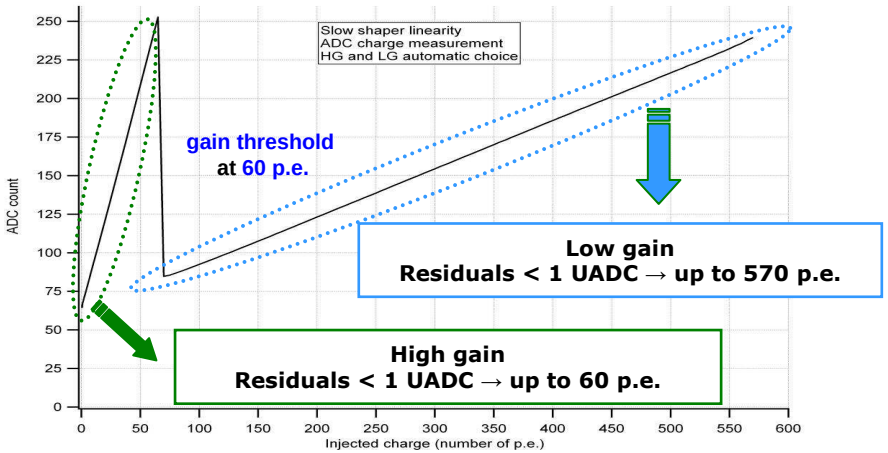
PARISROC - prototype characterization tests

50% Trigger efficiency as a function of the injected charge

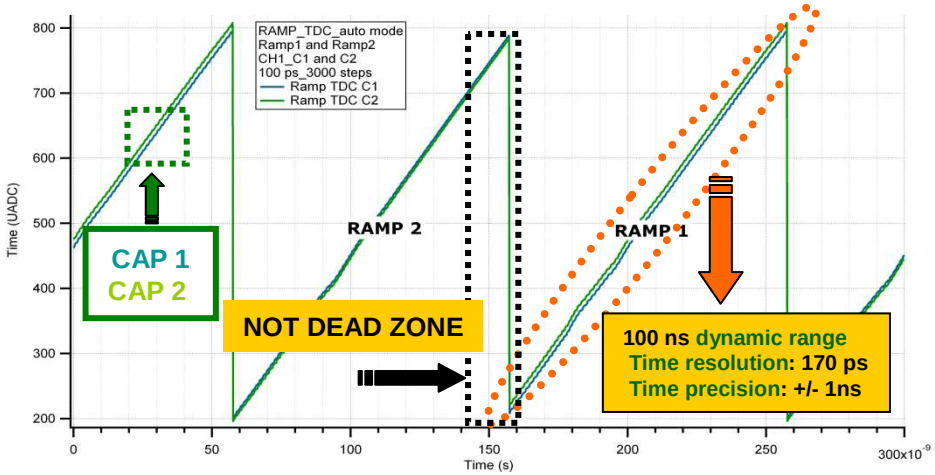


The whole chain is tested injecting a charge in the input: the signal is amplified, auto-triggered, held in the SCA cell and converted by 10-bit ADC

Auto-gain test (Charge measurements)



Time overall



Main publications

• S.ConfortiDiLorenzo,et al.," PARISROC, an autonomous front-end ASIC for triggerless acquisition in next generation neutrino experiments" NuclearInstruments&MethodsInPhysicsResearchSectionA(2011), doi:10.1016/j.nima.2011.11.028

• S. Drouet et Al, Subnano time to digital converter implemented in PARISROC for PMm2 R&D program, 2011 JINST 6 C01014.

• E. Wanlin et Al, PMm²: R&D on triggerless acquisition for next generation neutrino experiments, 2011 JINST 6 C01081.

• S.Conforti Di Lorenzo, PhD thesis. Développement et caractérisation d'un ASIC de lecture de macro-cellule de photo-détecteurs de grande dimension.LAL 10-152 (2010).

• F. Dulucq et Al, Digital part of PARISROC2: a photomultiplier array readout chip, 2010 JINST 5 C11004.

• S. Jakobsen, Nuclear Instruments & Methods In Physics Research Section A (2011), doi:10.1016/ j.nima.2011.10.017

• Sylvie Blin, Pierre Barrillon, Christophe de La Taille, "MAROC, a generic photomultiplier readout chip", IEEE Nuclear Science Symposium Conference Record (NSS/MIC), pp. 1074-1081 (2010), 10.1109/NSSMIC.2010.5874062 .

• P. Barrillon et Al, "PMF : the front end electronic of the ALFA detector", 10.1016/j.nima.2010.03.037

• Lucotte A., Blin S., Borer K., Campagne J.E., Cazes A., Hess M., de La Taille C., Martin-Chassard G., Raux L., Repellin J.P, "A front-end readout chip for the OPERA scintillator tracker"; NIMA 521-378-392 (2004) et LAL-RT 03-87.

• Salleh Ahmad et Al, "SPACIROC: A Front-End Readout ASIC for JEM-EUSO cosmic ray observatory" TIPP11-D-11-00047R1

• Callier, S.; Dulucq, F.; Fleury, J.; Jaeger, J.-J.; de La Taille, C.; Martin-Chassard, G.; Raux, L., "SPIROC (SiPM Integrated Read-Out Chip): Dedicated very front end electronics for an ILC prototype hadronic calorimeter with SiPM read-out", (TWEPP10) 2011_JINST_6_C01098 .

• C. de La Taille, G. Martin-Chassard and L. Raux, FLC SIPM: front-end chip for SIPM readout for ILC analog HCAL, in International Linear Collider Workshop, Stanford, U.S.A. (2005).

• Stéphane Callier; Ludovic Raux; Christophe de La Taille; Gisèle Martin-Chassard, "EASIROC, an easy & versatile readout device for SiPM", TIPP11-D-11-00006R1

Conclusion

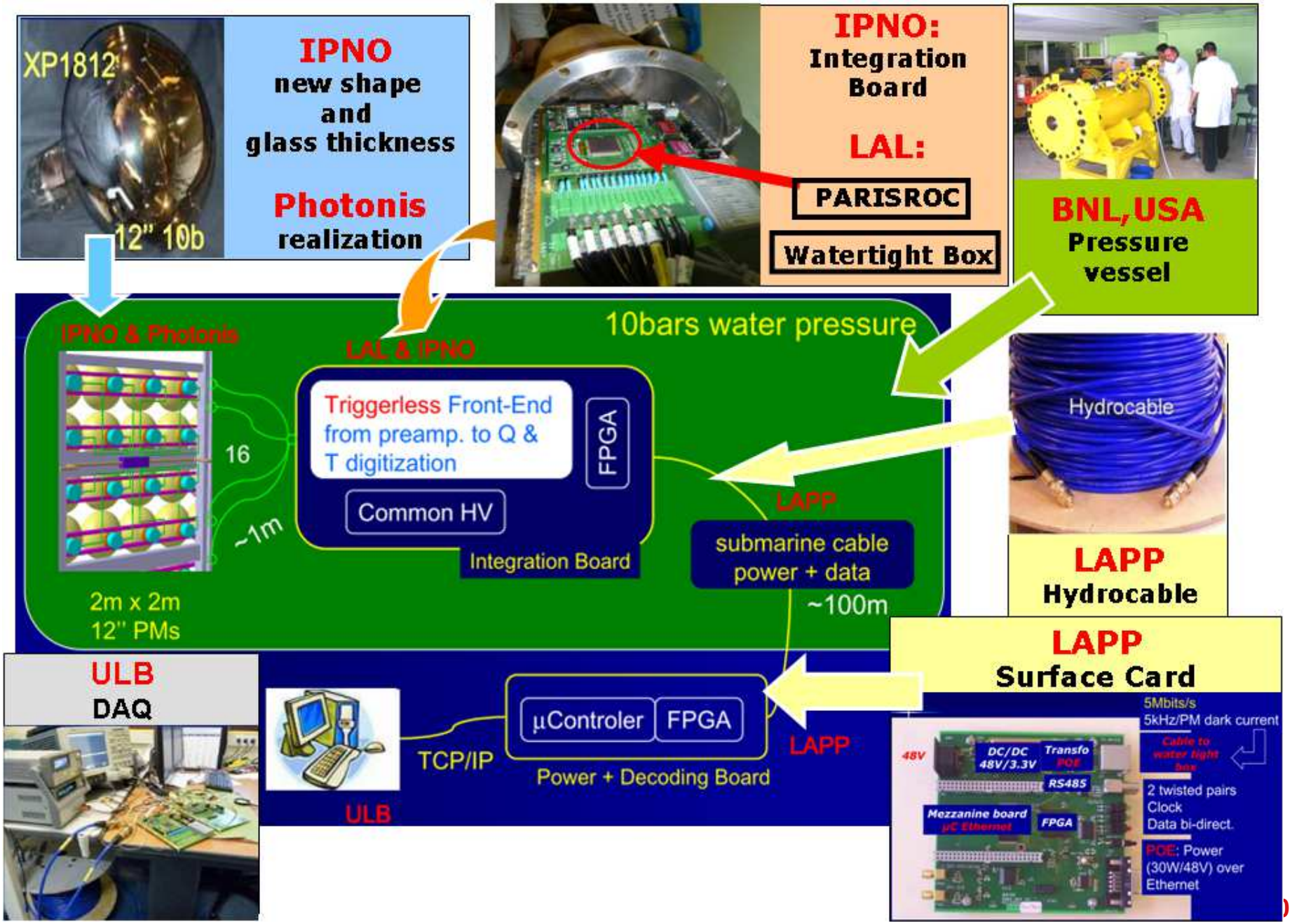
- A "ROC" family of complementary ASICs has been designed by the OMEGA group (http://omega.in2p3.fr/)
- Used to read all sorts of photo-detectors (PMTs, MAPMTs, SiPM, etc…)
- Extensive measurements performed on MAROC, PARISROC and SPIROC show that they fulfill the stringent requirements of the future photodetectors, in particular in terms of low noise, large dynamic range and high speed while keeping low power thanks to the SiGe technology.
- The versatility of these chips and the internal digitization seduce many (~ 30 different groups around the world) users of various fields as high energy physics, nuclear physics, medical imaging, vulcanology, etc…

ASICs summary

ASIC name	PARISROC2	MAROC	SPACIROC	SPIROC	EASIROC
Current available version	2	2-3	1	2A - 2B	1
# channels	16	64	64	36	32
input signal polarity	negative	negative	negative(anodes), positive(dynode)	positive	positive
Detector read out	Array of large PMTs compliant with MA-PMT, SiPM, MPPC	MA-PMT, PM, SiPM, MPPC	MAPMTs	SIPM, MPPC, compliant with PM, MA-PM	SIPM, MPPC, compliant with PM, MA-PM
Maximum input (charge)	600pe at minimum gain	200 pe at minimum gain	200 pe at minimum gain	2000 pe at min gain	2000 pe at min gain
Minimum input (trigger)	1/3 pe	< 1/32 pe	< 1/3 pe	< 1/3 pe	< 1/3 pe
Input	Voltage sensitive	Charge sensitive	Charge sensitive	Voltage sensitive	Voltage sensitive
Outputs	•digital charge and time •OR of the 16 triggers •16 Triggers outputs	•64 Triggers outputs •multiplexed analogue output •OR of the 64 triggers	• Digital photon counting & time-over-threshold •OR of 64 triggers	•digital charge and time •multiplexed analogue output •OR of the 36 triggers	•multiplexed Charge outputs (HG/LG) •32 Triggers outputs •multiplexed 32 triggers output •OR of the 32 triggers

PARISROC

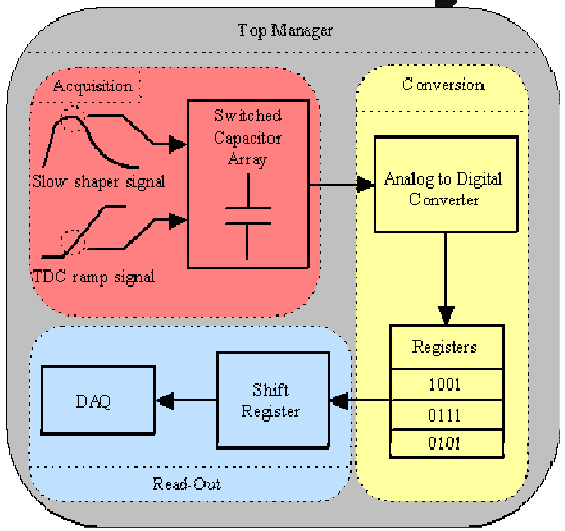
PMm² general description



PARISROC digital part

4 modules: ***Acquisition, Conversion, Read Out and Top manager***.

- ✓ **Acquisition**: Analog memory
- ✓ **Conversion:** Analog charge and time into 10 bits digital value saved in register (RAM)
- ✓ **Read Out:** RAM read out to an external system



SELECTIVE READOUT

- ✓ Only hit channels are readout
- ✓ Readout clock : 40 MHz
- ✓ Max Readout time (16 ch hit) : 25 µs
- ✓ 51 bits of data / hit channel
- ✓ 5 kHz hit rate

	PARIROC 2
Conversion Time	26 µs
Readout Time	25 µs
Total cycle duration	51 µs

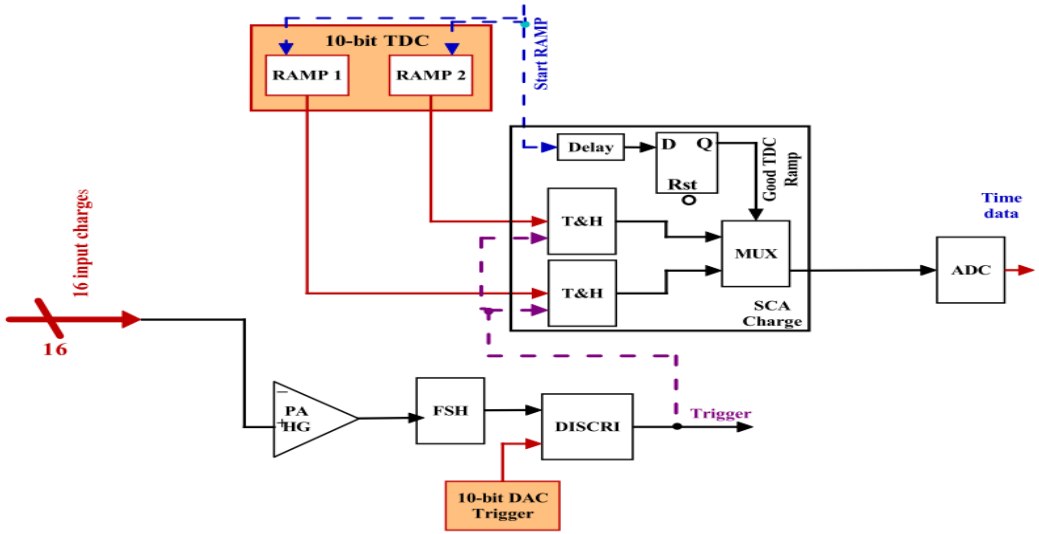
	PARIROC 2
Channel number	4
Coarse time counter	24
Extra Coarse time	1
Gain used	1
Charge converted	10
Fine time (TDC) used	1
Fine time (TDC) converted	10
Total	51 bits

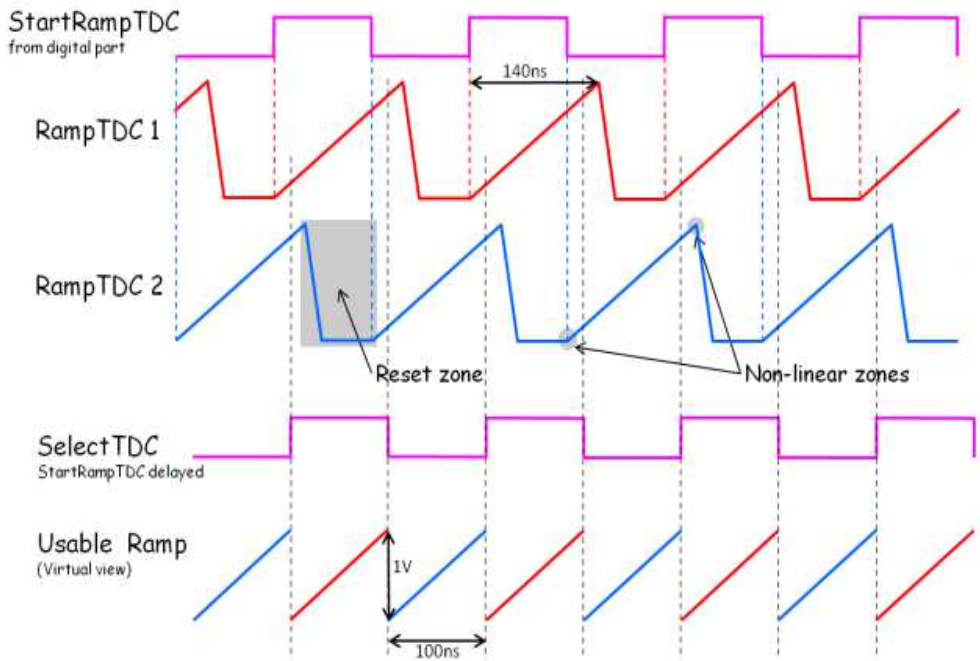
• F. Dulucq, et al., Digital part of PARISROC2: a photomultiplier array readout chip, JINST5 (2010) C11004.

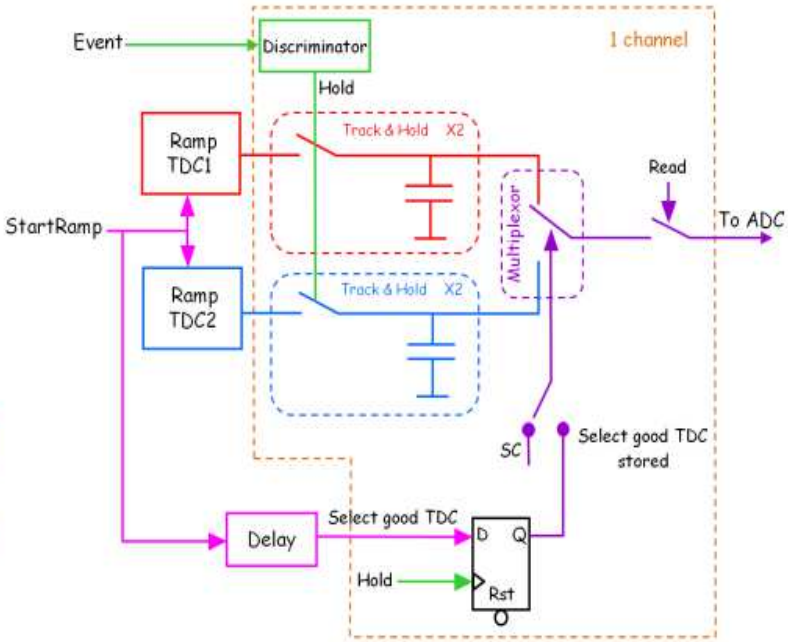
2 systems:

1. Coarse time by 24-bit gray counter
- working at 10 MHz
- with 1.67 s of dynamic
- 100 ns steps

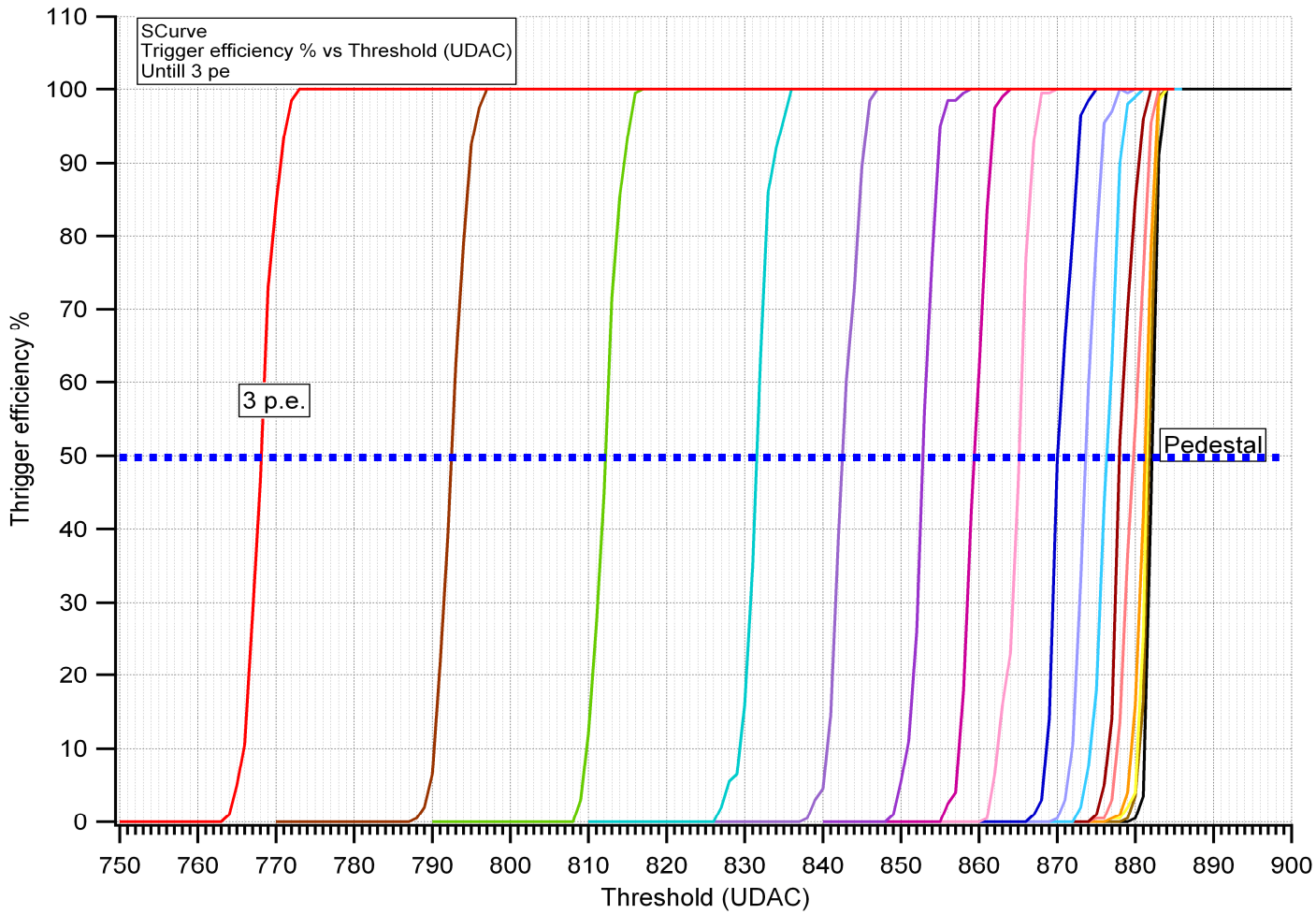
2. Fine time by analog TDC
- 100 ns dynamic
- 220 ps step



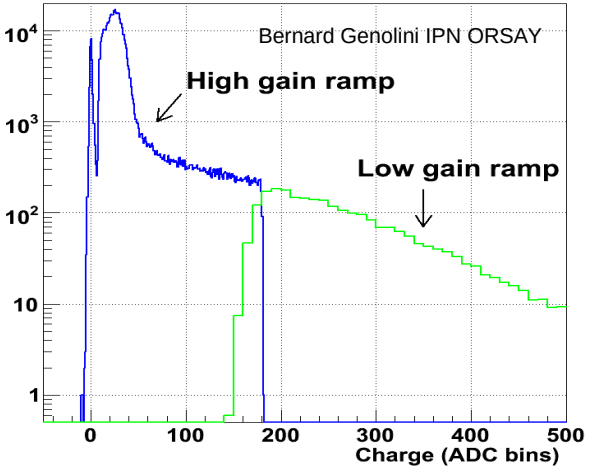




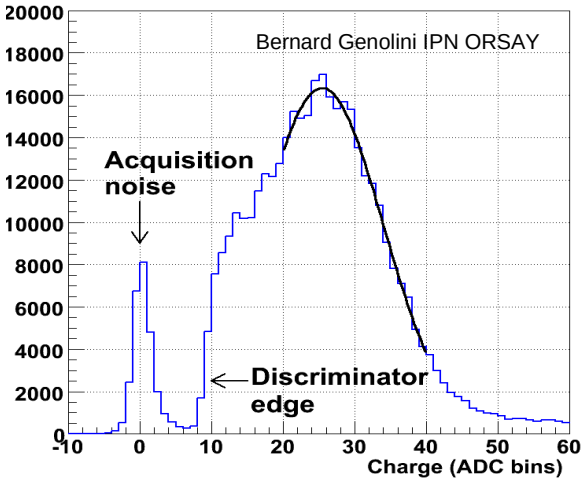
Trigger efficiency of one channel as a function of the injected charge at different threshold value



8-in (Hamamatsu R5912) HV 1550 V, gain $3x10^6$
Single p.e. noise spectrum.
Blue: high gain channel; Green: Low gain channel.



8-in (Hamamatsu R5912)
HV 1550 V, gain $3x10^6$
Single p.e. noise spectrum.



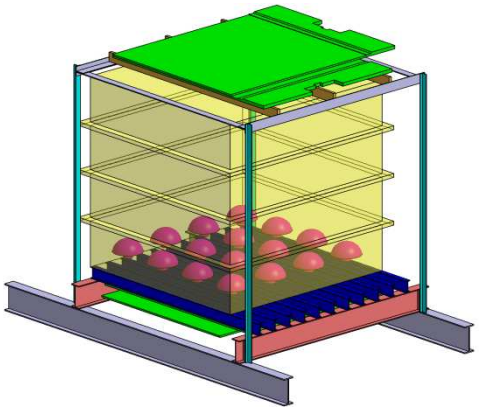
✓ The idea of the PMm2 project to perform a new generation of "smart photo-detectors" composed by sensor and readout electronics has been demonstrated thanks an important interdisciplinary collaboration
✓ The PARISROC ASIC has fulfilled the project requirements and it is available to be used in real detector

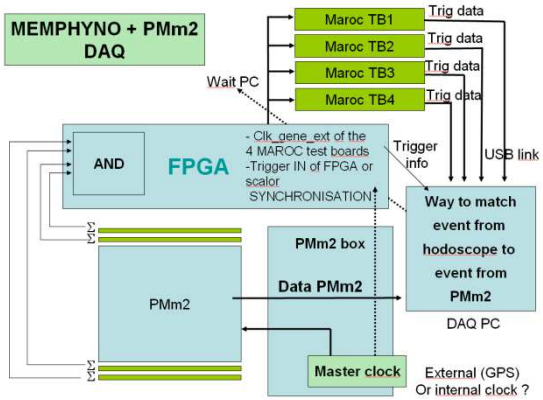
ASIC cost consideration indicates:

- ✓ For PARISROC first prototype fabrication we have spent:
  17k € for 25 dies of 17 mm² packaged → ~ 700 €/chip (44 €/channel)
  (the price is a function of the surface of the dies, around 1k €/ mm²)
- ✓ For another version of PARISROC → 2 years and around 50k € for 2 chips prototype + test board
- ✓ For mass production the cost decrease to:
  → 150 €/chip (10 €/channel) for 1'000 chips
  → 10 €/chip (0.7 €/channel) for 100'000 chips

Detailed study of costs must be done on the PMm2 box including cables, submarine and surface board and PMTs

Demonstrator realized by the IPNO with 16 x 8-inch Hamamatsu tubes is **at APC now.**
Future test will be performed with this demonstrator and the PARISROC ASIC and it might be used by **MEMPHYNO** collaboration.





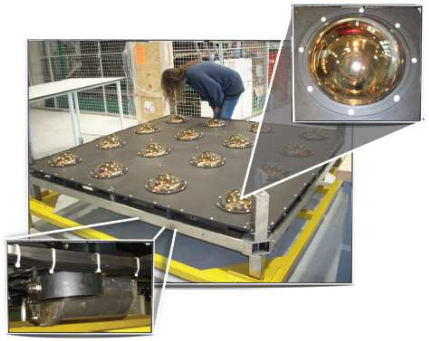


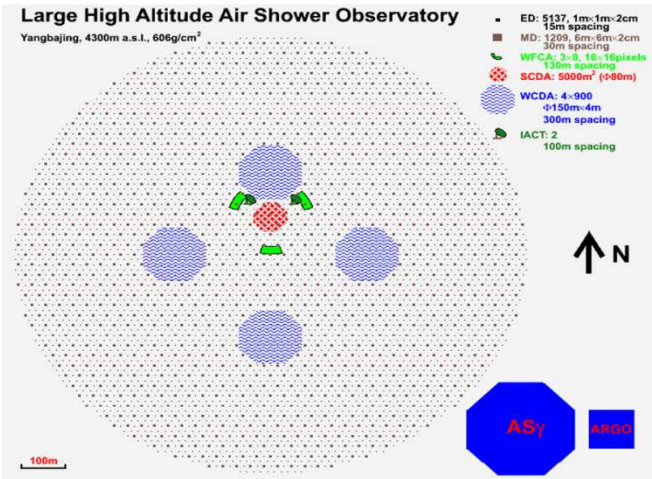
Figure 7.11: PMm2 demonstrator at APC: 16 PMTs organized in a matrix with common electronics and power supply.

• Michela Marafini, PhD thesis. Physics studies and R&D towards the MEMPHYS experiment: a water Cerenkov Detector in Europe.

LHAASO

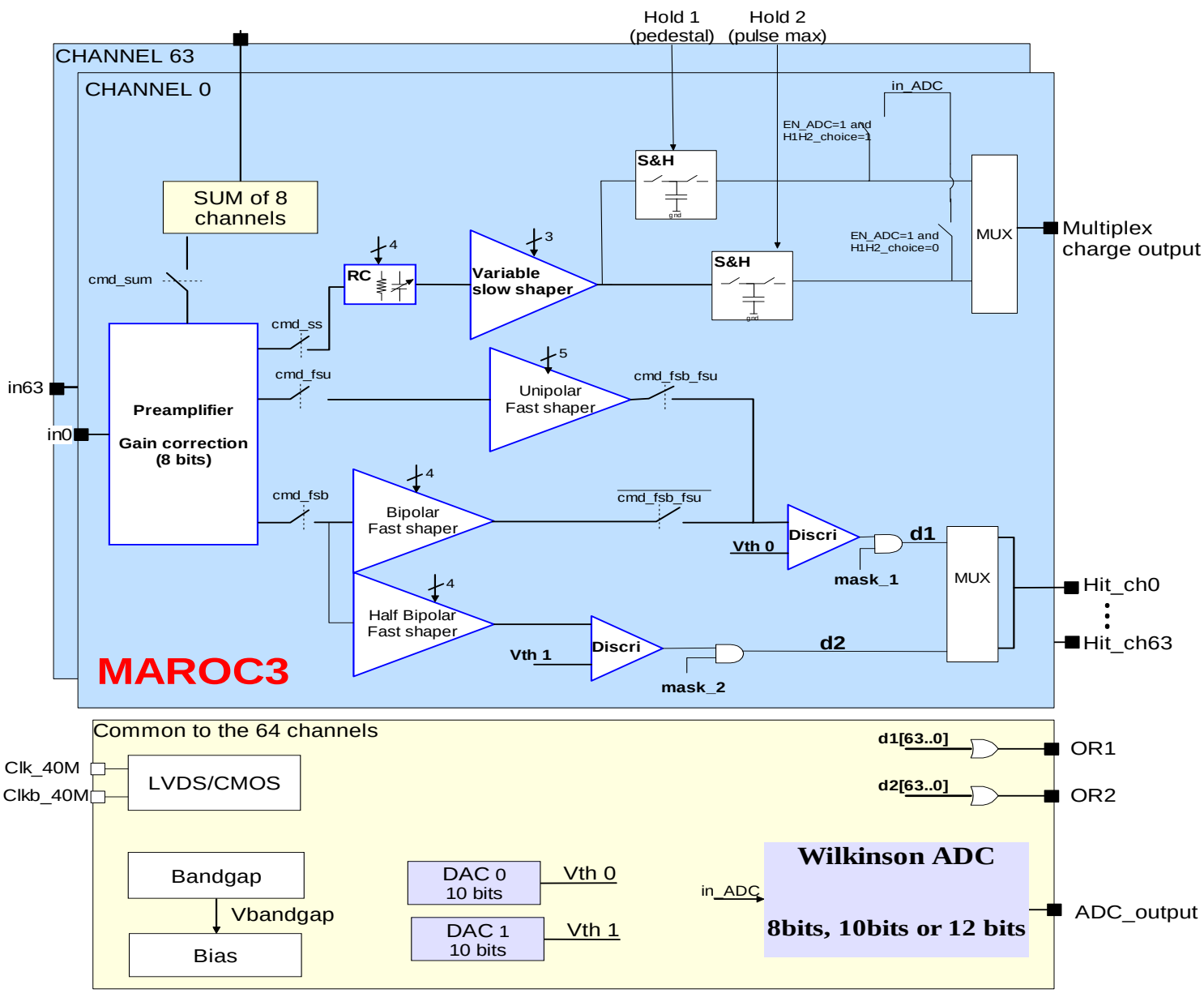
LHAASO (*Large High Altitude Air Shower Observatory*)

PARISROC 2 **PMT gain 10^6**
Input signal: negative
Single channel hit rate: 5 kHz
Charge dynamic range: 1- 600 p.e. (100 pC)
Resolution: <20%@1pe
Disc threshold: 0.3 pe (50 fC)
Timing resolution: 220 ps
Timing precision < 1 ns



- **PARISROC 2 could be used to check the LHAASO sub-detectors performances**
- **A test board and a PARISROC2 chip will be tested at IHEP- Institute of High Energy Physics, Beijing, China**
- **Modifications of PARISROC2 could be carried out in the next years to achieve the LHAASO sub-detectors requirements**

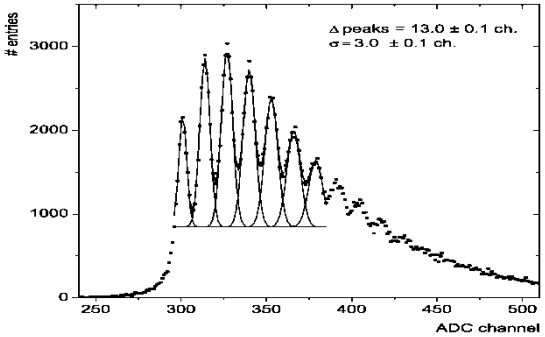
MAROC

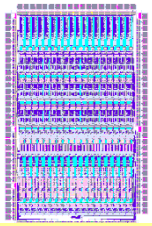

Hold 1
(pedestal)
Hold 2
(pulse max)
CHANNEL 63
CHANNEL 0
in_ADC
EN_ADC=1 and
H1H2_choice=1
S&H
SUM of 8
channels
EN_ADC=1 and
H1H2_choice=0
MUX
Multiplex
charge output
cmd_sum
RC
Variable
slow shaper
S&H
cmd_ss
in63
in0
Preamplifier
Gain correction
(8 bits)
cmd_fsu
Unipolar
Fast shaper
cmd_fsb_fsu
cmd_fsb
Bipolar
Fast shaper
cmd_fsb_fsu
Vth 0
Discri
d1
mask_1
MUX
Hit_ch0
Hit_ch63
Half Bipolar
Fast shaper
Vth 1
Discri
d2
mask_2
MAROC3
Common to the 64 channels
Clk_40M
Clkb_40M
LVDS/CMOS
d1[63..0]
OR1
d2[63..0]
OR2
Bandgap
Vbandgap
Bias
DAC 0
10 bits
Vth 0
DAC 1
10 bits
Vth 1
in_ADC
Wilkinson ADC
8bits, 10bits or 12 bits
ADC_output

SPIROC

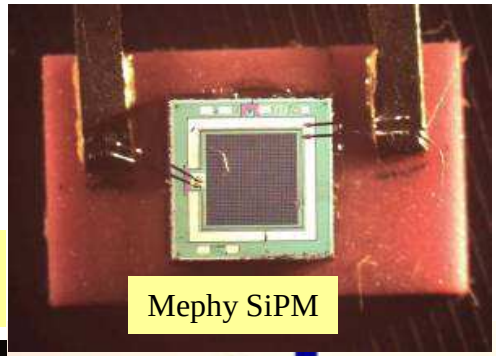
CALICE AHCAL testbeam physics prototype

- **SPIROC** is the second generation for SiPM readout
- The first generation **FLC_SiPM** was designed to equip the Analog H-Cal physics prototype for the ILC: 1 cubic meter, 38 layers, 2cm steel plates
- **8000 tiles with SiPM** fabricated by MePHY group

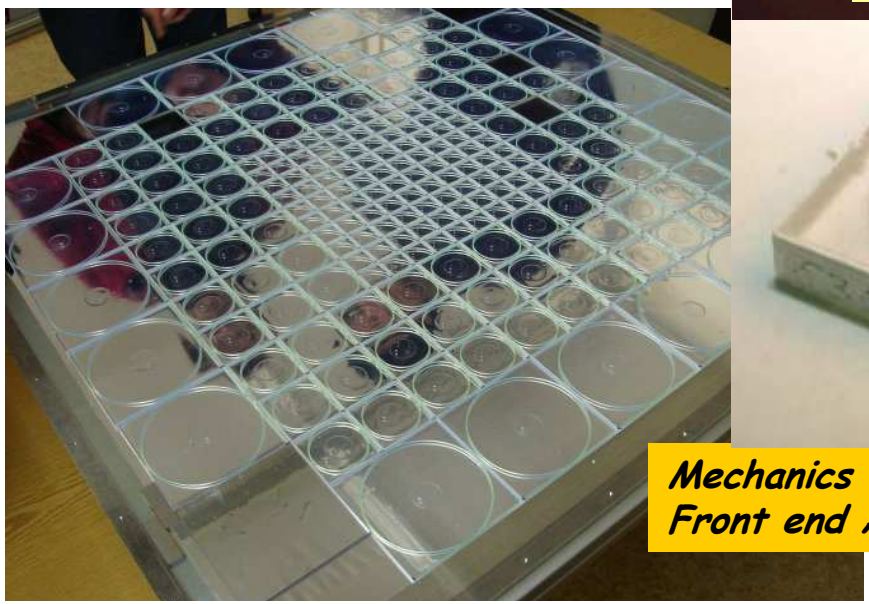


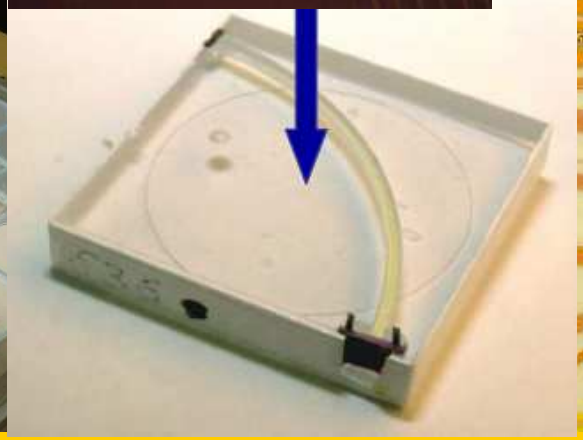


FLC_SiPM ASIC



Mephy SiPM



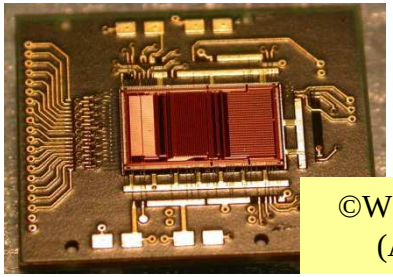


Mechanics and front end boards: DESY
Front end ASICs: LAL

Also used with W/Sci SiPM japanese ECAL with MPPCs

SPIROC saga….

- **200 chips SPIROC 1 produced in Nov 2007**
  - Package PQFP240
  - Good analog performance
  - Bug in ADC ramp : no digital data out



©W. Karpinski (Aachen)

- **50 chips SPIROC 2 produced in June 2008 to equip AHCAL and ECAL EUDET modules**
  - **EUDET milestone**
  - Package TQFP208
  - Difficult slow control loading

PEBS experiment Aachen University

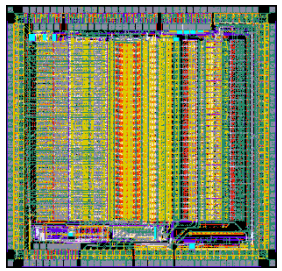
- **Full CALICE production run : April 2010 (Chip delivery Sept. 2010)**
  - **SPIROC 2a** (1200 chips) : conservative prototype in which the major bugs of SPIROC 2 are fixed
  - **SPIROC 2b** (1200 chips) : more agressive prototype in which the major bugs of SPIROC 2 are also fixed and some interesting improvements are added (in particular the independent gain adjustment channel by channel)
  - **SPIROC A** (3600 chips) : "light" analog version of SPIROC users who don't need the digital core.

MU-RAY project INFN Napoli

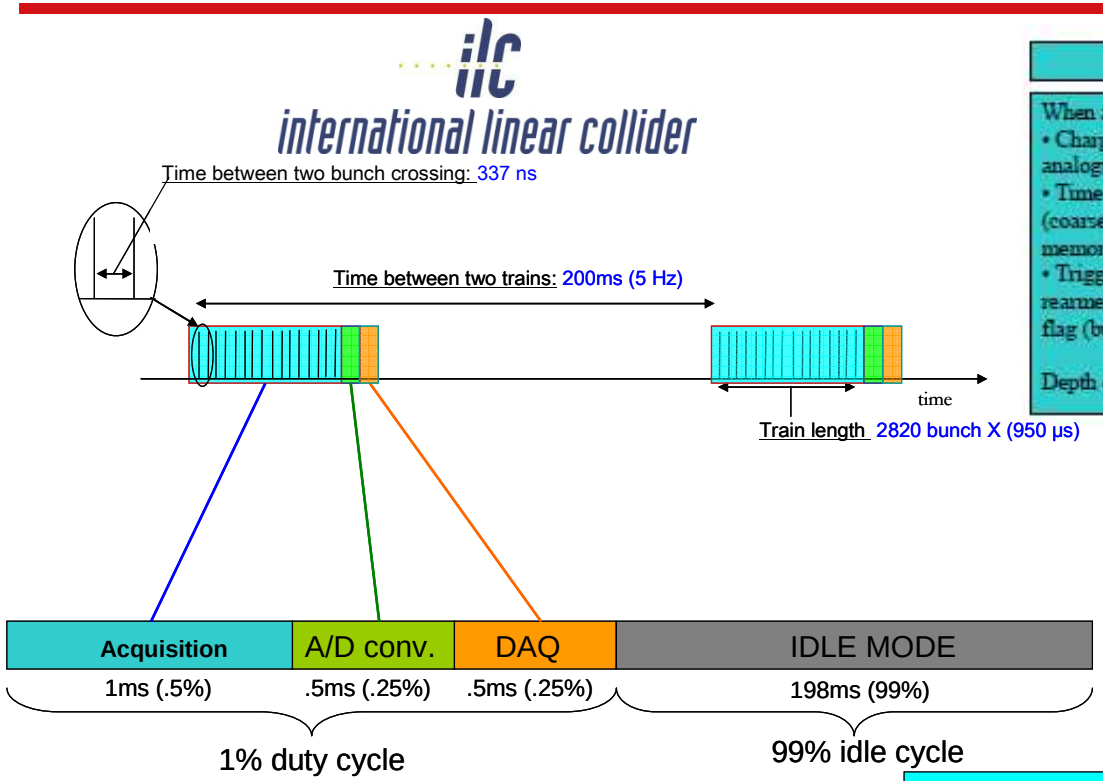
- **Others applications using SPIROC chips**
  - astrophysics PEBS experiment (Aachen University),
  - medical imaging (Roma, Pisa, INMC Orsay, Valencia, etc.)
  - Nuclear physics (IPNO, KEK)
  - Vulcanology: Muon radiography of geological structures (INFN Napoli)

SPIROC A

Fabricated in SiGe AMS 0.35 µm
Submitted in September 2009
Delivered in December 2009
Chip area: 17 mm² (4.2 mm × 4.1 mm)

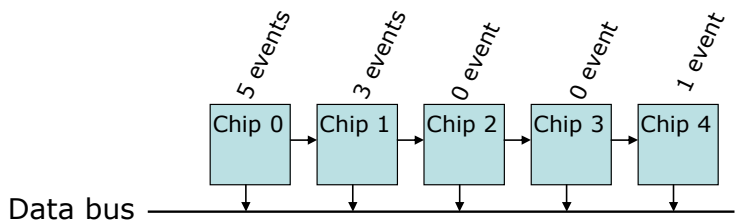


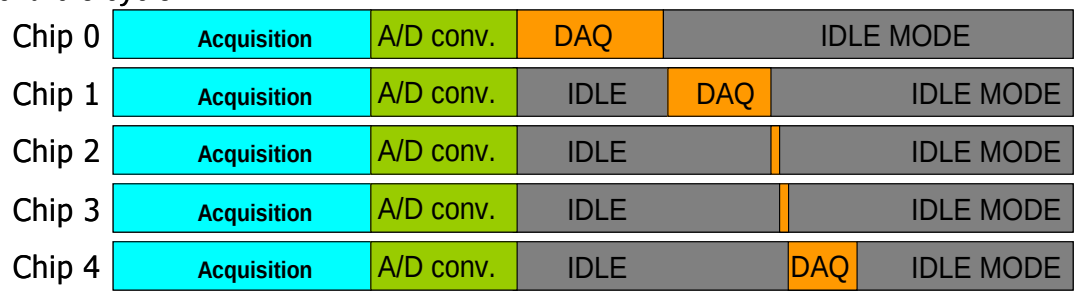
ILC beam structure and SPIROC running modes



Acquisition	A/D conversion	DAQ
When an event occurs : • Charge is stored in analogue memory • Time is stored in digital (coarse) and analogue (fine) memory • Trigger is automatically rearmed at next coarse time flag (bunch crossing ID) Depth of memory is 16	The data (charge and time) stored in the analogue memory are sequentially converted into digital data and stored in a SRAM.	The events stored in the RAM are readout through a serial link when the chip gets the token allowing the data transmission. When the transmission is done, the token is transferred to the next chip. 256 chips can be read out through one serial link

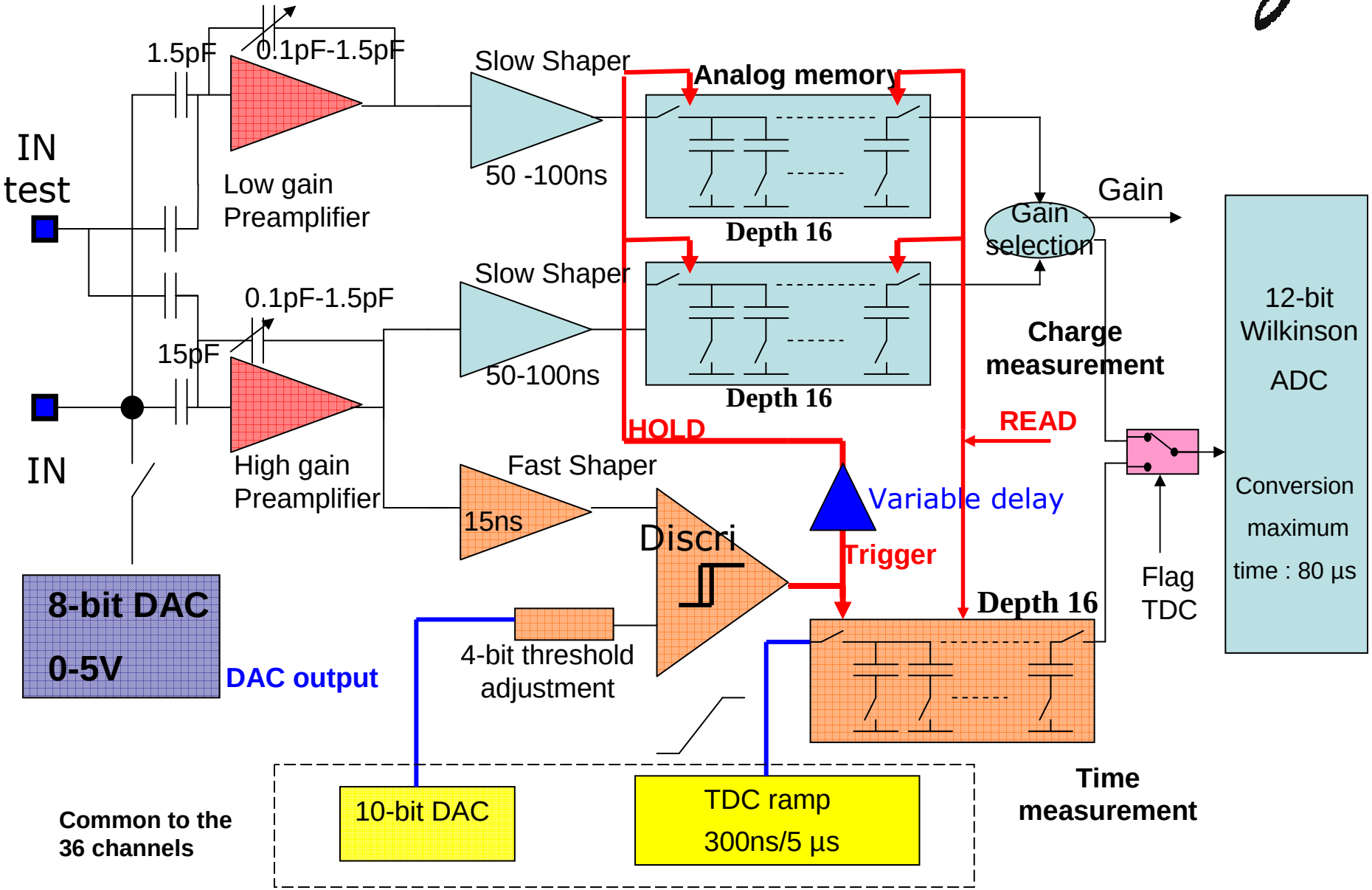
- **Readout based on token ring mechanism initiated by DAQ**
- **One data line activated by each chip sequentially**
- **Readout rate few MHz to minimize power dissipation**

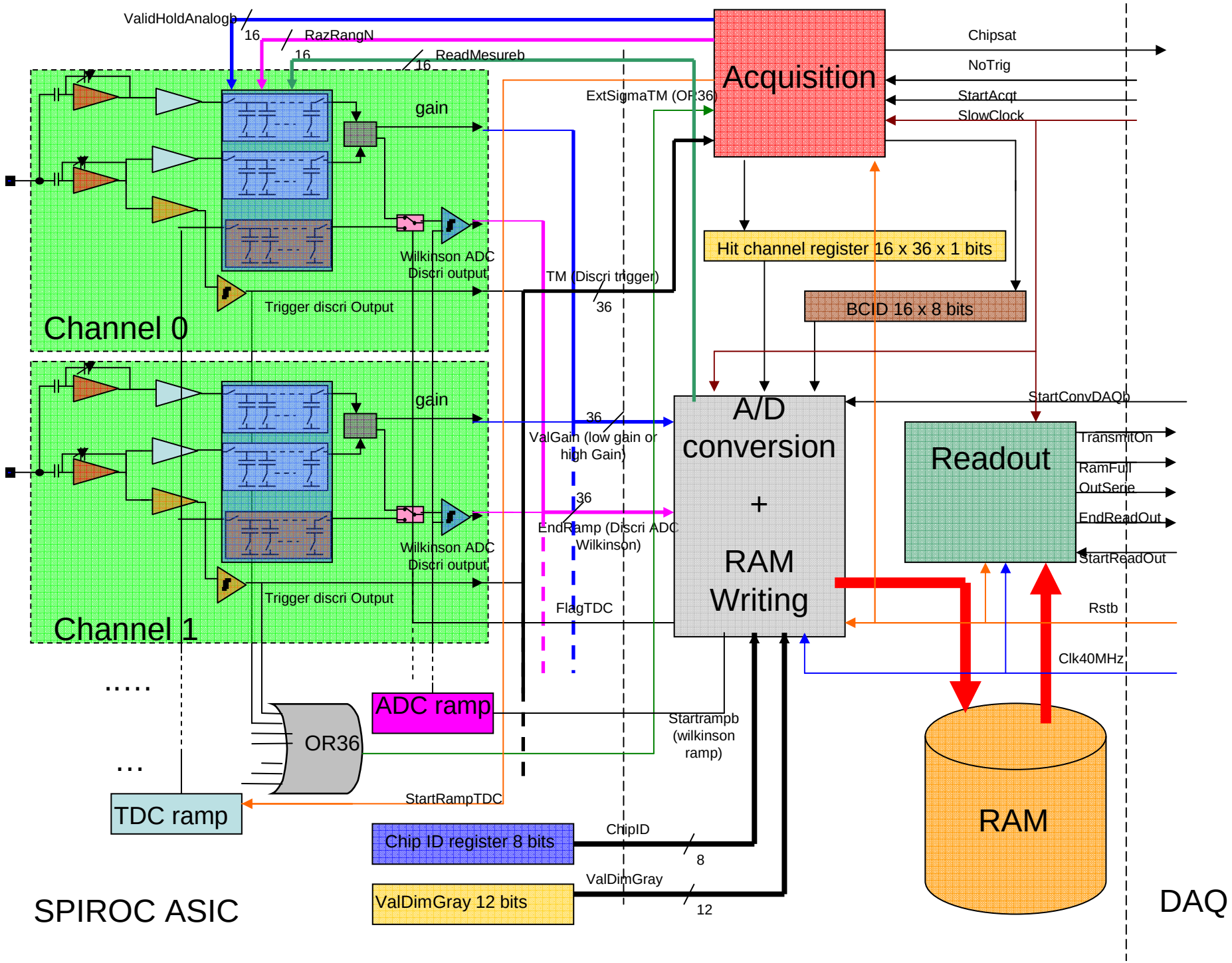




Two orders of magnitude saved on the consumption by using the ILC beam structure and the power pulsing

SPIROC : One channel schematic




ValidHoldAnalogb
16
RazRangN
16
ReadMesureb
16
Acquisition
Chipsat
NoTrig
StartAcqt
SlowClock
ExtSigmaTM (OR36)
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 0
TM (Discri trigger)
36
Hit channel register 16 x 36 x 1 bits
BCID 16 x 8 bits
gain
Wilkinson ADC
Discri output
Trigger discri Output
Channel 1
36
ValGain (low gain or
high Gain)
36
EndRamp (Discri ADC
Wilkinson)
FlagTDC
A/D
conversion
+
RAM
Writing
StartConvDAQb
Readout
TransmitOn
RamFull
OutSerie
EndReadOut
StartReadOut
Rstb
Clk40MHz
.....
...
OR36
ADC ramp
Startrampb
(wilkinson
ramp)
TDC ramp
StartRampTDC
Chip ID register 8 bits
ChipID
8
ValDimGray
ValDimGray 12 bits
12
RAM
SPIROC ASIC
DAQ

SPIROC Input DAC

- Input DAC to optimize SiPM bias voltage
- 8-bit DAC, 5V range
- LSB=20mV
- 36 DAC (one per channel)
- Ultra low power (<1µW) : no power pulsing
- Can sink 10 µA leakage current
- Linearity : ± 1%
- DAC uniformity between the 36 channels : ~3%