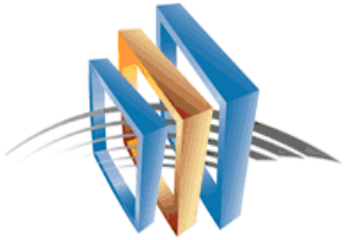


Talent

WP3:
Development of radiation-hard high-density electronics and interconnection with sensors

Norbert Wermes, University of Bonn

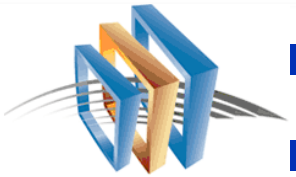
universitätbonn

SI LAB
Silizium Labor Bonn

Objectives

- WP3: **Development of radiation-hard high-density electronics and interconnection with the sensors**: design, prototyping and testing of **ASIC** mixed circuit analogue-digital **chips**, the assembly of highly integrated **modules** and implementation of **quality-assurance** protocols for the production of high-reliability pixel detector modules. Associated Partners IBA, CNM and CIVIDEC host secondments and provide courses and coaching on bump bonding, sensors and electronics for beam instrumentation.

WP3



1. Optical data transmission (Wuppertal)

2. 3D integration of (bumped) chips (and sensors) -> modules

   - CMOS ICs (Bonn)
     - very deep submicron (65 nm),
     - vias first → new CMOS technologies

   - 3D post processing and testing (IZM, Bonn) – ICs and modules

Partners and Fellows

ESR 4	Optical data transmission for detector system Implementation of quality monitoring of the data transmission, development of production tests, integration of the card in test setups in labs, test beams and system tests, definition and realization of automatic tuning of the optical link.	WP 3	uWuppertal	36
ESR 5	New technical advances in vertical interconnection or very deep submicron technologies of CMOS circuits for integrated custom pixel modules, the FE-I4 chip and successors, development of new powering concepts based on multiplexing or serially servicing multiple modules	WP 3	uBonn	36
ESR 6	Development of high-density interconnects for future pixel detectors. Further development of interconnect structures to reduce the bump size and the pitch for further detector generations. Development of the 3D technologies: Integration of through silicon vias (TSVs) in the detector modules to minimize the detector volume and to allow an x-y sensor matrix without spacing.	WP 3	Fraunhofer	36

3 ESRs (3 years) at 3 institutions (Wuppertal/Bonn/IZM Berlin)

ESR4

ESR5

Tasks and deliverables

New optical data transmission: This project covers the implementation of quality monitoring of the data transmission, development of production tests and their implementations, integration of the card in test setups in labs, test beams and system tests, definition and realization of automatic tuning of the optical link. These tasks involve the ESR into developing firmware and design and operation of test environments for electronic equipment (uWuppertal, uBonn).

New technical advances in the vertical interconnection of CMOS circuits (vias first) and also by post-processed chip/sensor assemblies using through-silicon-vias (vias last) have opened the possibly for deeply integrated full custom pixel modules. Alternatives for high integration are very deep submicron technologies (65 nm). During 2011 and 2012, further investigations of a via-first 3D integrated process and 65 nm processes will be pursued, to lead to an IC with FE-I4 like functionality but analogue and digital parts in different tiers and a pixel granularity divided by 2 (uBonn).

Further development of interconnect structures to reduce the bump size and the pitch for further detector generations. Development of the 3D technologies: Integration of through silicon vias (TSVs) in the detector modules to minimize the detector volume and to allow an x-y sensor matrix without spacing. (Fraunhofer)

List of deliverables:

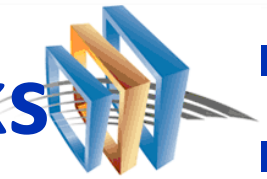
D-3.1 USB-Pix Setup for module tests commissioned, M12

D-3.2 Pixel Sensor and FE ASIC qualification modules, M18

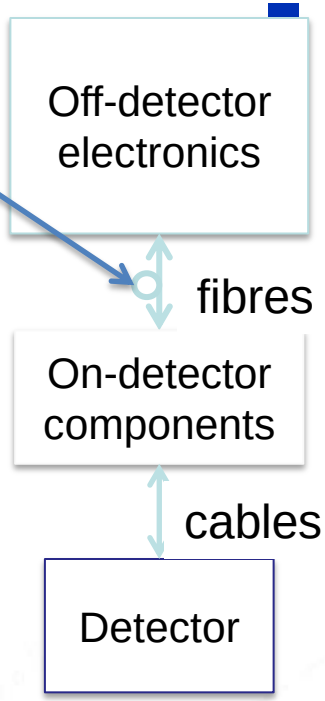
D-3.3 Full system test of module to DAQ, M36

ESR6

ESR4: R&D for Improved Data Links



- This research project focuses on the optical data transmission between detector systems and readout electronics.
- The ATLAS **IBL data link** is the **starting point**
  - learning about the functionality
  - system aspects (lab, test-beam, system test, detector commissioning) when connecting the chain together
  - learning about the detector requirements on the link
- Knowledge about electronics and optics will be gained, including modern FPGA techniques
- This will be the basis for driving the link components towards higher requirements for upcoming detector systems:
  - optical components (laser / PiN diodes) need to be more radiation hard, deliver higher bandwidth, use less power and space
  - electronics will change architecture and follow the increased requirements of the detector systems



Typ. data link structure

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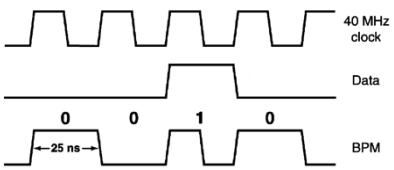
ESR4: Research Items

- Based on the gained experience with the existing links, **research focuses** will be:
  - **optical components and systems** – to improve their properties, bandwidth **(160 Mb/s → 5 Gb/s)**, radiation tolerance, cooling and packaging, multichannel vs. single channel links …
  - **study transmission protocols** to be used in data transmissions – reliability and bandwidth
  - development of **new readout electronics in modern architectures** (i.e. PC standards)
  - realize **link prototypes** (electronics and optics) to test and prove the improvements
- The candidate is expected to have a Master degree in the field of physics or electronics engineering
- Skills in working with electronics and doing systematical studies are useful
- The candidate will gain experience about readout systems, optical components, and hardware programming
- The candidate will be based in **Wuppertal,** but the work will be performed in collaboration with German and international groups and institutes having close contact to industry, too.

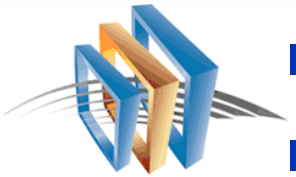
Optical components



Data encoding

FPGA evaluation board

ESR5: IC dev. and 3D integration



FE-I4 Chip as starting point and working horse for

- development of a testing environment for chips and modules (USBpix)
- module building and integration
  - building of qualification modules
  - building of a serially powered full stave
- building of qualification modules
- full system (IBL) test to DAQ
- 3D integration (post processing)
  - through silicon vias and post processing (with IZM)
  - merging of FE-I4 with monolithic pixel sensors
- further chip development towards
  - very deep submicon technologies (65 nm)
  - 3D CMOS integration (Tezzaron/Chartered)

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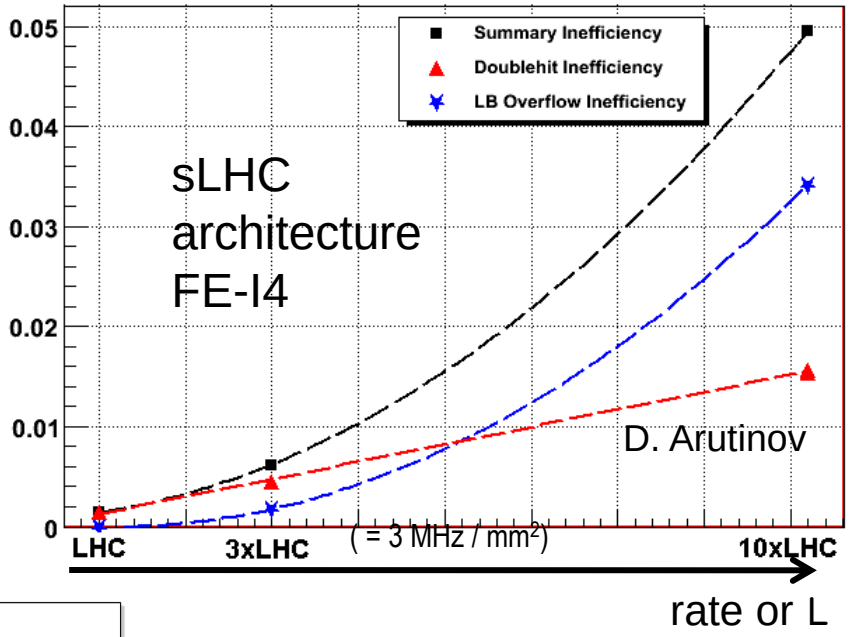
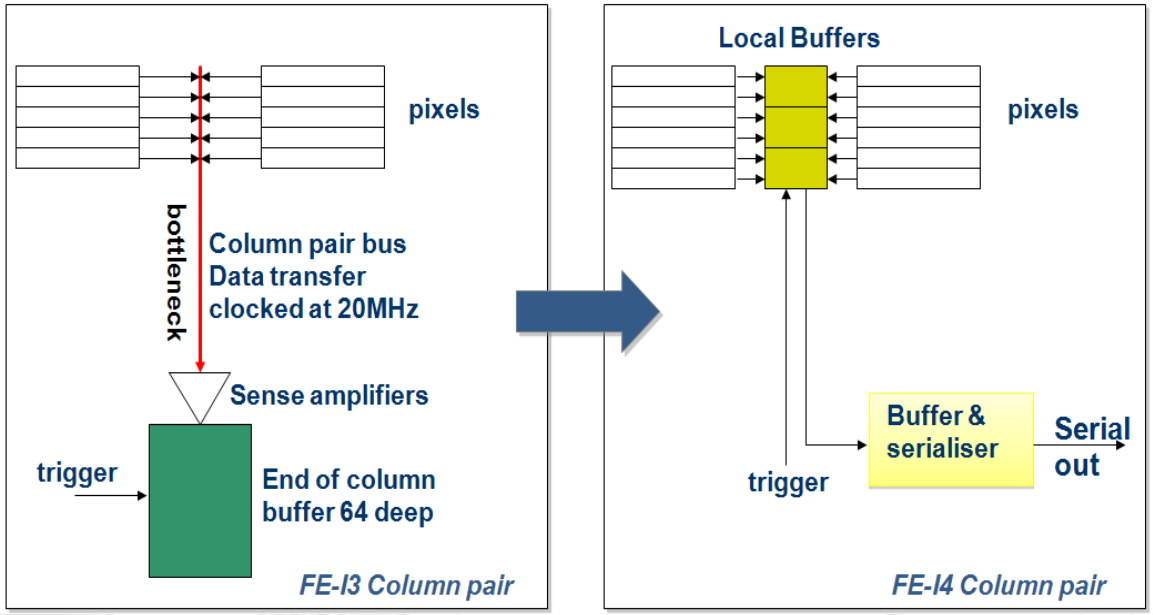
sLHC data rates

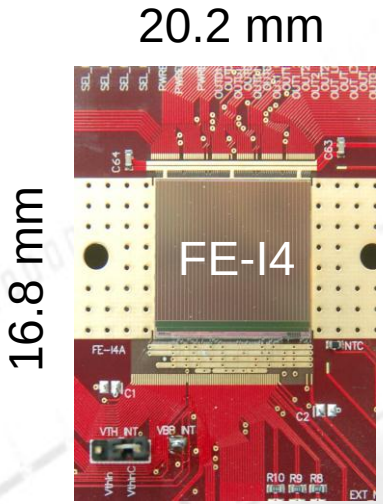
Hit inefficiency rises steeply with the hit rate

Bottleneck: congestion in double column readout

⇒more local in-pixel storage (130 nm !)
>99% of hits are not triggered
⇒ don't move them -> not blocking



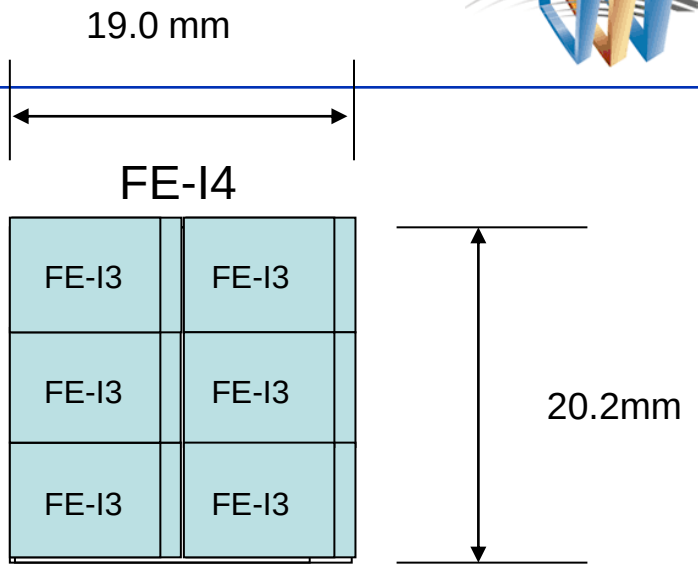




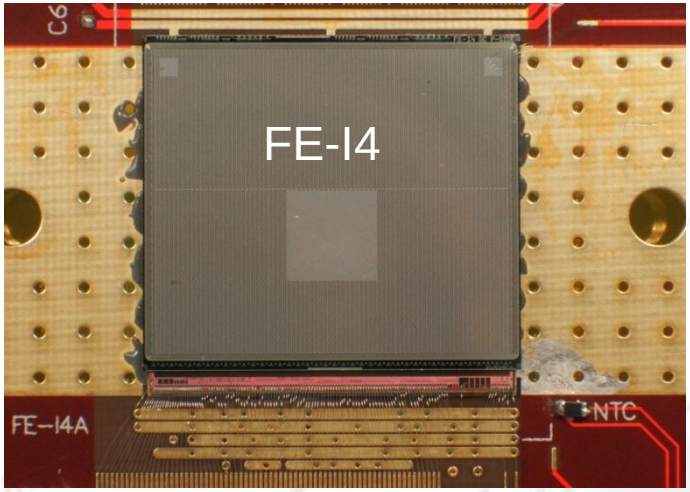
Bonn
CPPM
Genova
LBNL
NIKHEF

FE-I4

- successor of current (50 x 400 µm²) FE-I3 for new IBL
  - smaller pixels (50 x 250 µm²)
  - lower noise and threshold operation
  - higher data rate compatibility

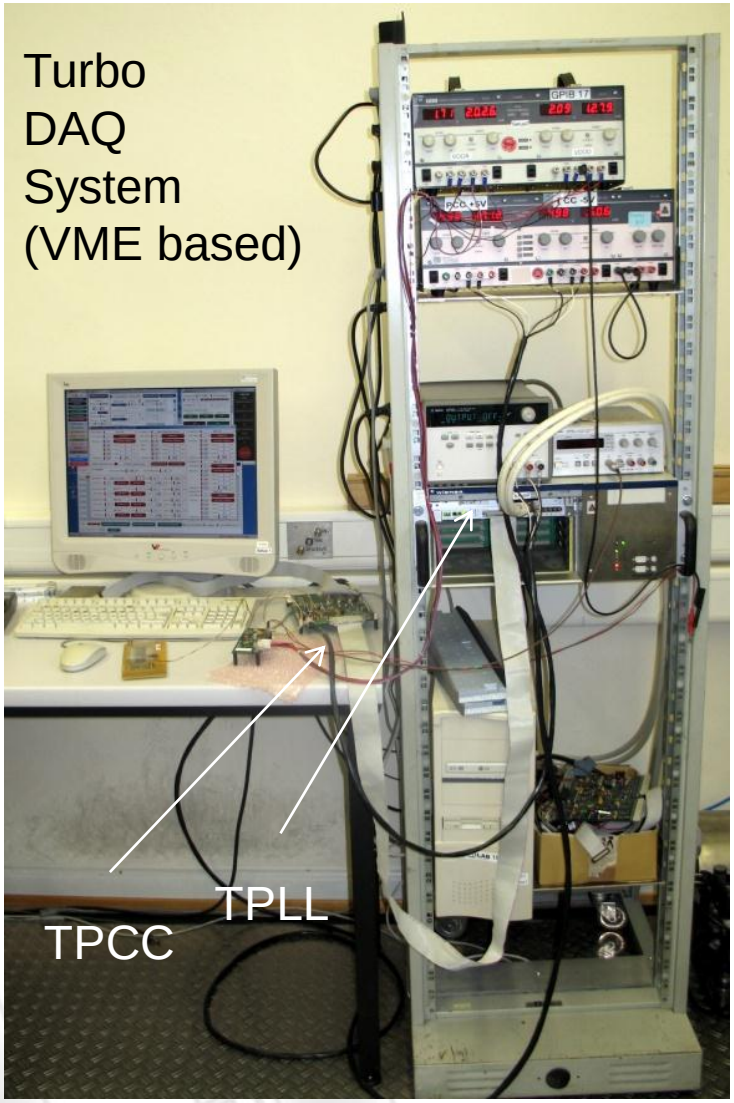


- column drain architecture with local hit storage
- IBM 130 nm
- array size: 80 col. x 336 rows 26880 pixels, 7x10⁷ transistors
- average hit rate @ 1% inefficiency = 400 MHz/cm²
- max. trigger rate: 200 kHz



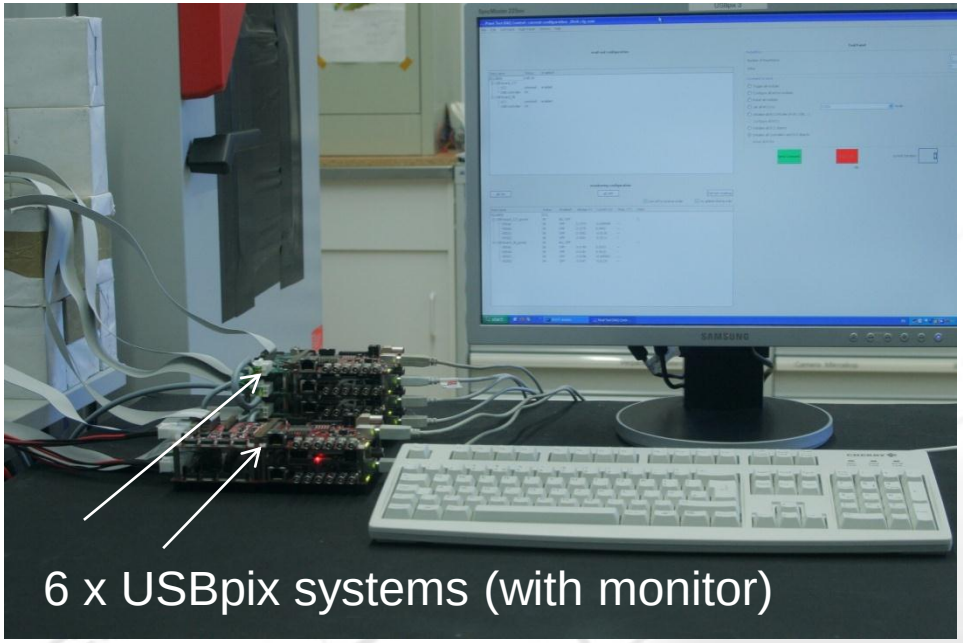
- **FE-I4A works, FE-I4B back from foundry: Nov. 2011, tested ~ok**

TESTS:TDAQ → USBpix

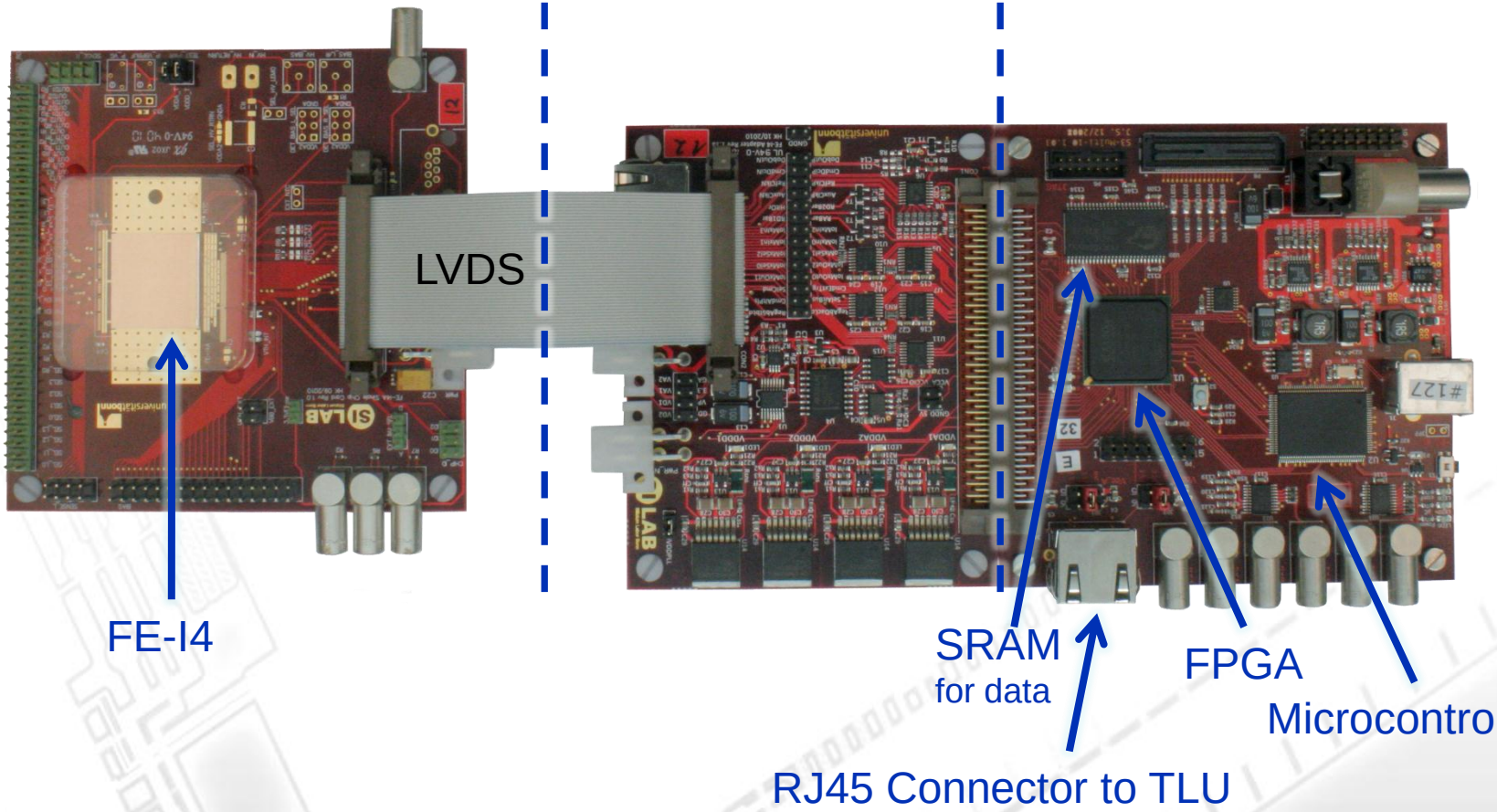


new readout and test system for

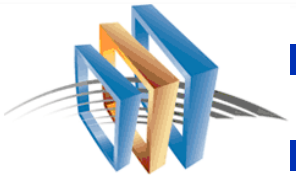
- FE-I4 ICs
- FE-I4 wafers
- FE-I4 module assemblies
- testbeam operation



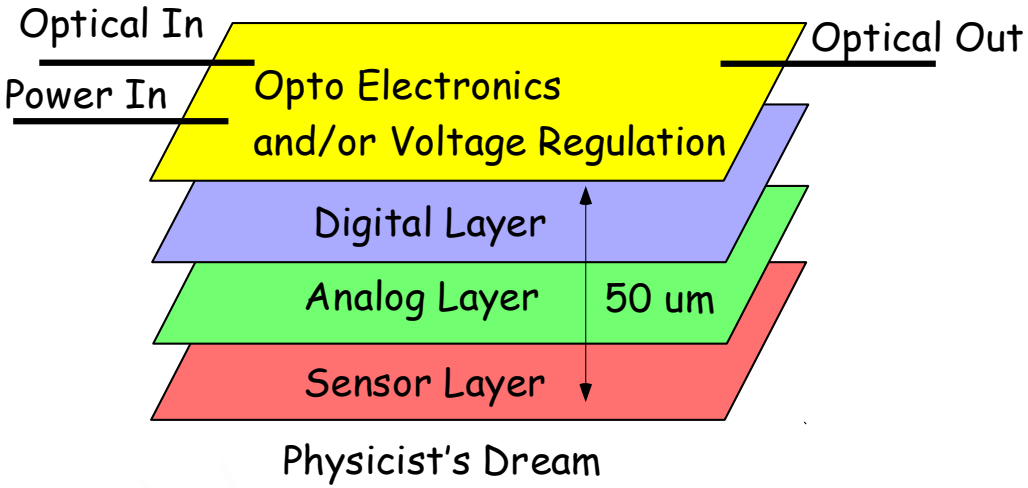
USBpix with FE-I4 (details)

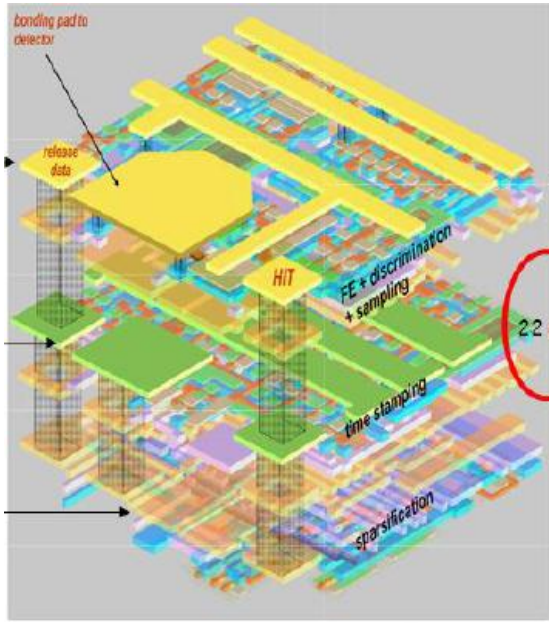


3D integration … a hot topic



"vias first" … various CMOS layers





3D integration promises

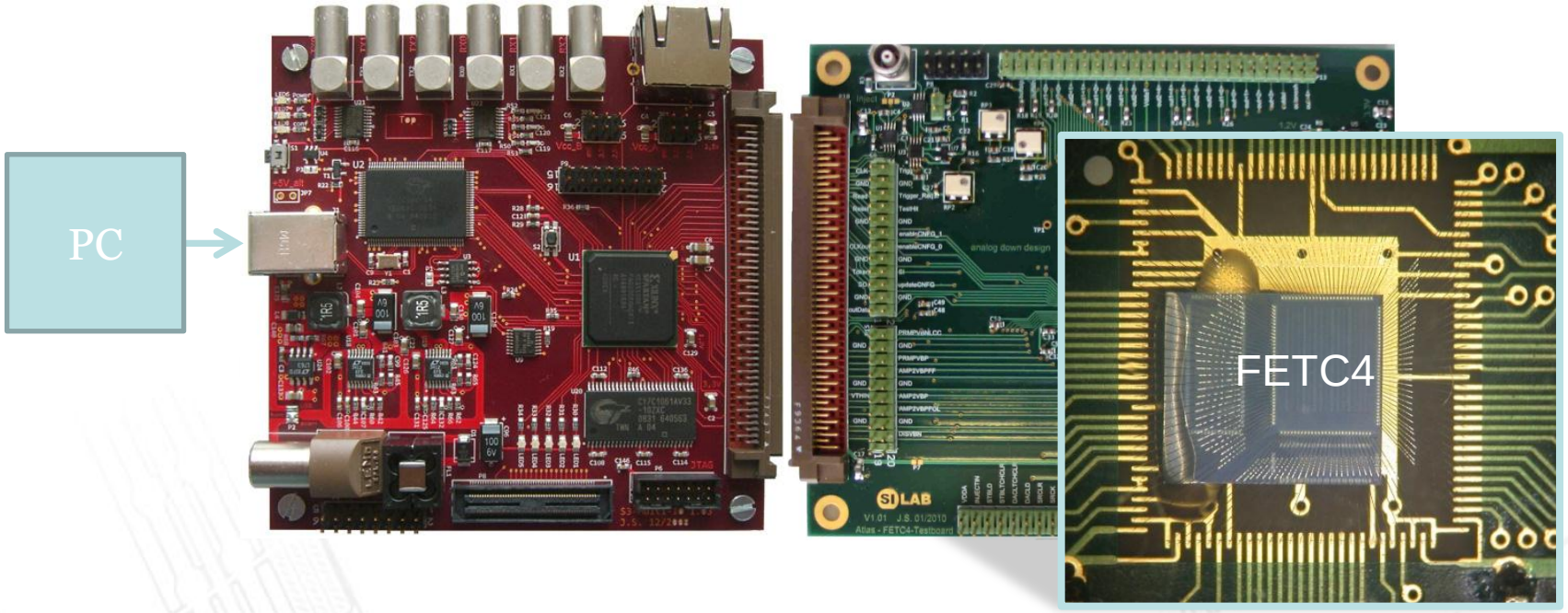
- higher granularity
- lower power
- large active over total area ratio
- low mass
- dedicated technology for each functional layer

prototypes with

- OKI
- MIT LL
- Tezzaron/ Chartered

First ATLAS 3D CMOS structures ...

3D CMOS chip FETC4 bonded and tested.



- still some severe problems
  - mostly alignment issues
- analog tier thinned down to 12µm and operated stand alone shows same noise behavior as un-thinned 2D

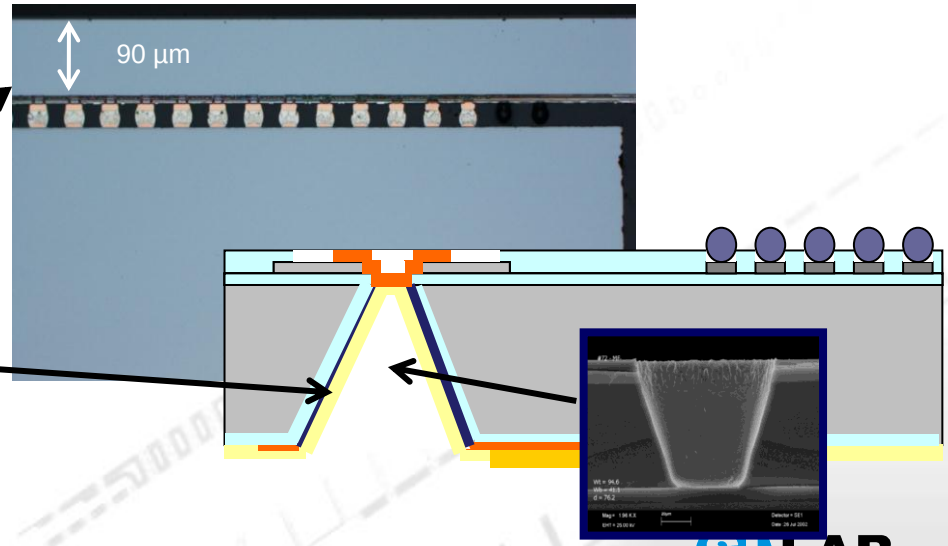
vias last … post processing

exploit: 3D integration for hybrid pixels, through silicon vias, wafer to wafer connection

Through Silicon Vias (TSVs)
(FhG IZM Berlin / UBonn)

gain ~ 1% x/X_0 in ATLAS with

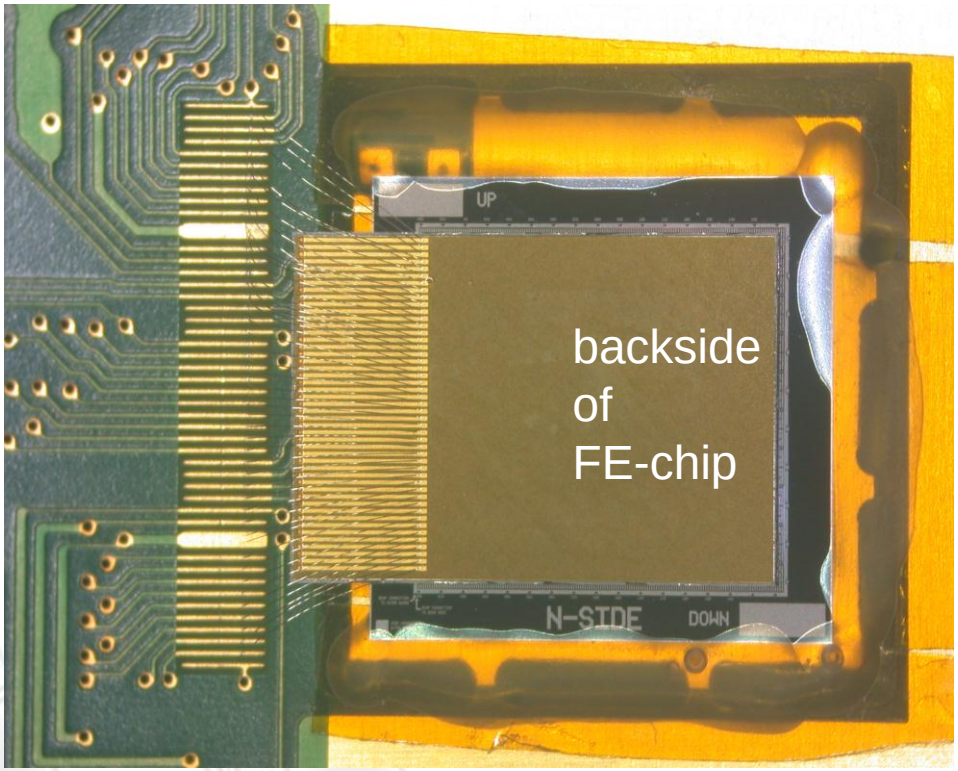
- 90 µm bumped FE-I4 chip
- thin Al flex
- serial powering
- TSV and backside metal routing



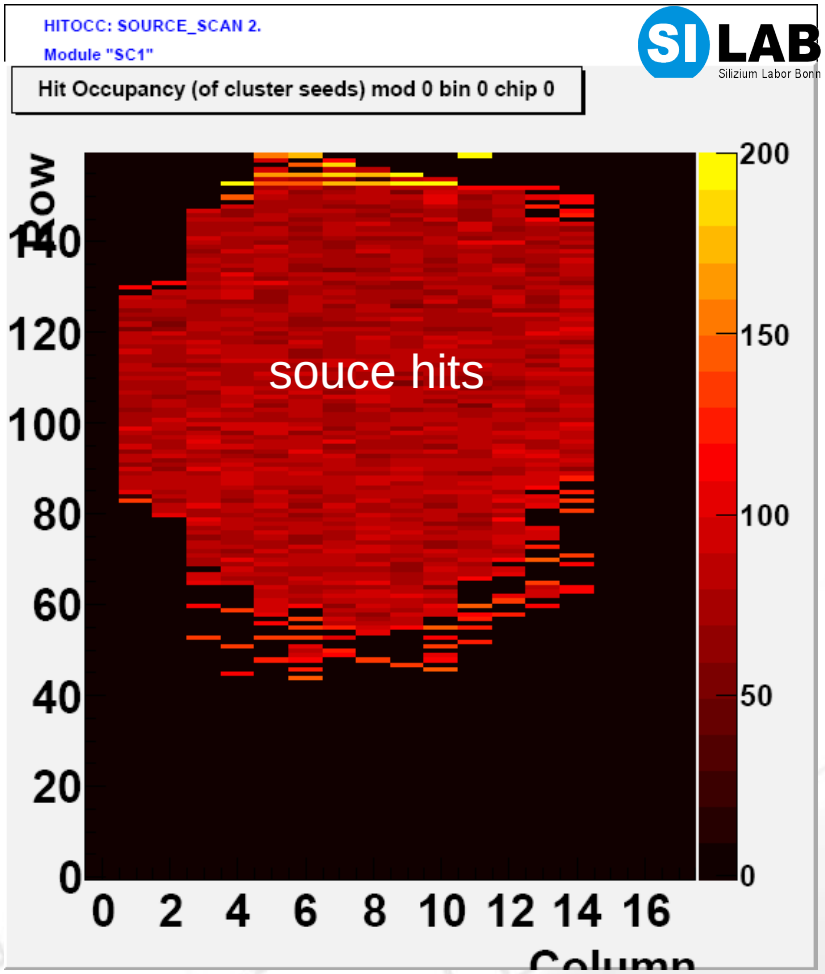
aggressive reduction in material

Proof of principle demonstration

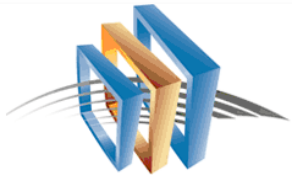
ATLAS FE-I3 chip-sensor module operated
through TSV and backside re-routing



- **Source scan with Am-241 source**



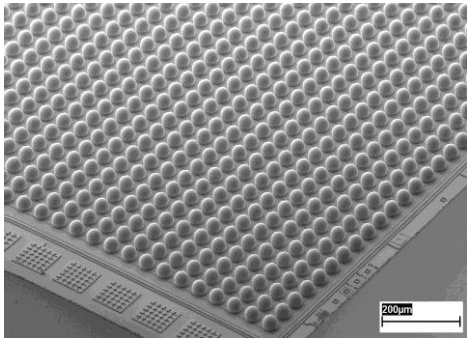
ESR5: tasks and opportunities



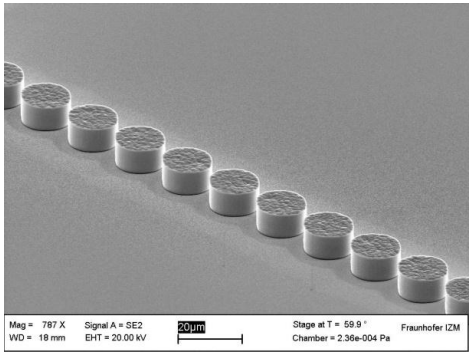
- design, prototyping and testing of ASIC mixed circuit analog/digital chips, and/or the design and assembly of highly integrated modules and the implementation of quality-assurance protocols for the production of high-reliability pixel detector modules.

- new technical advances in vertical interconnection or in very deep submicron technologies of CMOS circuits for integrated custom pixel modules, the FE-I4 chip of the ATLAS pixel detector at CERN and its successors, or the development of new powering concepts based on multiplexing or serially servicing multiple modules are possible research directions.

ESR6: Advanced interconnects



25µm bumps / 55µm pitch



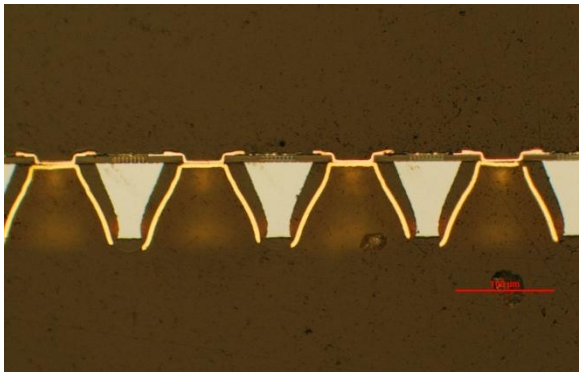
10µm pillars / 20µm pitch

Further development of interconnect structures to reduce the bump size and the pitch for further detector generations

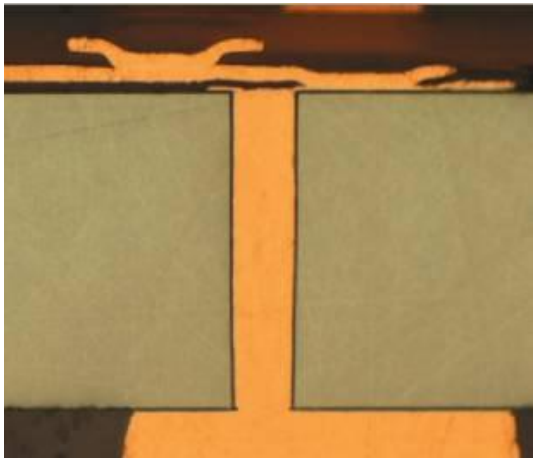
Tasks:

- design of **small size interconnection structures**
- Investigation of material requirements
- **Process development** and prototyping
- Development of modified **assembly technologies** for small size interconnection structures
- Reliability investigation

ESR6: Through Silicon Vias



Tapered TSVs in ATLAS FE-I2 ROC



Straight sidewall TSVs for interposer

Development of the 3D technologies: Integration of through silicon vias (TSVs) in the detector modules

Tasks:

- design of TSV structures and implementation into ASIC design
- Development of readout-chip wafer adapted TSV-process chain
- TSV Processing of readout-chip wafer
- Process development of modified assembly technologies for thinned TSV-ROC chips
- Manufacturing of prototypes
- Reliability investigation

ESR6: Researcher Fellowship

Fellowship Description

The main objective of this research fellowship is design of interconnection and TSV structures, process development on wafer level, manufacturing of prototypes and reliability investigation of assembled modules. The investigation of requirements for small size interconnection structures as well as the development of adapted bonding technologies are possible fields of study. Another task will be the integration of TSVs process into module fabrication to form 3D integrated pixel detector modules.

Academic Requirements

Eligible applicants for this Fellowship (equivalent to a PhD position) must be in possession of a Master degree in the field of microsystem technology, electronics engineering or comparable fields.

Conclusions

- WP3 (electronics) already well underway

- ESR4, ESR5, ESR6

  will find plenty of opportunity to contribute to this research