Serial Powering

System level … challenges and caveats

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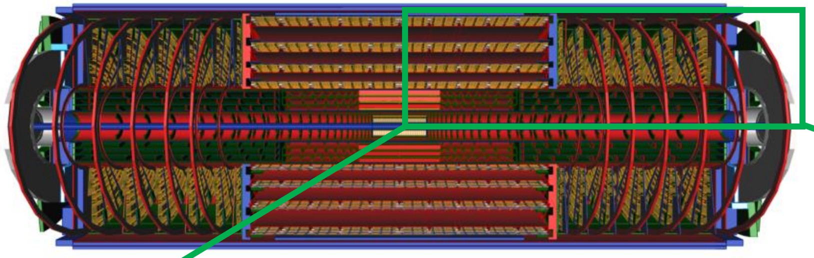
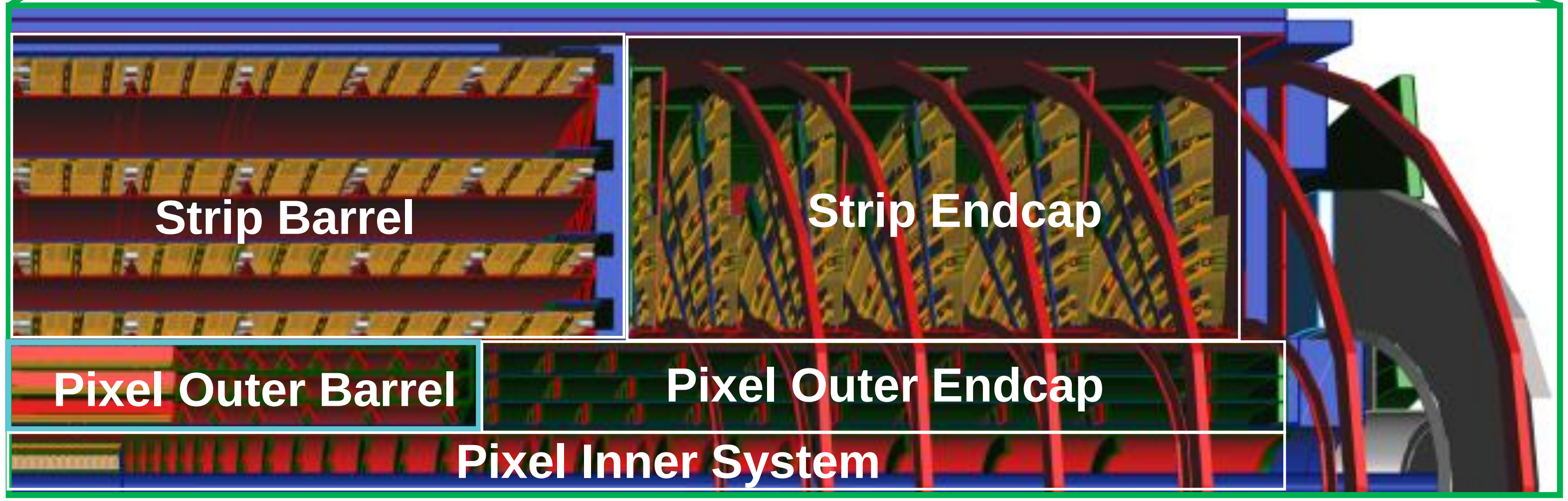
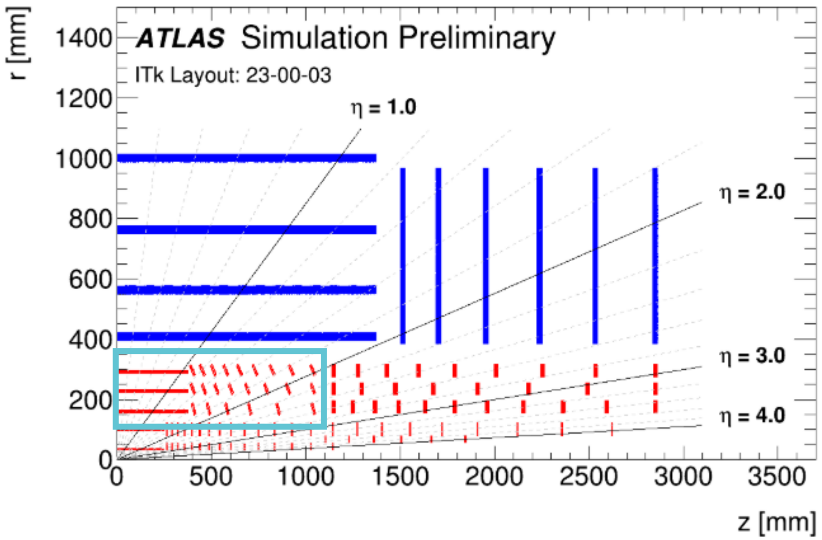
Background - ATLAS ITk and the Outer Barrel sub-system 1/2



ITk layout for HL-LHC



3D rendering – One quadrant



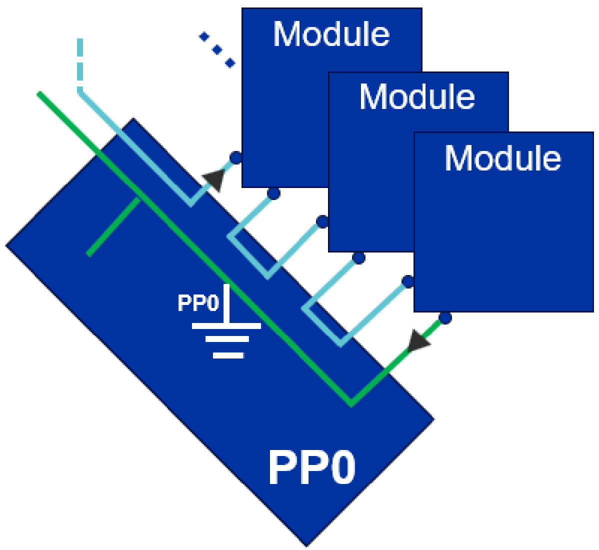
ITk Schematic layout – One quadrant, only active components shown

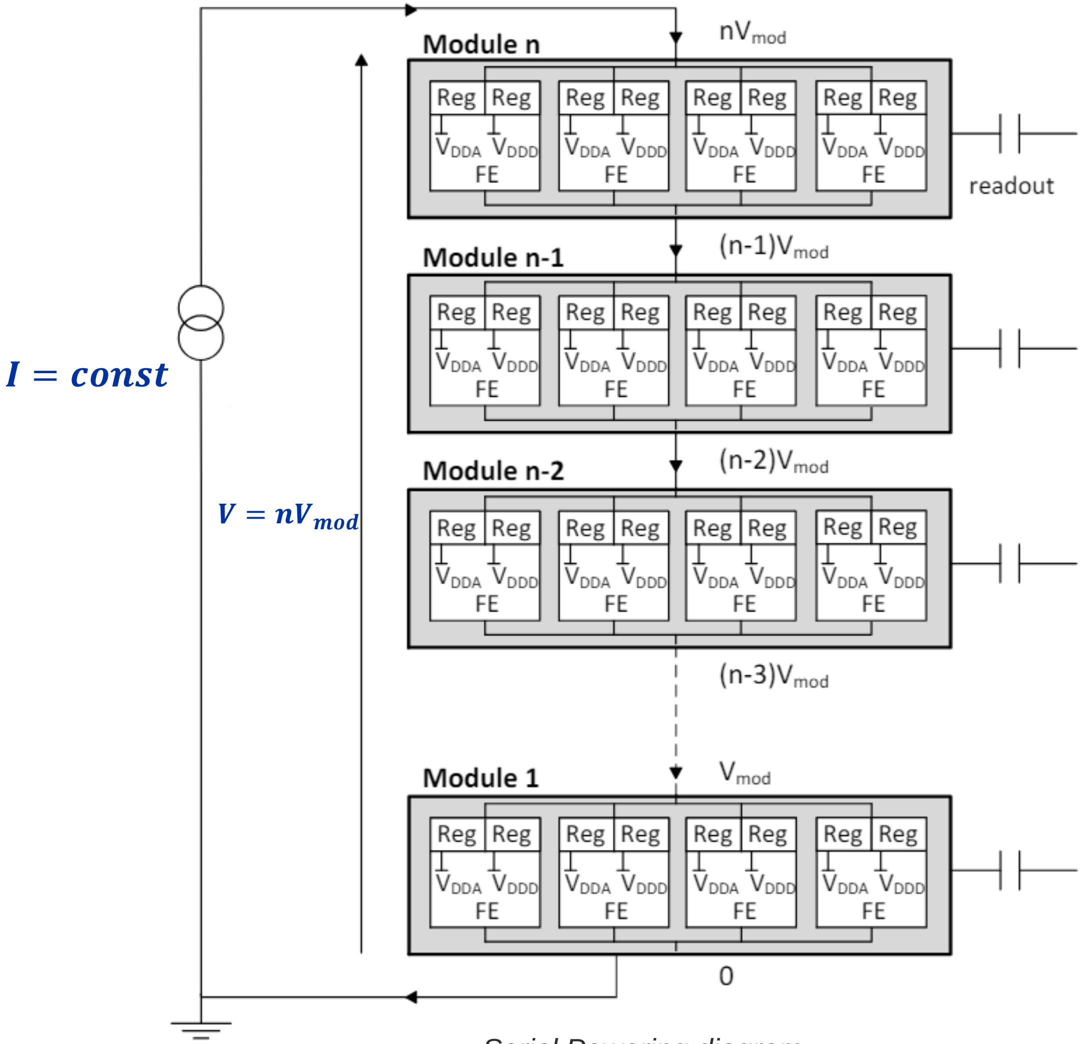
Pixel sensors in red, strip sensors in blue. The OB in light blue.

Background - ATLAS ITk and the Outer Barrel sub-system 2/2

- Up to n=14 modules in series
- 4 FE-chips per module
- 2 Shunt-LDOs per FE-chip

- 6A nominal current (I), 1.6V per module (V_{mod})





Serial Powering diagram

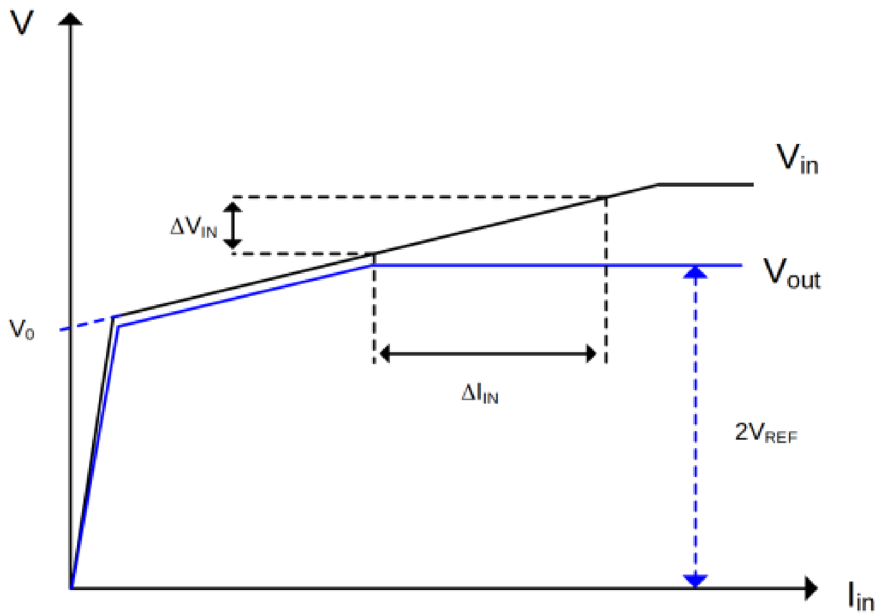
Serial Powering – Introduction

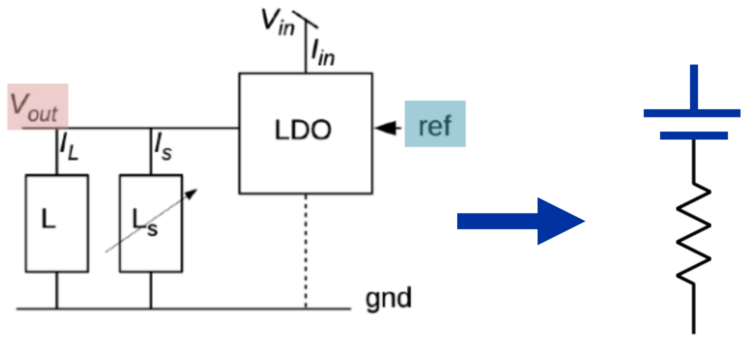
$$I_{IN} = I_L + I_S = \frac{V_{IN} - V_O}{R_{eff}} = const^*$$

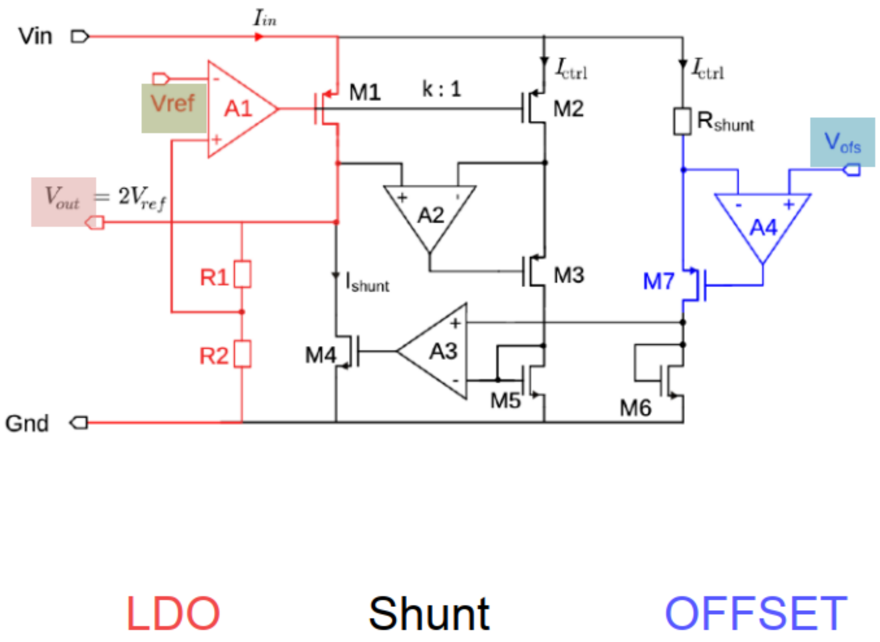
VIN: Input voltage by power supply

VOFFSET: Offset reference, programmable, constant, defines current draw

Reff: constant, programmable



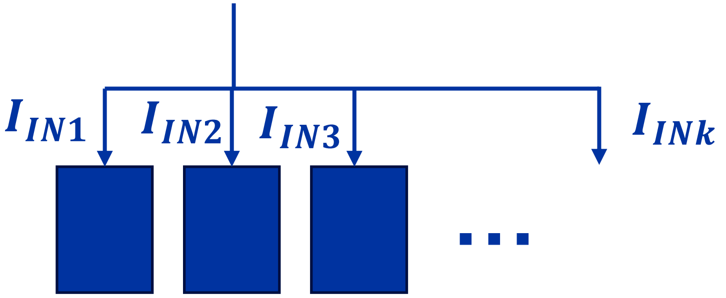




Serial Powering – SLDOs in parallel

Parallel SLDO design trades efficiency (low Reff) vs current sharing robustness:

$$\frac{dI_{IN}}{dV_O} = -1/R_{eff}$$



$$I_{INk} = \frac{V_{IN-}V_O}{R_{eff}} = const^*$$

Managing current sharing:

- **Trim main current reference for Vofs**
- **Resistively tie Vofs to force a common one*.**

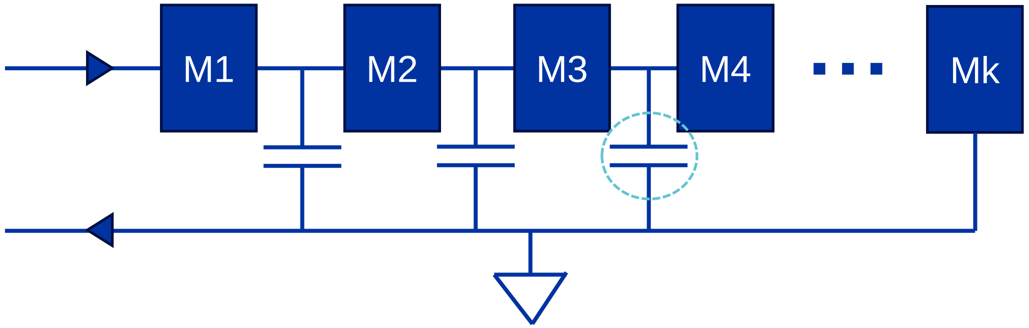
*ATLAS ITk config

Serial Powering – System specific details

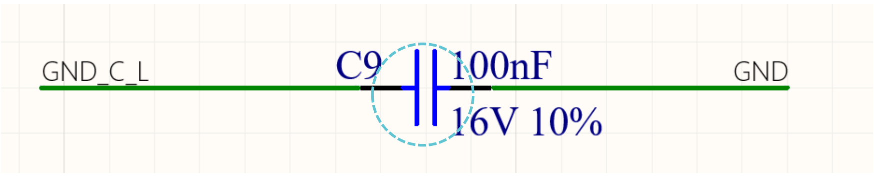
- **Undershunt protection (disabled in ITk Pixel)**
- **Overvoltage protection (enabled in ITk Pixel)**
- **How much Shunt current is enough?**
- **..**
- **..**

System level understanding – ESSENTIAL for all

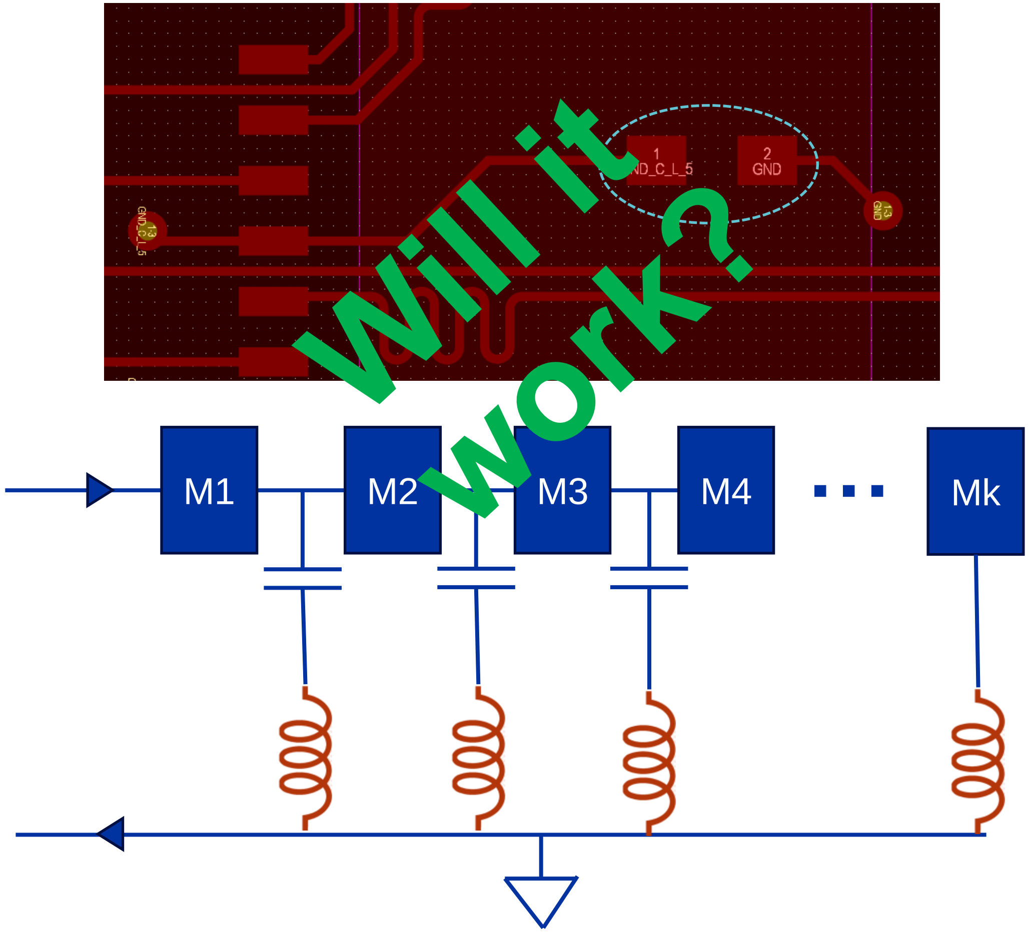
Shunt LDO simulations:



Module Schematic:

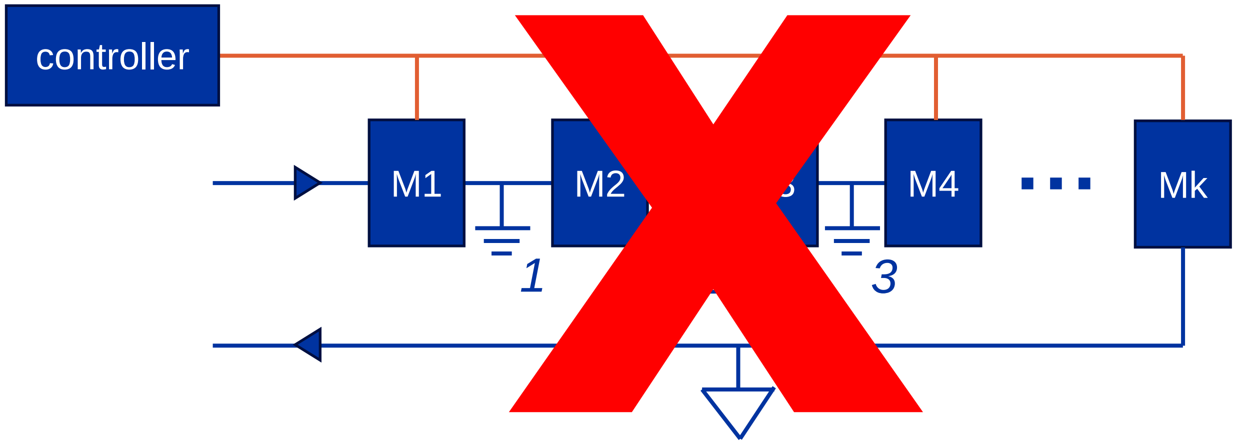


Misunderstandings can lead to “Ugly” reality:

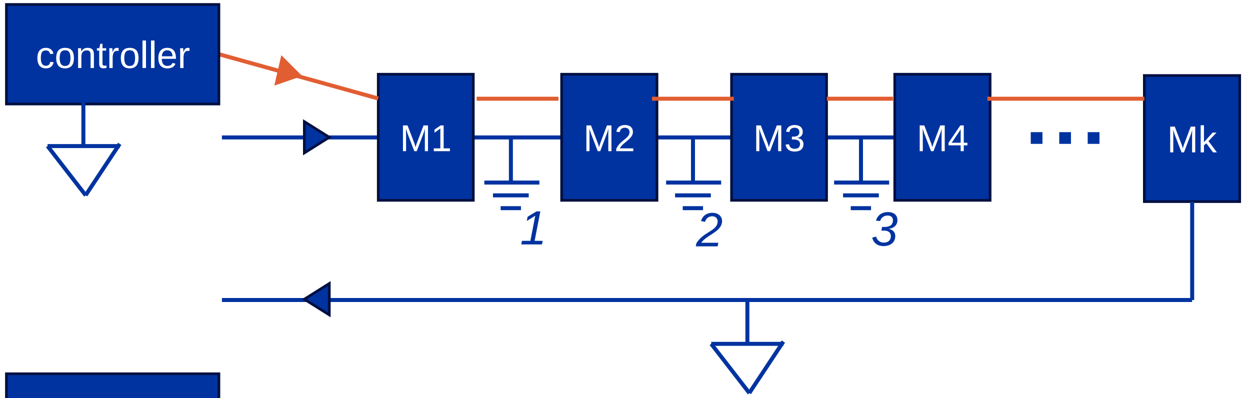


Simple Control Signals?

How to send control signals (reset, power mode change etc.)

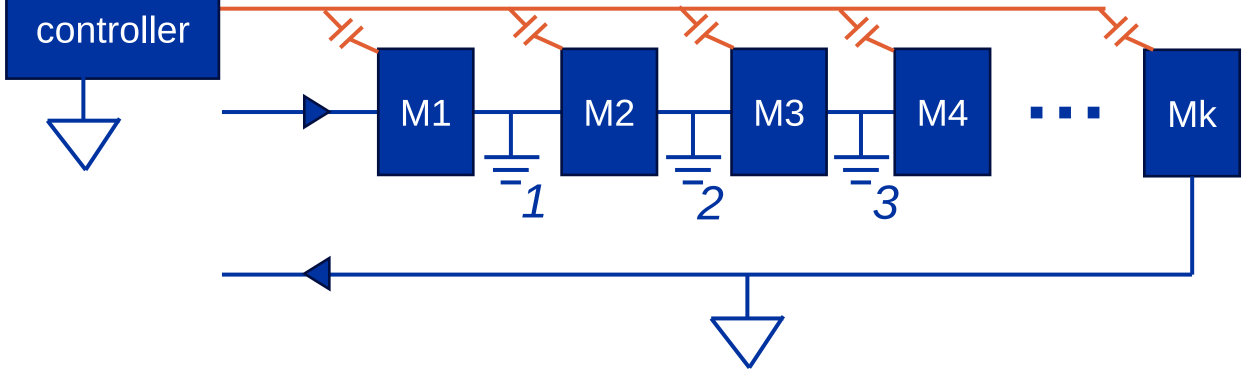


Send a current as a control signal



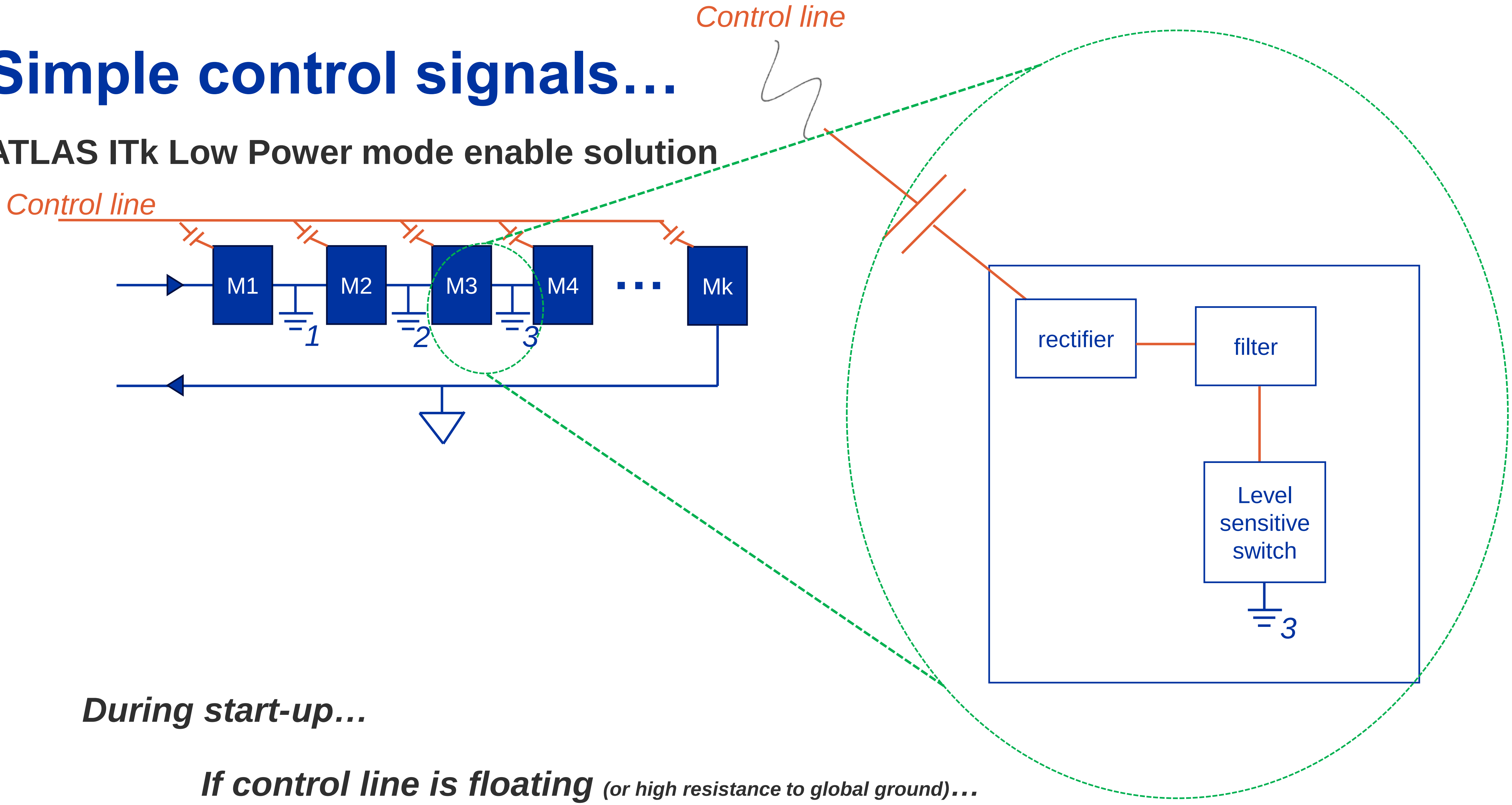
What can work?

AC couple and send a wave



Simple control signals…

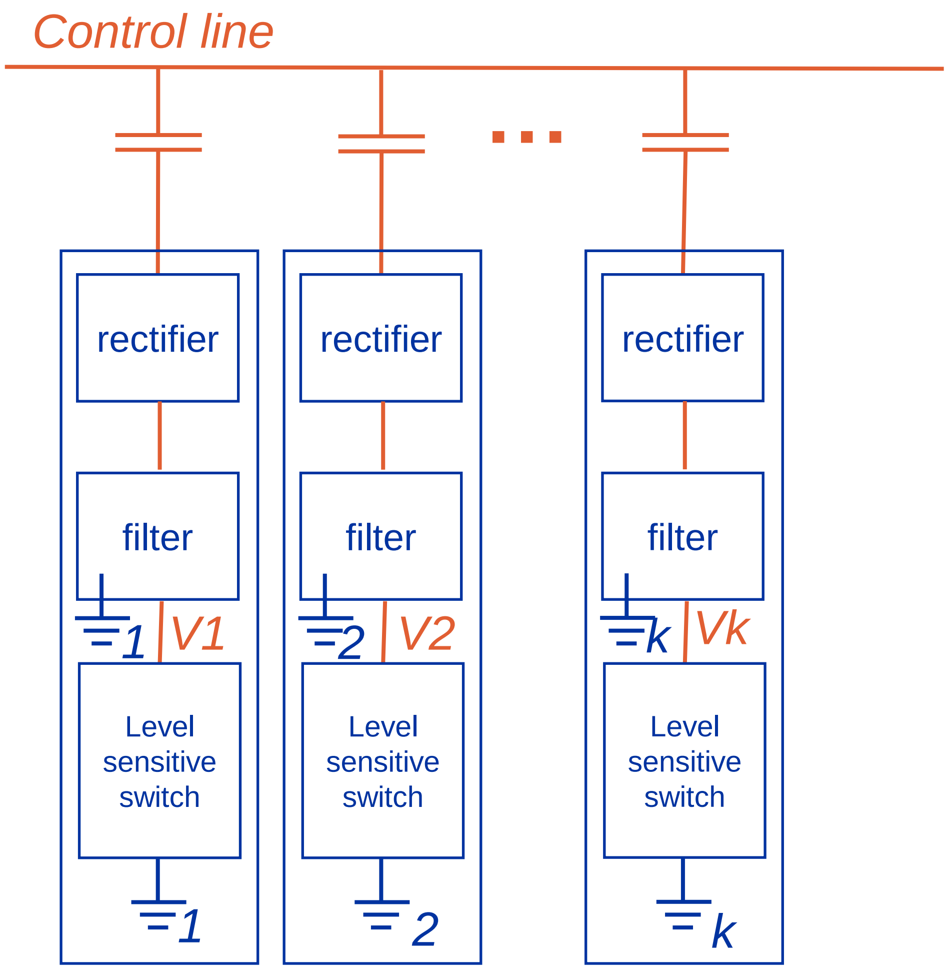
ATLAS ITk Low Power mode enable solution

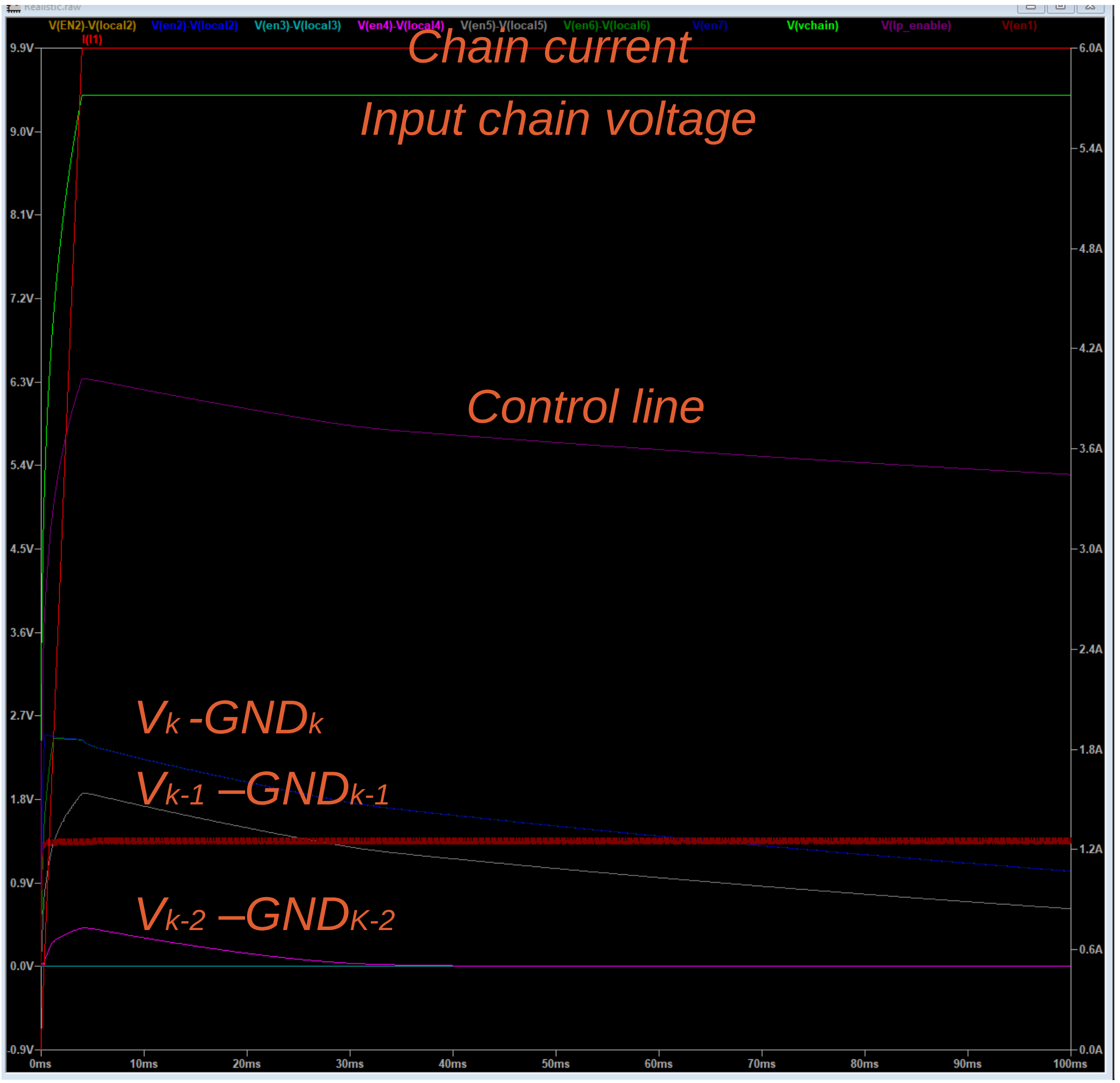


During start-up…

***If control line is floating** (or high resistance to global ground)…*

Simple control signals…





Last modules in the chain see a logic “high” during startup – headache/catastrophe

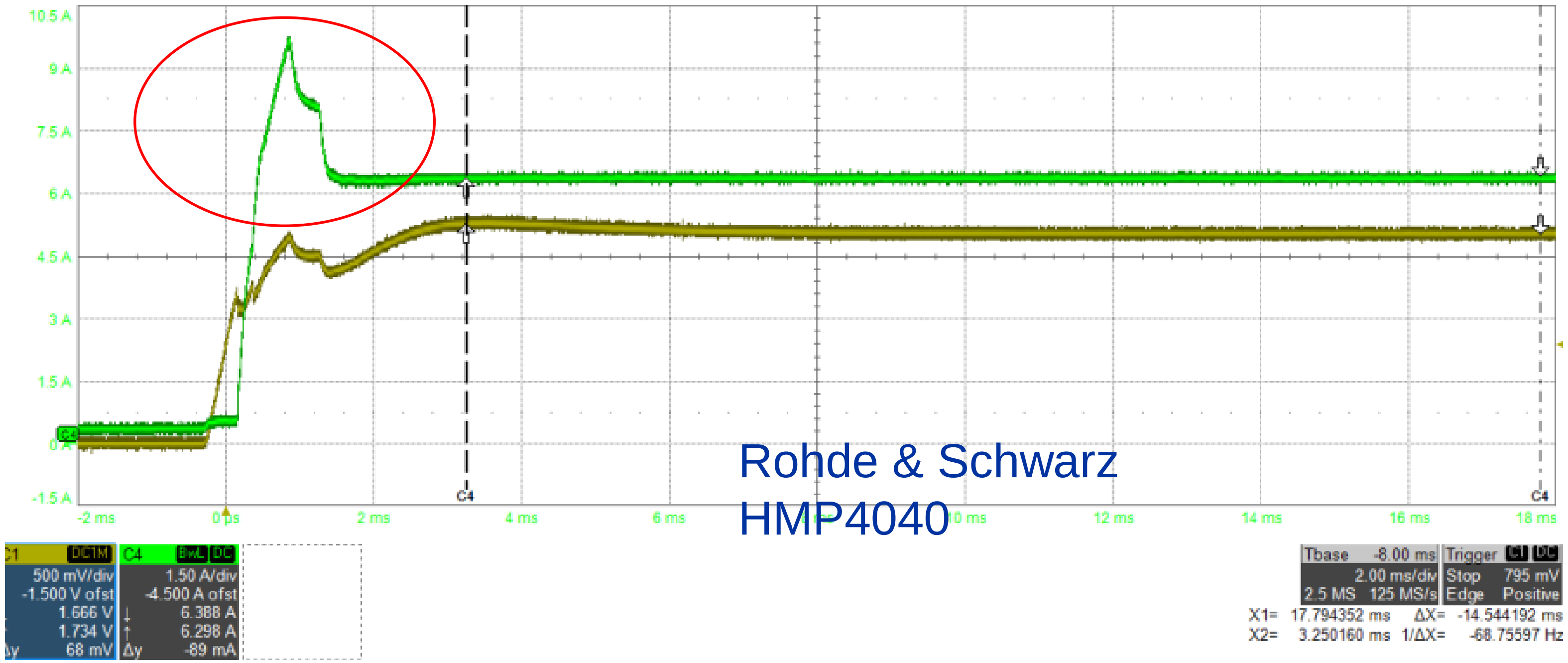
→

Fix requires low resistance to ground on control line so, also high driving capability of control source

Power Supplies 1/2

Proper Current supplies are a <u>must</u>

- Current stability
- Transient response
- Predictability during faults



Rohde & Schwarz HMP4040

- **ATLAS vs future LHCb MightyTrk**
- **What to use during testing?**

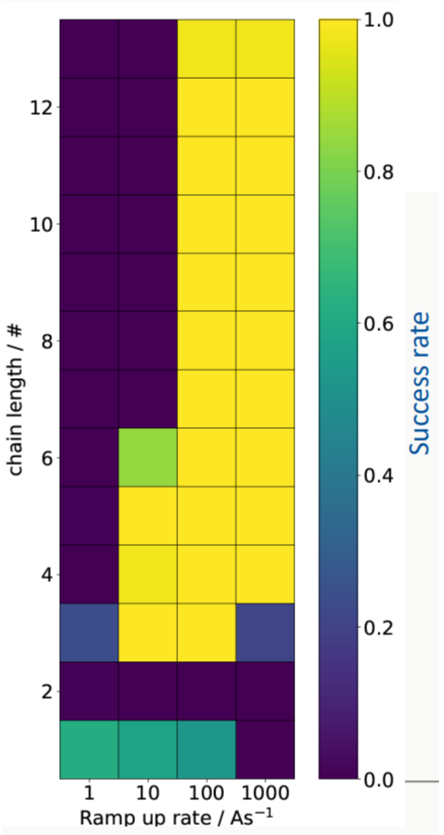
Power Supplies 2/2

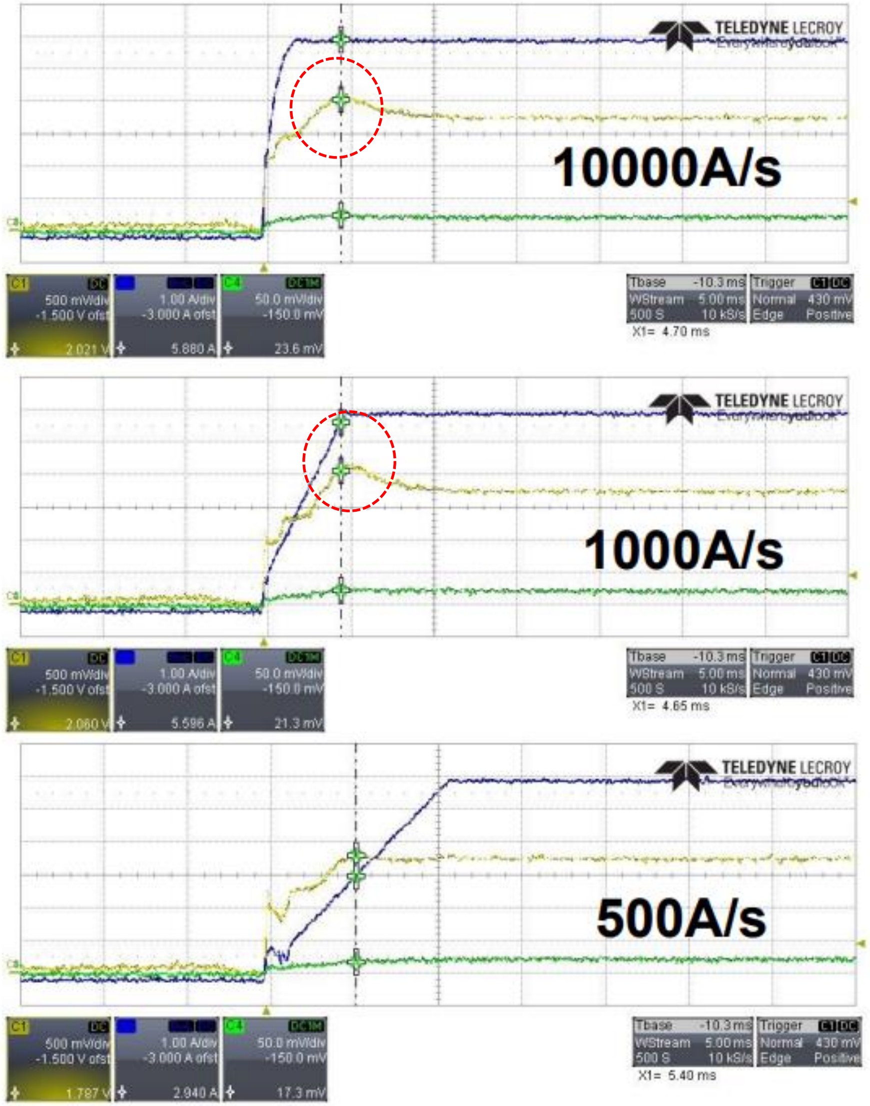
1. ***Production RD53 SLDO –when P.S. had uA of leakage in off state*** → ***Startup issues***

2. ***Ramp-up rate***

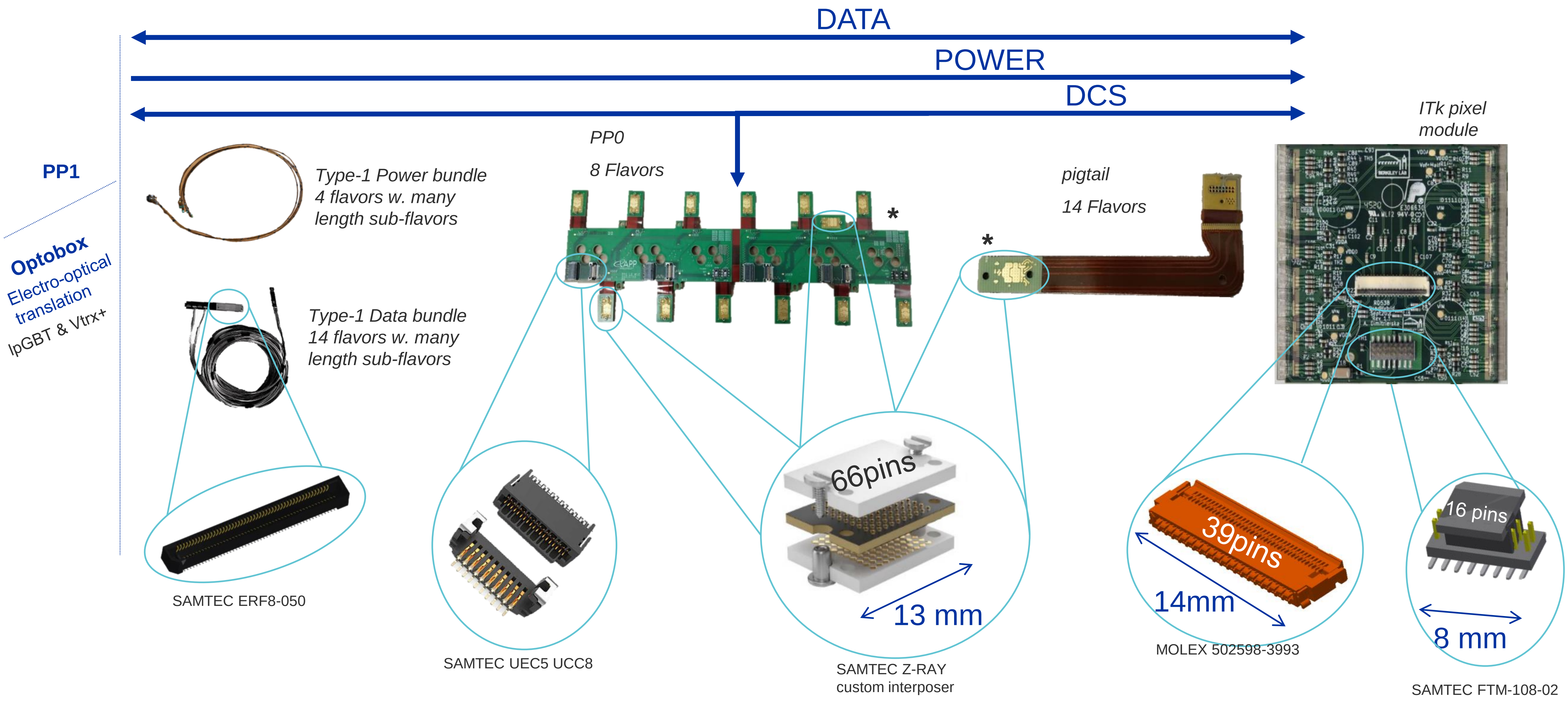
- *Before issues with slow ramps, now issues with fast ramp*
- *Current advice: need configurable ramps for testing and detector operation*

3. Conducted emissions testing?





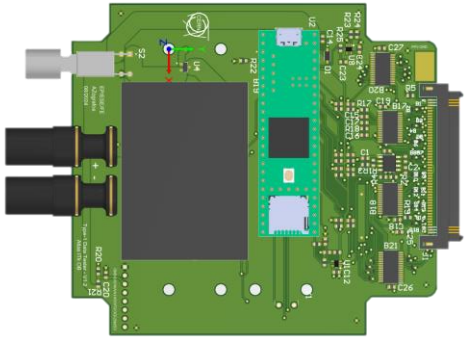
Connectivity testing complications – ATLAS ITk example

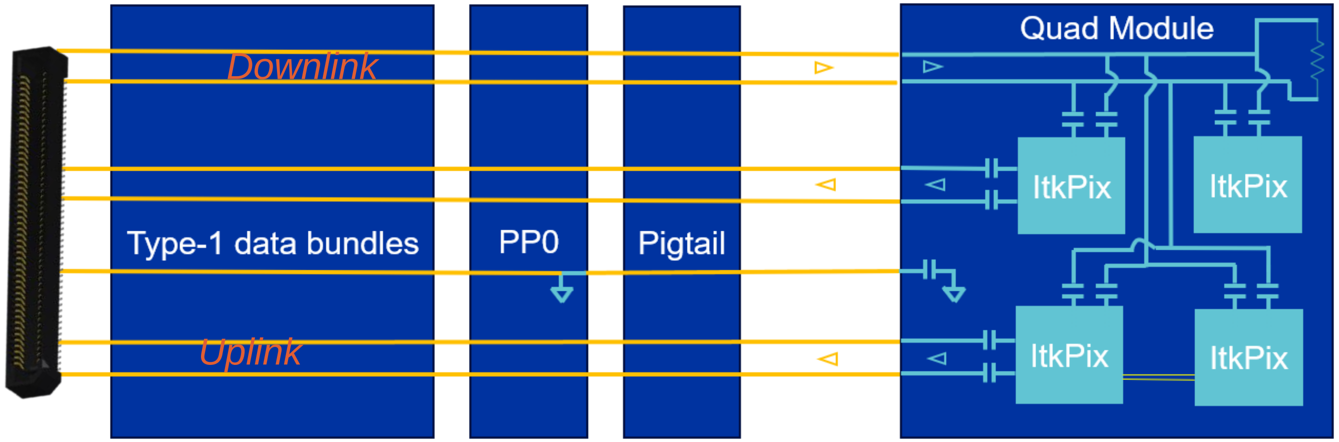


Connectivity testing complications – ATLAS ITk example

Lines AC coupled → Need to check capacitance instead of resistance and associate it with a healthy line
→ Distinguish services vs services + module

*ATLAS ITk developed specialized tool to perform these tests easily**



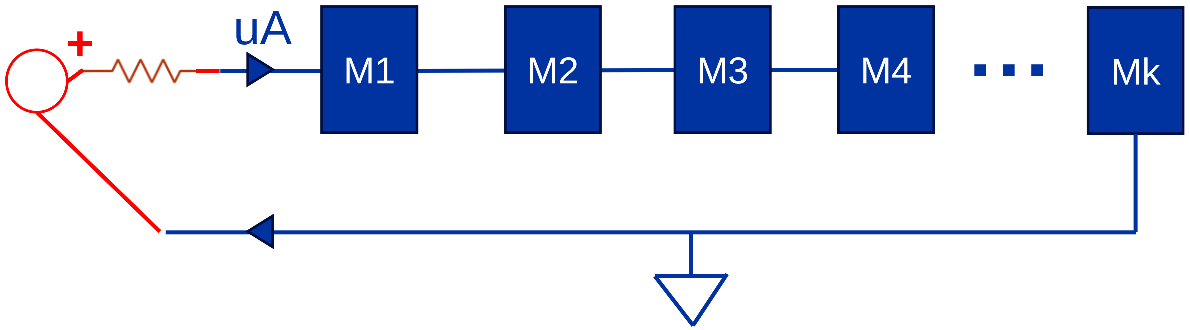


*https://iopscience.iop.org/article/10.1088/1748-0221/20/01/C01012/pdf

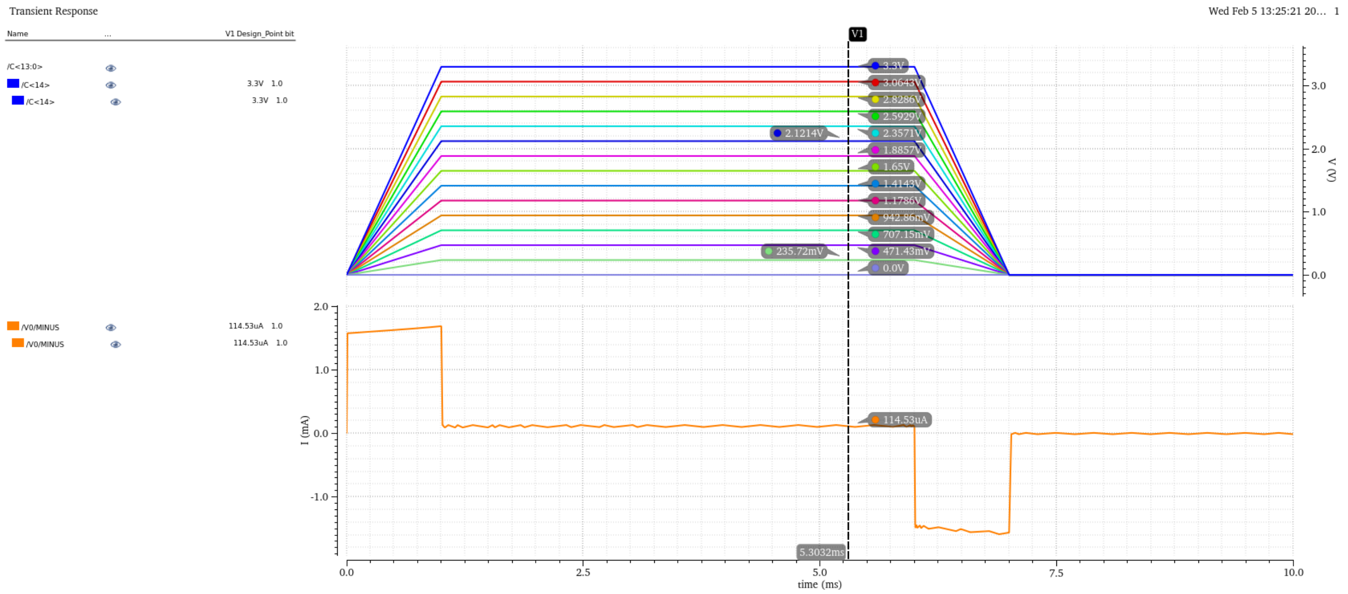
Connectivity testing complications – SLDO is.. delicate?

How to check serial powering chain is connected correctly?

→ Let's pass a small current to measure the resistance of the chain

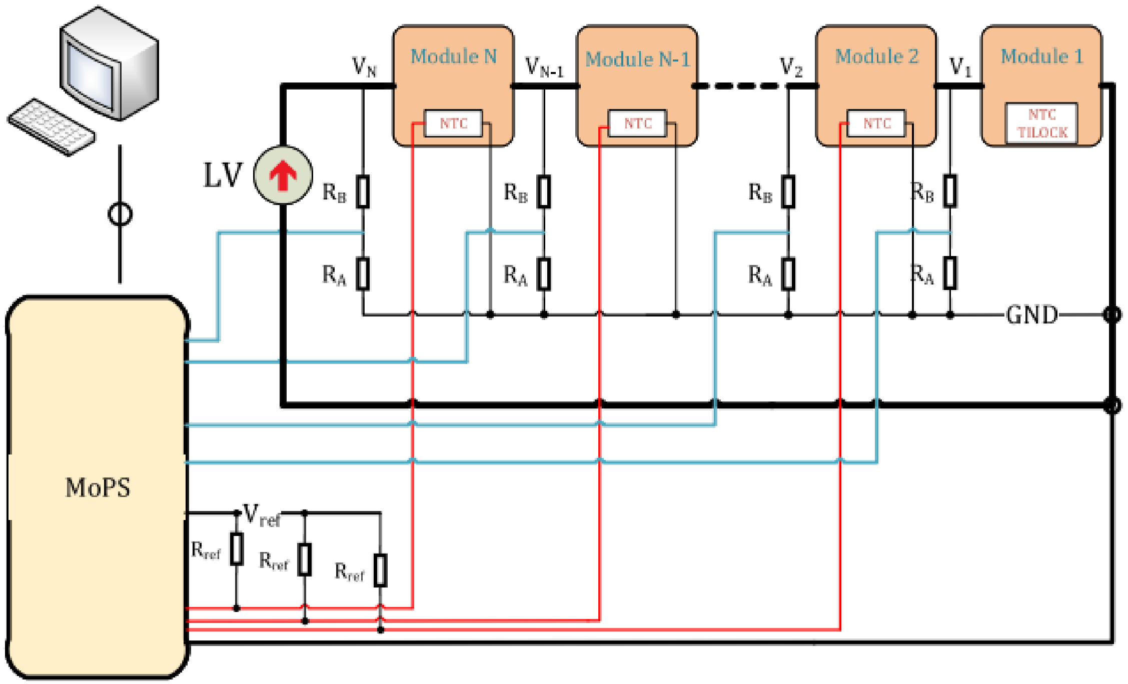


SLDO designer was not comfortable with running the system in this manner
→ long discussions and simulations



Monitoring

Local monitoring is required to observe SP chain operation.
→ *Monitoring from the Power Supply is, probably, not sufficient.*



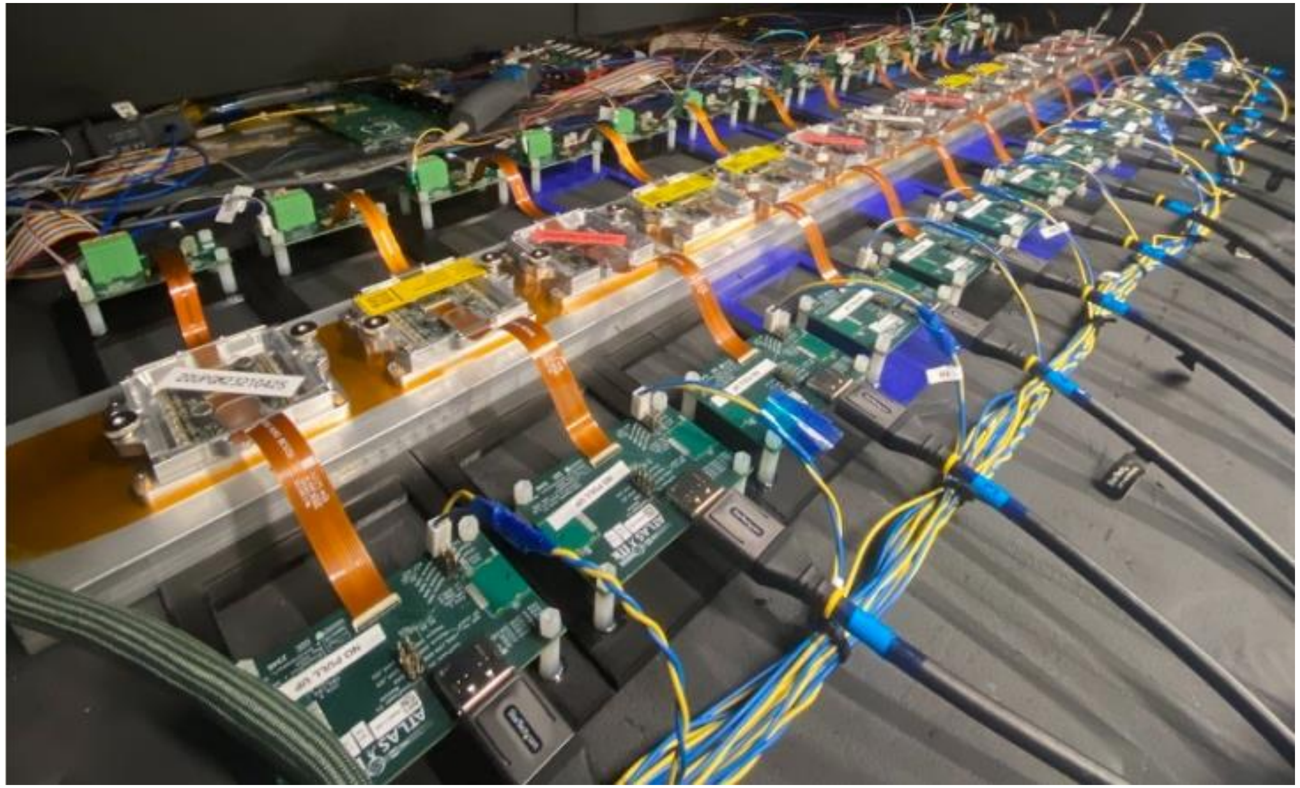
https://iopscience.iop.org/article/10.1088/1742-6596/2374/1/012094/pdf

Testing complications

- Full System tests require A LOT of hardware in working condition → Difficult to achieve early.

- Hardware required: PCBs to be able to complete chains of different sizes, special power supplies

Case of ITk: System test reveals issue → too late for Services to adapt, we live with suboptimal case (potentially floating control line)



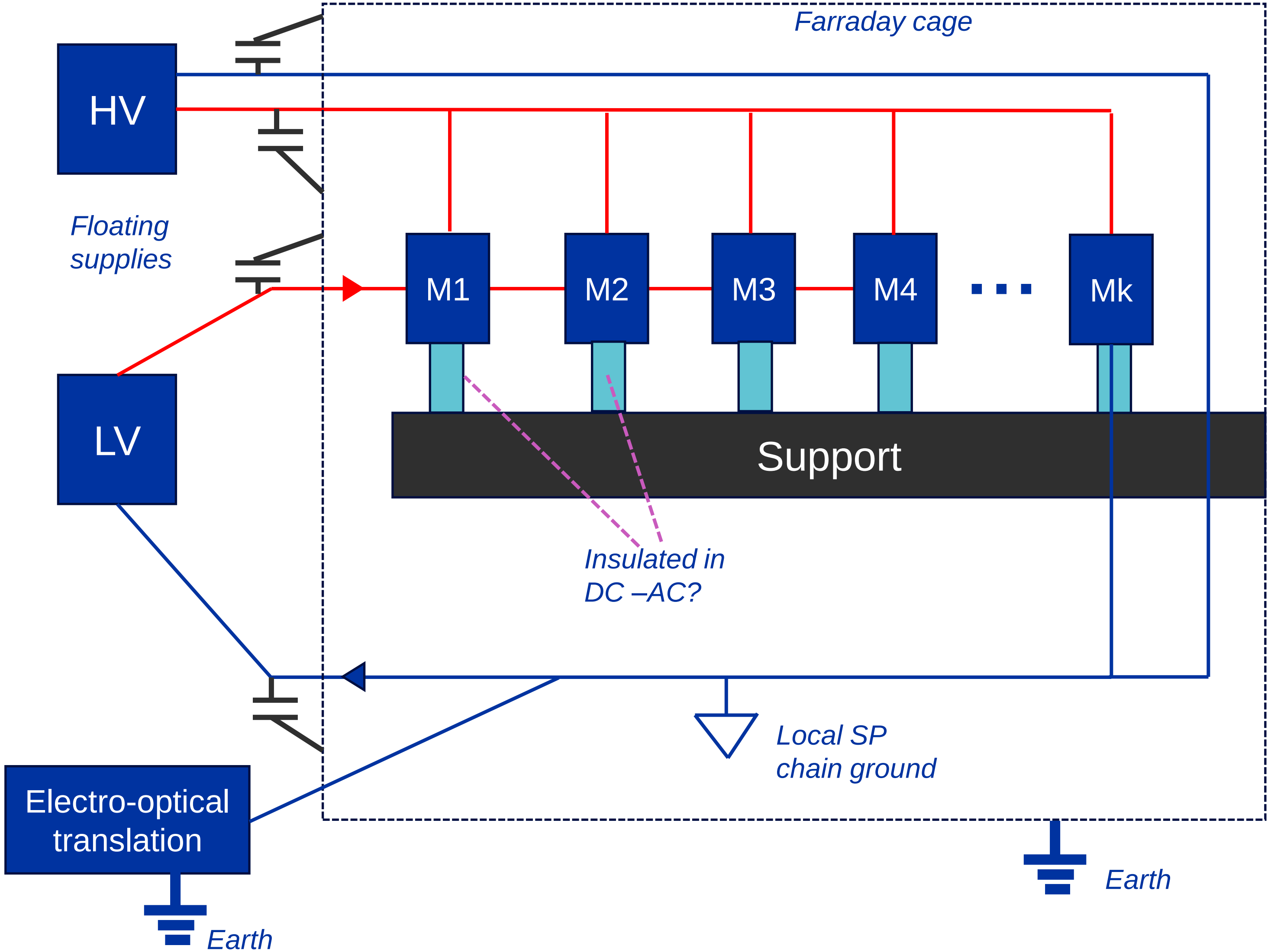
Grounding

No EMC rules/standards to guide designs. Noise?

→ *Prototype characterizations, how?*

→ *Different solutions implemented by different sub-detectors*

Complicated ESD safety, support structure grounding.



Failure modes..

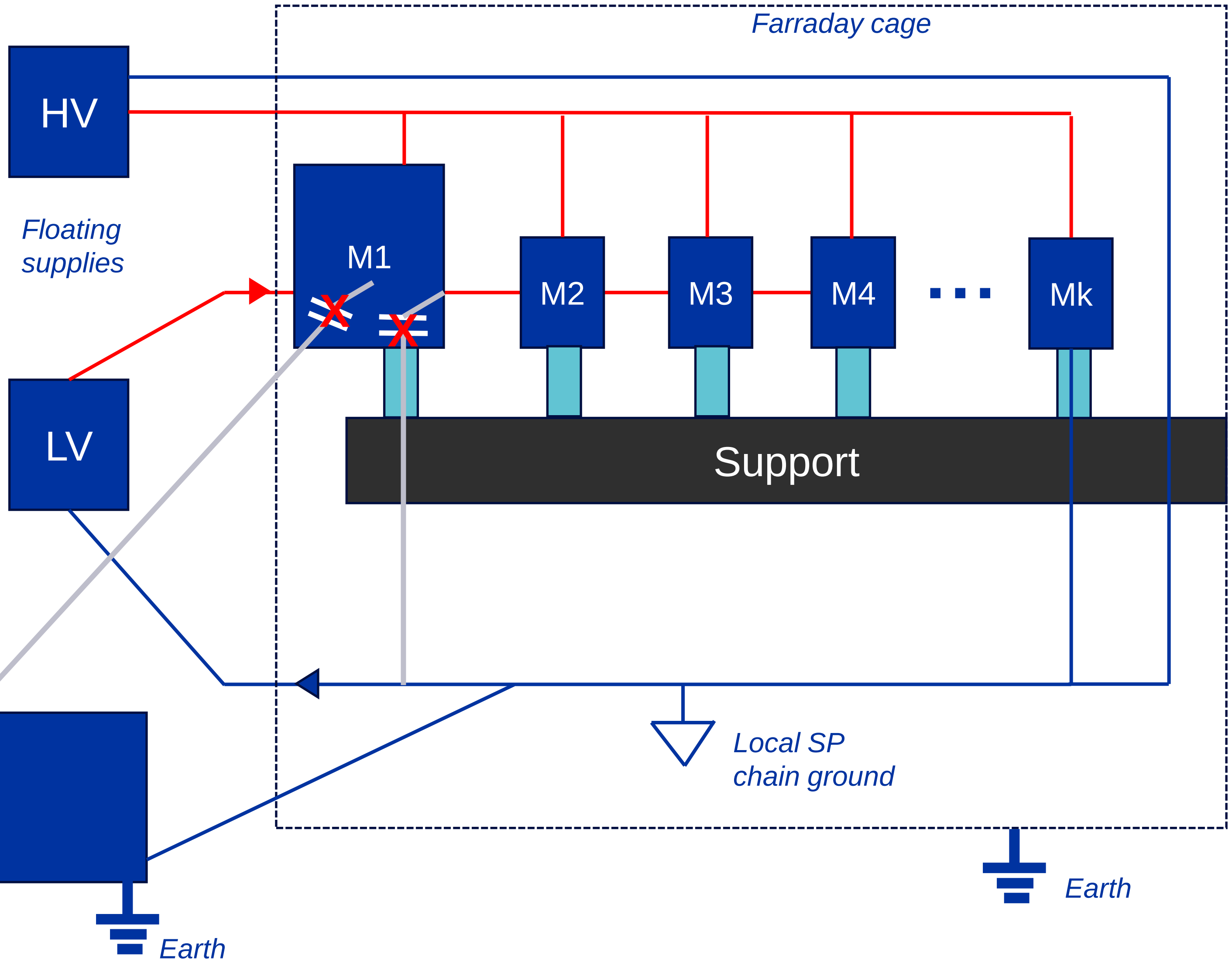
What happens if a capacitor (e.g. data AC coupling, Ground decoupling) fails?

- **Does the optosystem survive?**

- **Do you lose the full chain?**

Leakage currents through capacitors in weird configurations (Optoboard OFF, SP chain ON)

- **Need to think about all possibilities and prevent them!**

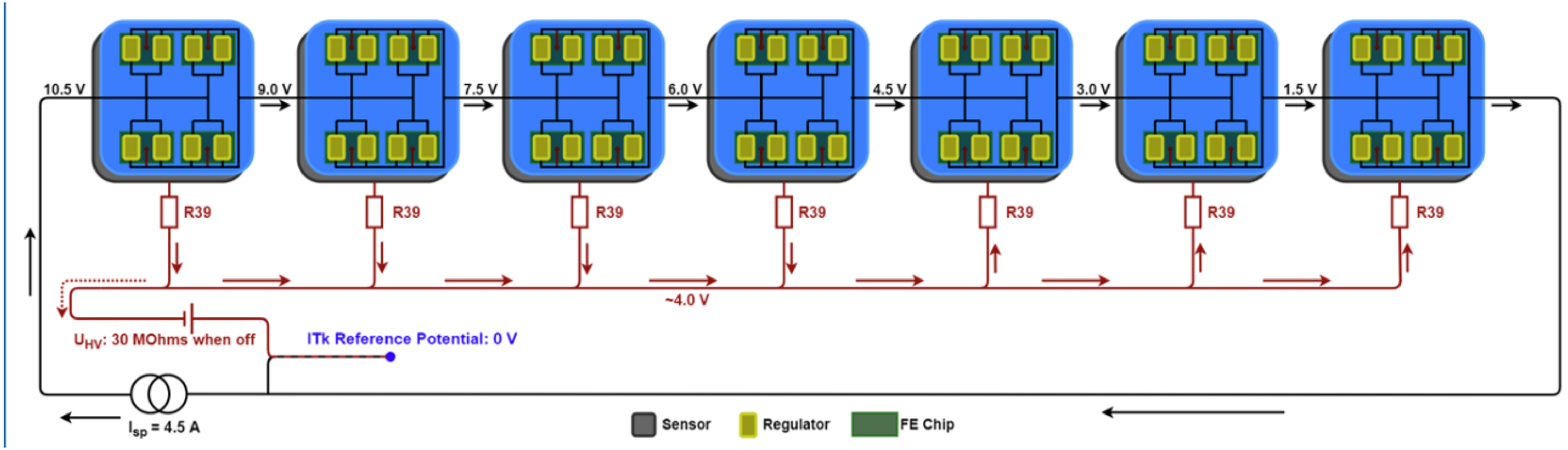


Sensor Biasing

If you share HV channels:

- **Sensors will not be biased with identical levels**

- **HV power supplies: High impedance when off → some sensors are forward biased in this condition**



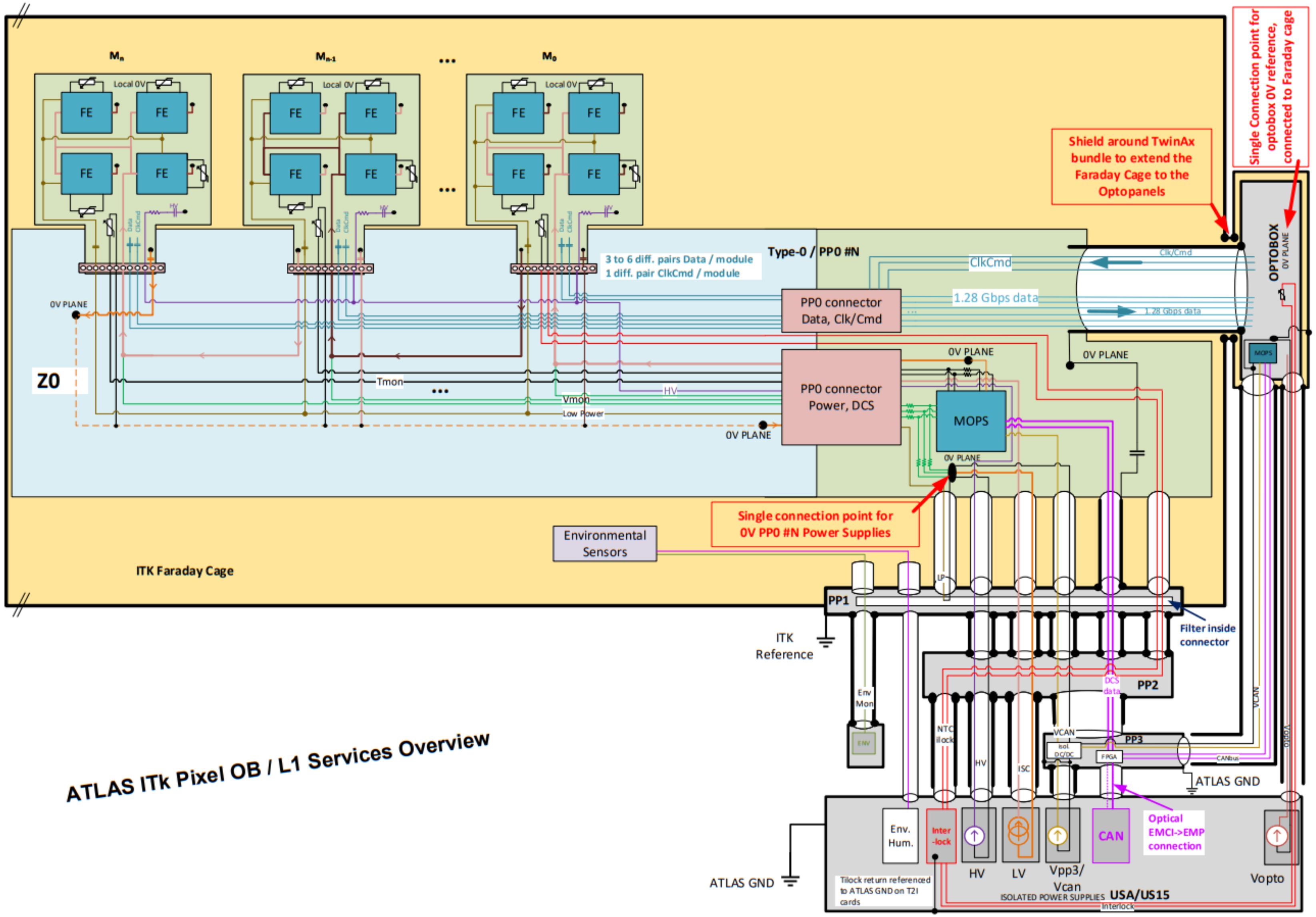
Bonus: **No way to *not* bias *all* sensors even with HV off!**

Conclusion

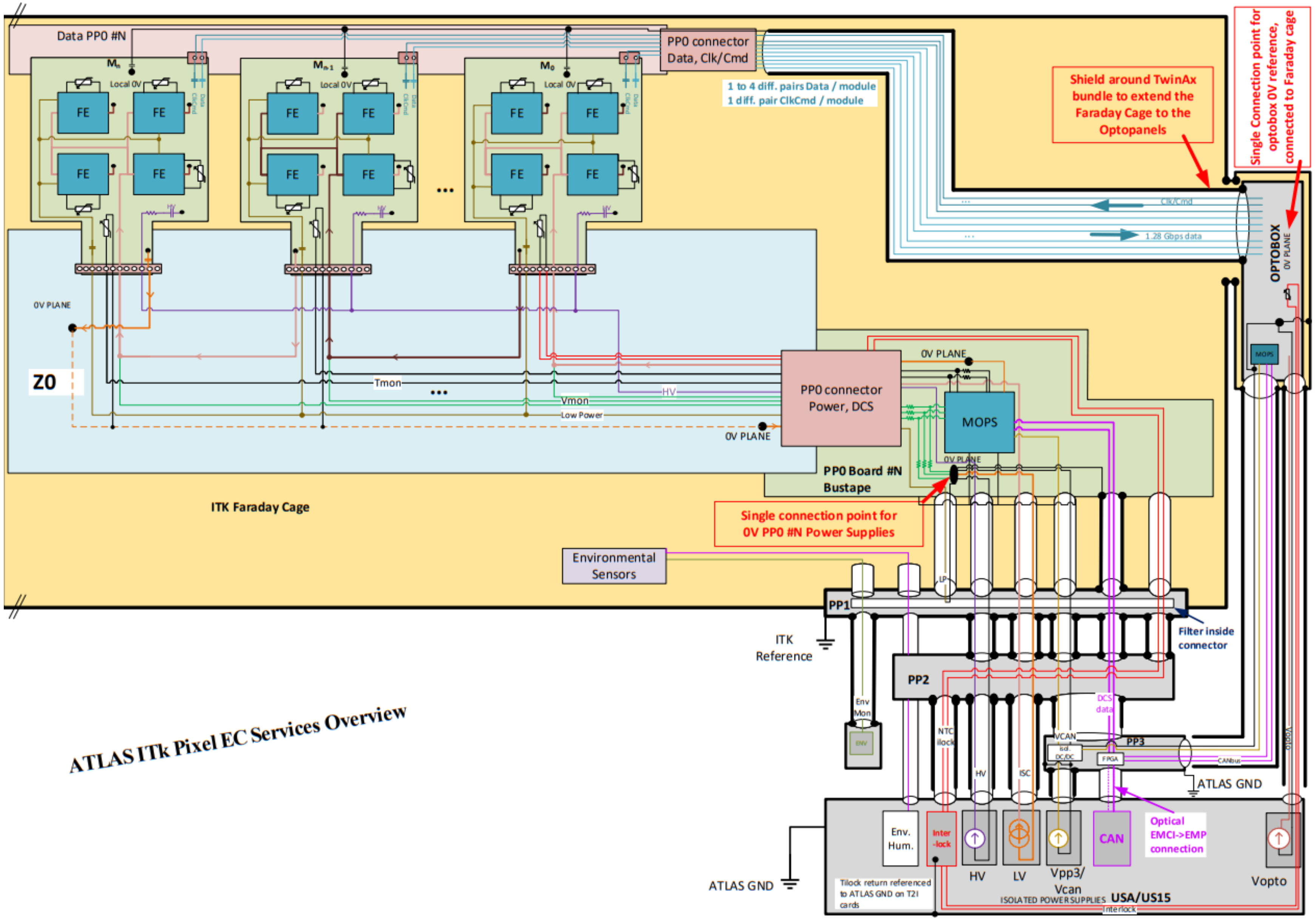
- **Right now, it seems to be working/ can work – Issues are still being uncovered.**
- **It’s very complicated: If you want to leave nothing to chance, it is a <u>major</u> undertaking.**
- **M. Karagounis: “Serial Powering is an experiment in an experiment” – valid to this day, will/would be valid for you too.**
- **Be careful, foresee… have fun ☺**

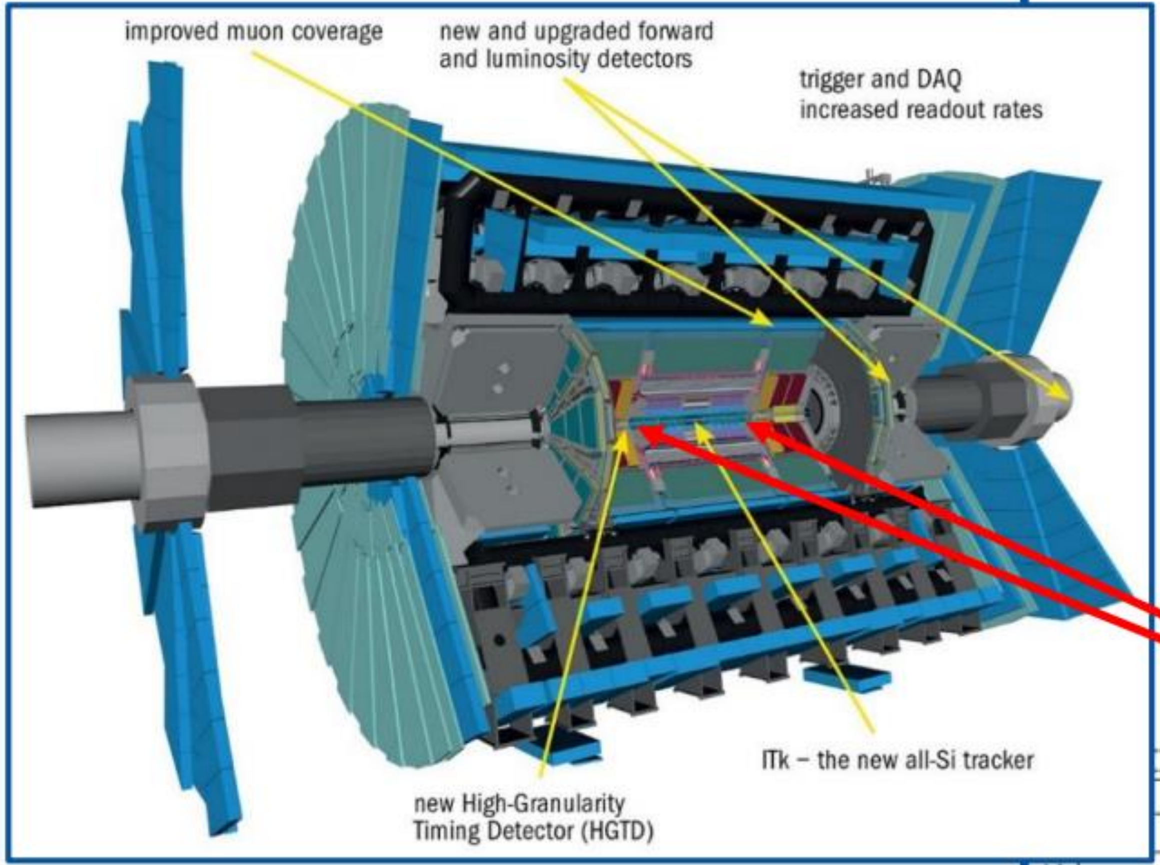
Personal views and experience – not exhaustive

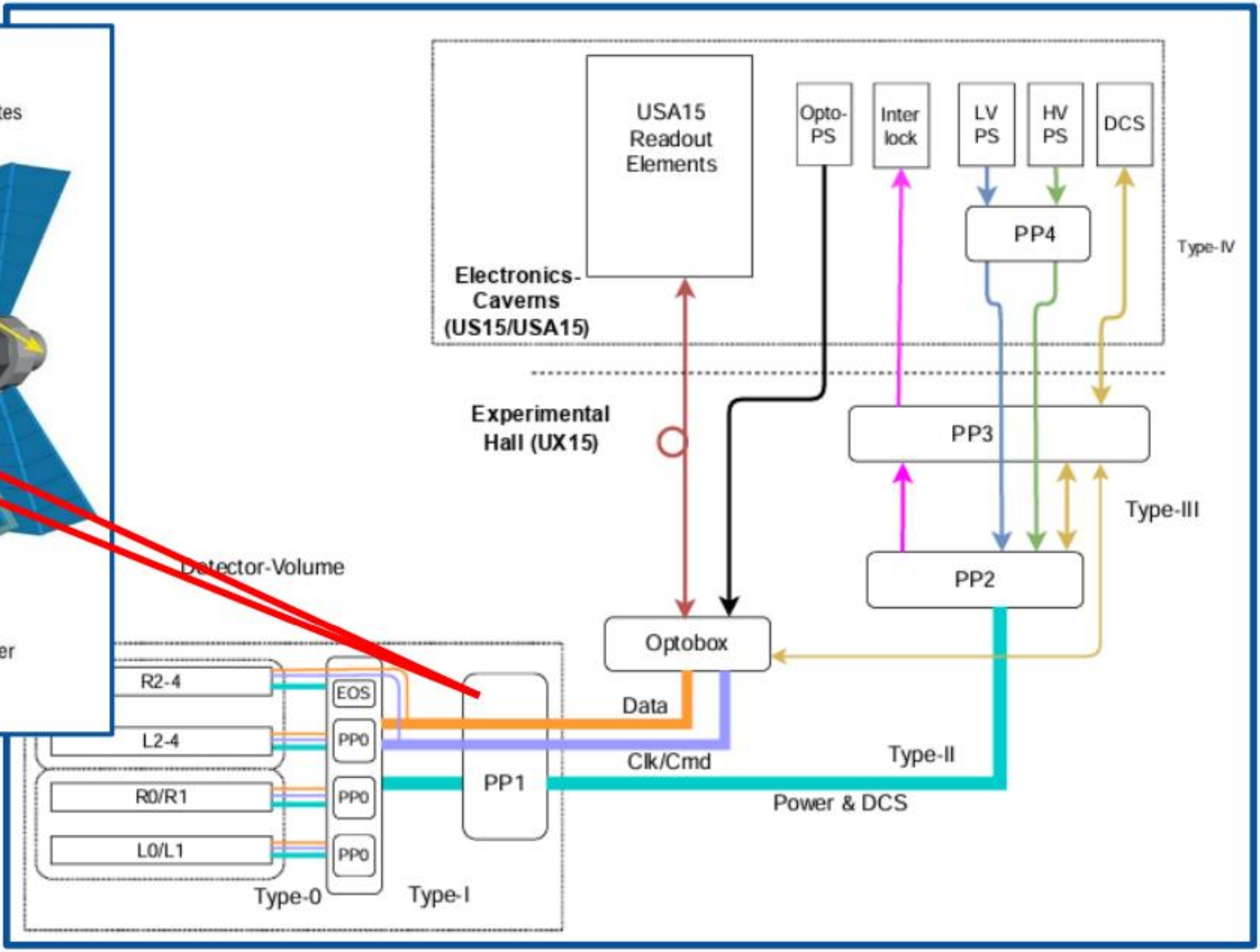
CERN



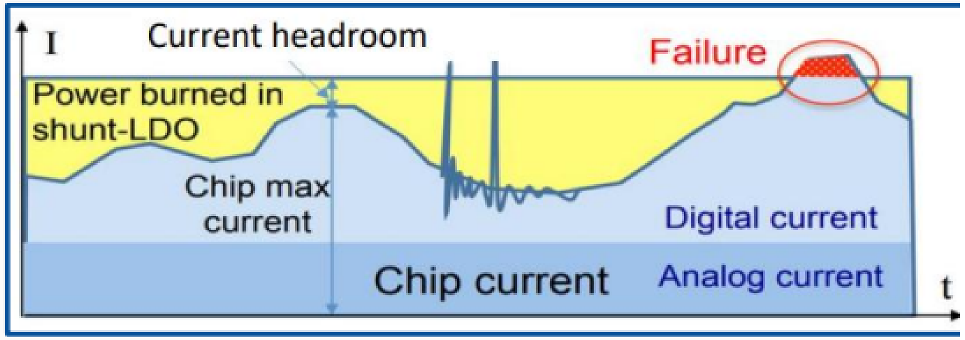
Mn
Mn-1
M0
Local 0V
FE
3 to 6 diff. pairs Data / module
1 diff. pair ClkCmd / module
Type-0 / PP0 #N
ClkCmd
1.28 Gbps data
PP0 connector Data, Clk/Cmd
PP0 connector Power, DCS
MOPS
0V PLANE
Z0
Tmon
Vmon
Low Power
HV
Shield around TwinAx bundle to extend the Faraday Cage to the Optopanels
Single Connection point for optobox 0V reference, connected to Faraday cage
OPTOBOX
Single connection point for 0V PP0 #N Power Supplies
Environmental Sensors
ITK Faraday Cage
PP1
Filter inside connector
ITK Reference
PP2
PP3
ATLAS GND
Env. Hum.
Inter -lock
HV
LV
Vpp3/ Vcan
CAN
Optical EMCI->EMP connection
Vopto
Tilock return referenced to ATLAS GND on T2I cards
ISOLATED POWER SUPPLIES
USA/US15
ATLAS ITk Pixel OB / L1 Services Overview


Data PP0 #N
PP0 connector
Data, Clk/Cmd
1 to 4 diff. pairs Data / module
1 diff. pair ClkCmd / module
Shield around TwinAx bundle to extend the Faraday Cage to the Optopanels
Single Connection point for optobox 0V reference, connected to Faraday cage
FE
Local 0V
Clk/Cmd
1.28 Gbps data
OPTOBOX
0V PLANE
MOPS
Z0
Tmon
Vmon
Low Power
HV
PP0 connector
Power, DCS
PP0 Board #N
Bustape
Single connection point for 0V PP0 #N Power Supplies
ITK Faraday Cage
Environmental Sensors
PP1
ITK Reference
Filter inside connector
PP2
PP3
ATLAS GND
CAN
Optical EMCI->EMP connection
Env. Hum.
Inter-lock
HV
LV
Vpp3/ Vcan
Vopto
ISOLATED POWER SUPPLIES
USA/US15
ATLAS ITk Pixel EC Services Overview


improved muon coverage
new and upgraded forward and luminosity detectors
trigger and DAQ increased readout rates
ITk – the new all-Si tracker
new High-Granularity Timing Detector (HGTD)


USA15 Readout Elements
Opto-PS
Inter lock
LV PS
HV PS
DCS
PP4
Type-IV
Electronics-Caverns (US15/USA15)
Experimental Hall (UX15)
PP3
Type-III
PP2
Detector-Volume
Optobox
R2-4
EOS
L2-4
PP0
R0/R1
PP0
L0/L1
PP0
PP1
Data
Clk/Cmd
Type-II
Power & DCS
Type-0
Type-I

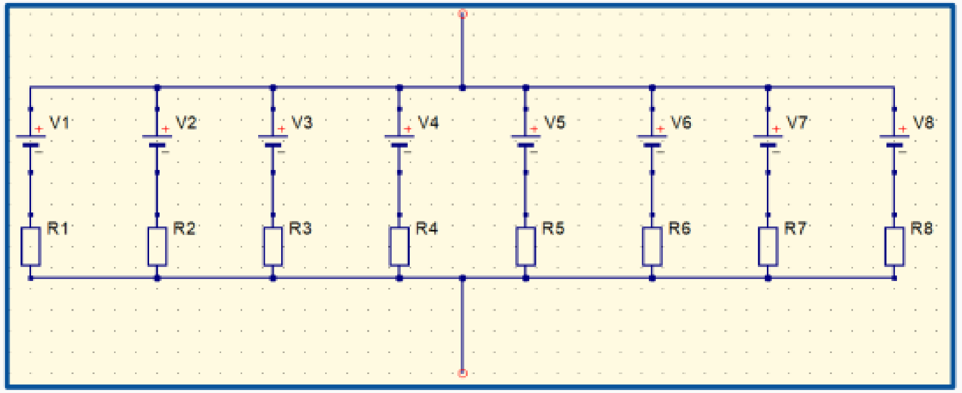
Matthias Hamer – Serial powering
https://indico.gsi.de/event/23364/attachments/53645/80986/SerialPowering_GSISeminar_17112025_v2.pdf



- can determine 'nominal' input current per chip
  - add a little overhead for 'unusual events'
- consider current distribution on module
  - analyse configuration phase space and add appropriate overhead current!
  - tolerances, process variation, manufacturing variability!

$$I_{\text{in}} = \left(1 + s_{\text{global}}\right) \sum_i I_{\text{Load},i}$$

$$I_j = \frac{I_{\text{in}}}{\sum_i \frac{R_j}{R_i}} + \frac{\sum_i \frac{V_i}{R_i}}{\sum_i \frac{R_j}{R_i}} - \frac{V_j}{R_j}$$



$$I_i \geq I_{\text{Load},i} \cdot \left(1 + s_{\text{min},i}\right)$$