

# Summary of SLDO tests

**From RD53A to SLDO testchip C**

**Part 1**

CMS SLDO review, 28. January 2020

<https://indico.cern.ch/event/879967/>

# Measurements overview

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## ❑ General

- Variation from wafer probing (Slope and Offset)
- Preregulator bandgap voltage increase in testchip C
- Load transient
- Overview of irradiation campaigns

## ❑ Undershunt protection

- Load regulation
- Dynamic behavior

## ❑ Overvoltage protection

- Line regulations with different configurations
- Dynamic behavior

## ❑ Start up

- Start up in RD53A
- Measurements with start up circuitry

## ❑ Low power mode

- With external signal (RD53B)
- With internal signal (not in RD53B)

# Reminder: SLDO test chips overview

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## 1. SLDO test chip A – August 2018 submission:

- New bandgap scheme ⇒ Improved line regulation
- Overload protection (= Under shunt protection) ⇒ Limits transient propagation to other chips

## 2. SLDO test chip B – November 2018 submission:

- Overvoltage protection ⇒ Limits maximum input voltage
- Low power mode ⇒ Operation with low input current
- New start up circuitry ⇒ Earlier start up
- Improvements in bandgap scheme

## 3. SLDO test chip C – February 2019 submission:

- Improvements in start up stability
- Increase of preregulator bandgap output by 25 mV

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## ❑ Undershunt protection

- Load regulation
- Dynamic behavior

## ❑ Overvoltage protection

- Line regulations with different configurations
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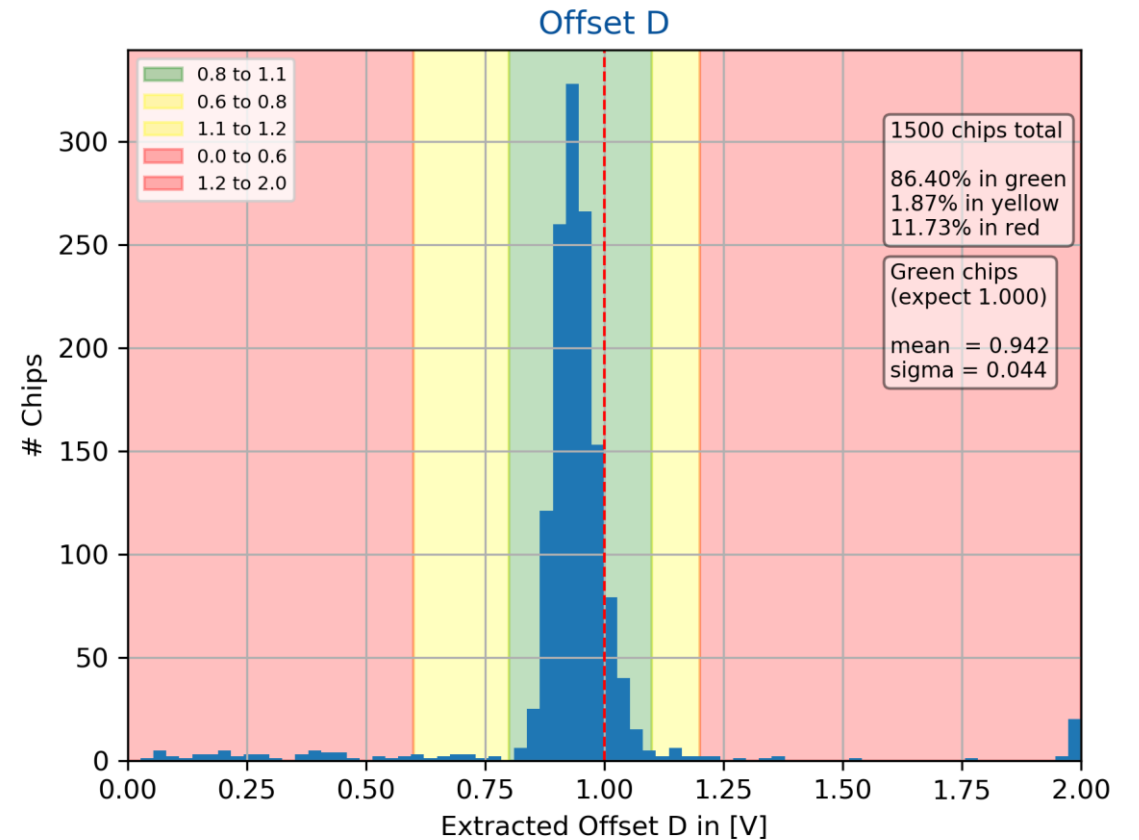
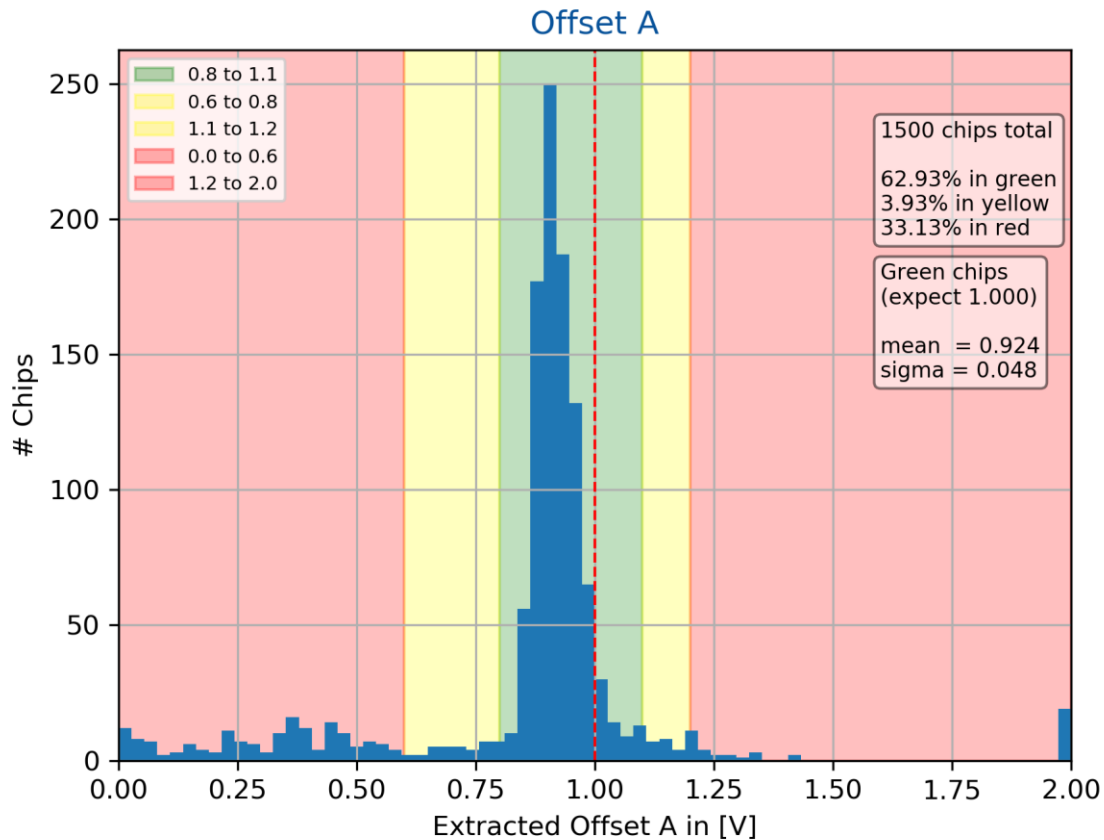
## ❑ Start up

- Start up in RD53A
- Measurements with start up circuitry

## ❑ Low power mode

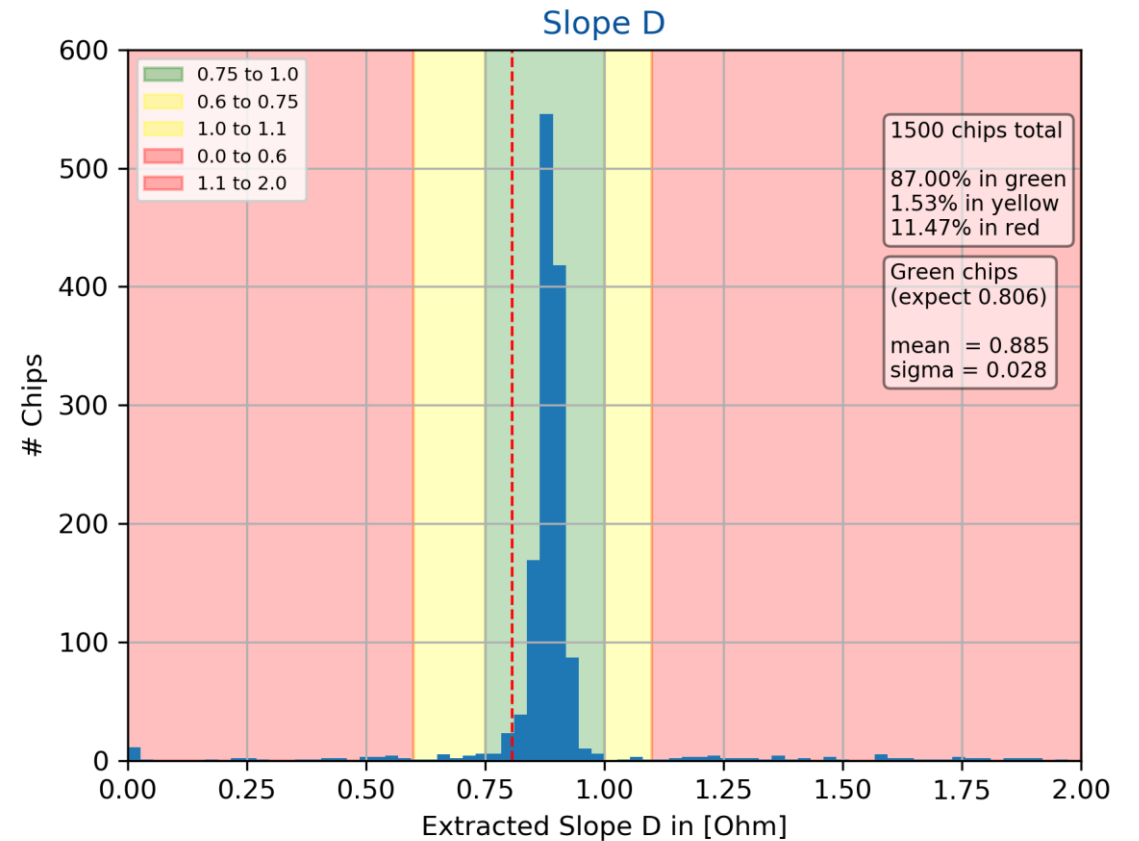
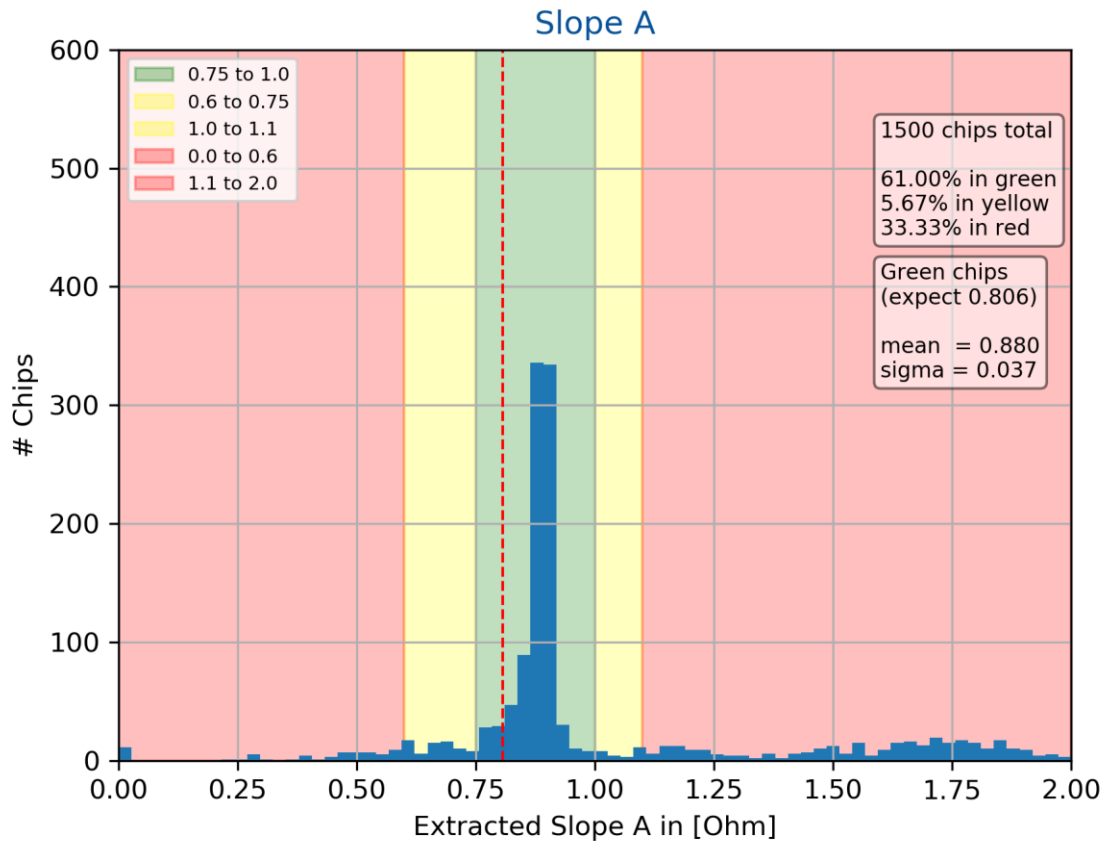
- With external signal (RD53B)
- With internal signal (not in RD53B)

# Wafer probing - Extracted Offsets



- Extracted offset is 60-80 mV lower than expected (as already seen)
- Sigma is around 45 mV (4 to 5%) => expected to improve with RD53B (trimming + sharing)

# Wafer probing - Extracted Slope

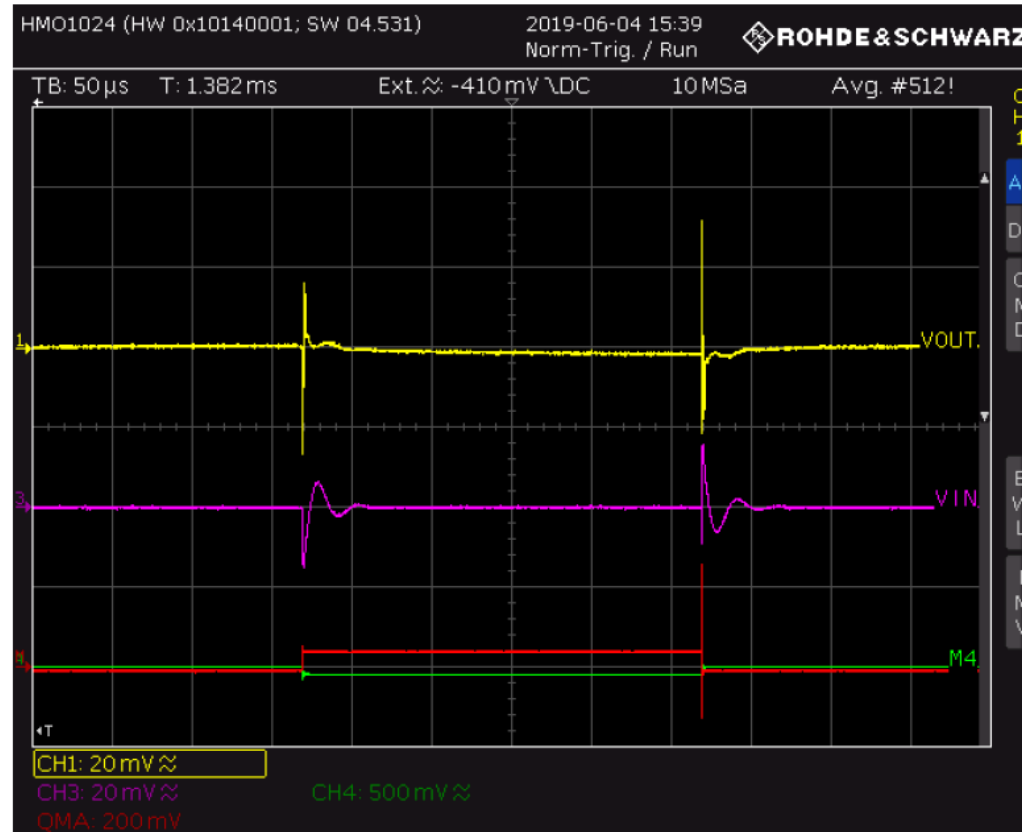


- Extracted slope is around 80 mΩ higher than expected (as already seen)
- Sigma is around 35 mΩ (3 to 4%)

# Load transient

## Load Transient - SLDO

Vofshalf=400mV, Vref=600mV, Irefset=1110, Rext=600Ω, Vwave=1.96Vpp,  
Iload=0-500mA, lin=1.7A

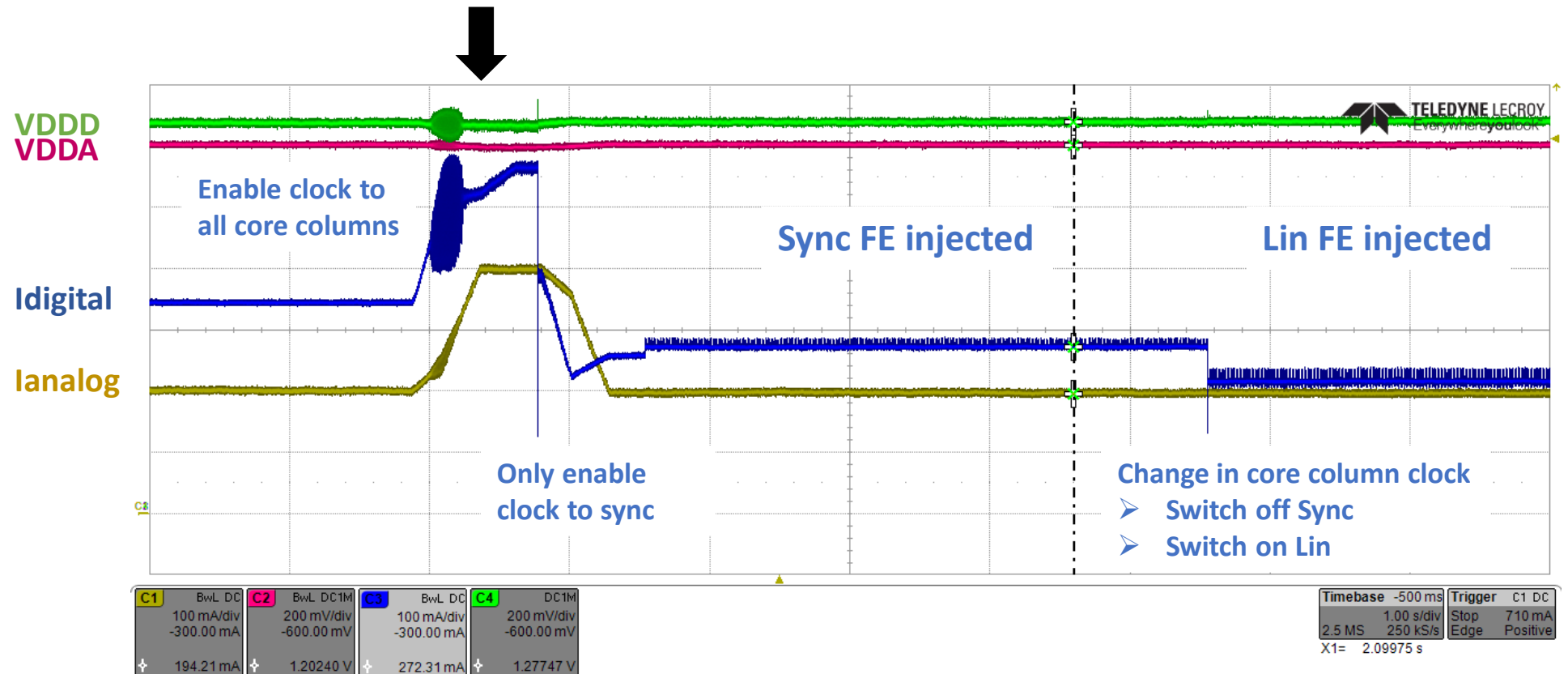


# Example of load transients in RD53A

- RD53A powered in direct powering by two SLDO testchip C
- Initiating digital injection scan (BDAQ v14)
  - => Causing  $\approx 40\text{mV}$  transient on VDDD (Very small variation on VIN and VDDA)

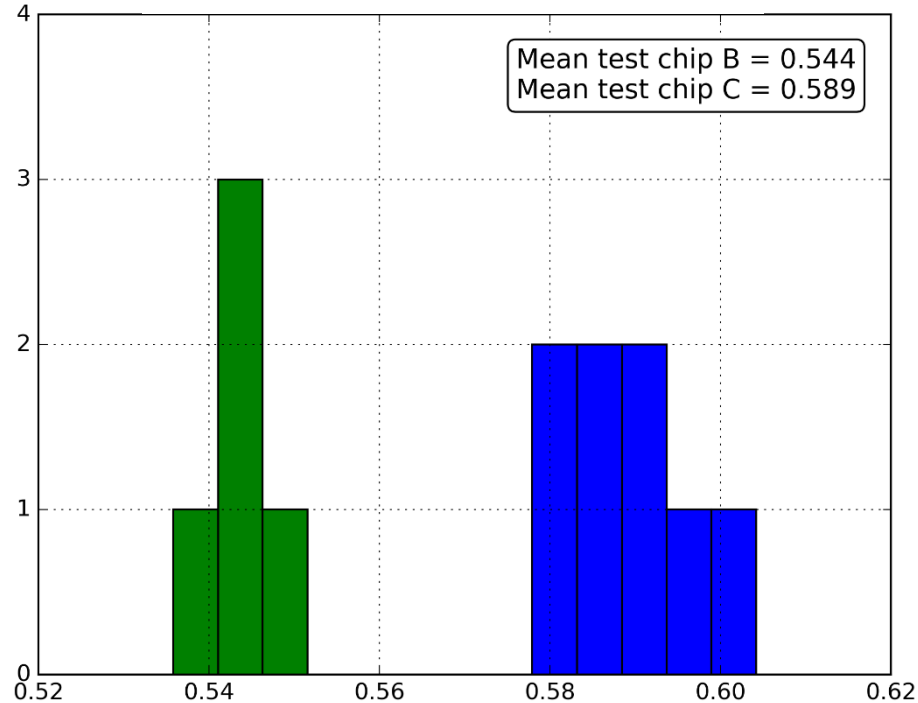
Probably causes the oscillations on module that are propagated to Vin seen by Vasilije:

[https://indico.cern.ch/event/829670/contributions/3473445/attachments/1886831/3110713/SP\\_meeting\\_27\\_Jul.pdf](https://indico.cern.ch/event/829670/contributions/3473445/attachments/1886831/3110713/SP_meeting_27_Jul.pdf)

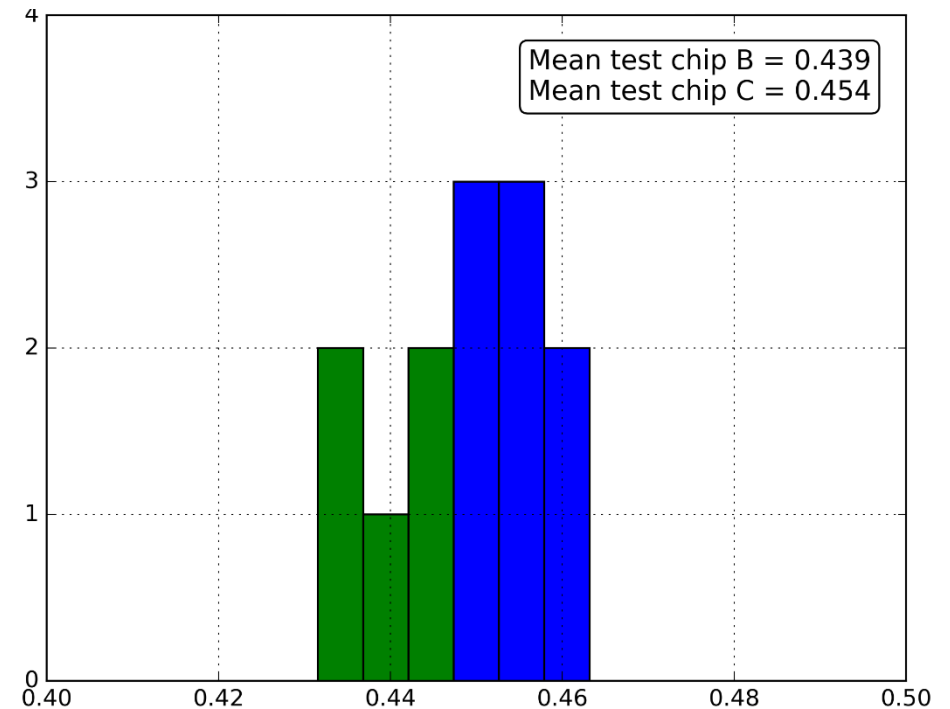


# Bandgap output voltages Testchip B vs C

## Preregulator bandgap (increased by 25 mV)



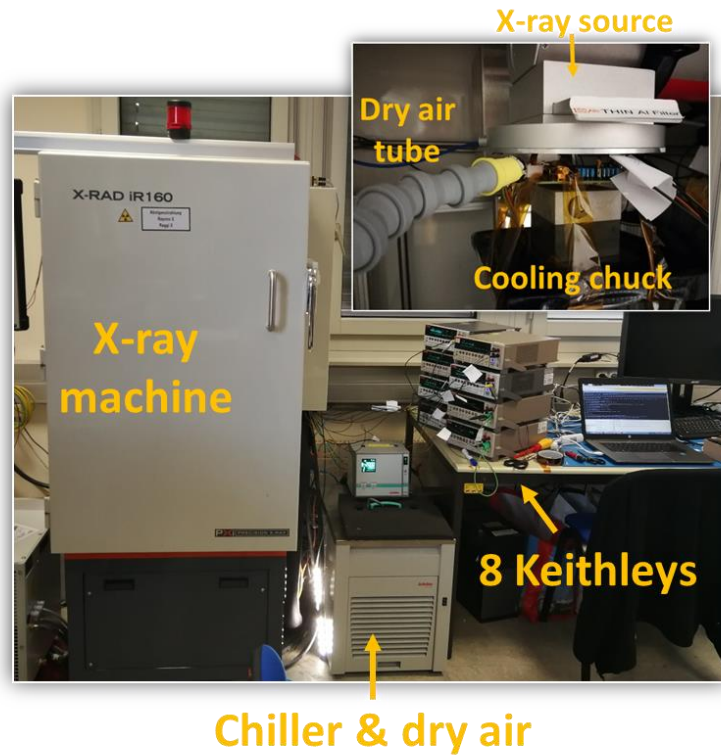
## Core bandgap (unchanged)



- ❑ Measured 5 testchip B and 8 testchip C with  $V_{in} \approx 1.5$  V
- ❑ Bandgap output voltage lower than in simulations
  - Increased preregulator bandgap ( $V_{ref\_pre}$ ) by 25 mV from test chip C on
    - Is reference for overvoltage protection
  - Core bandgap unchanged

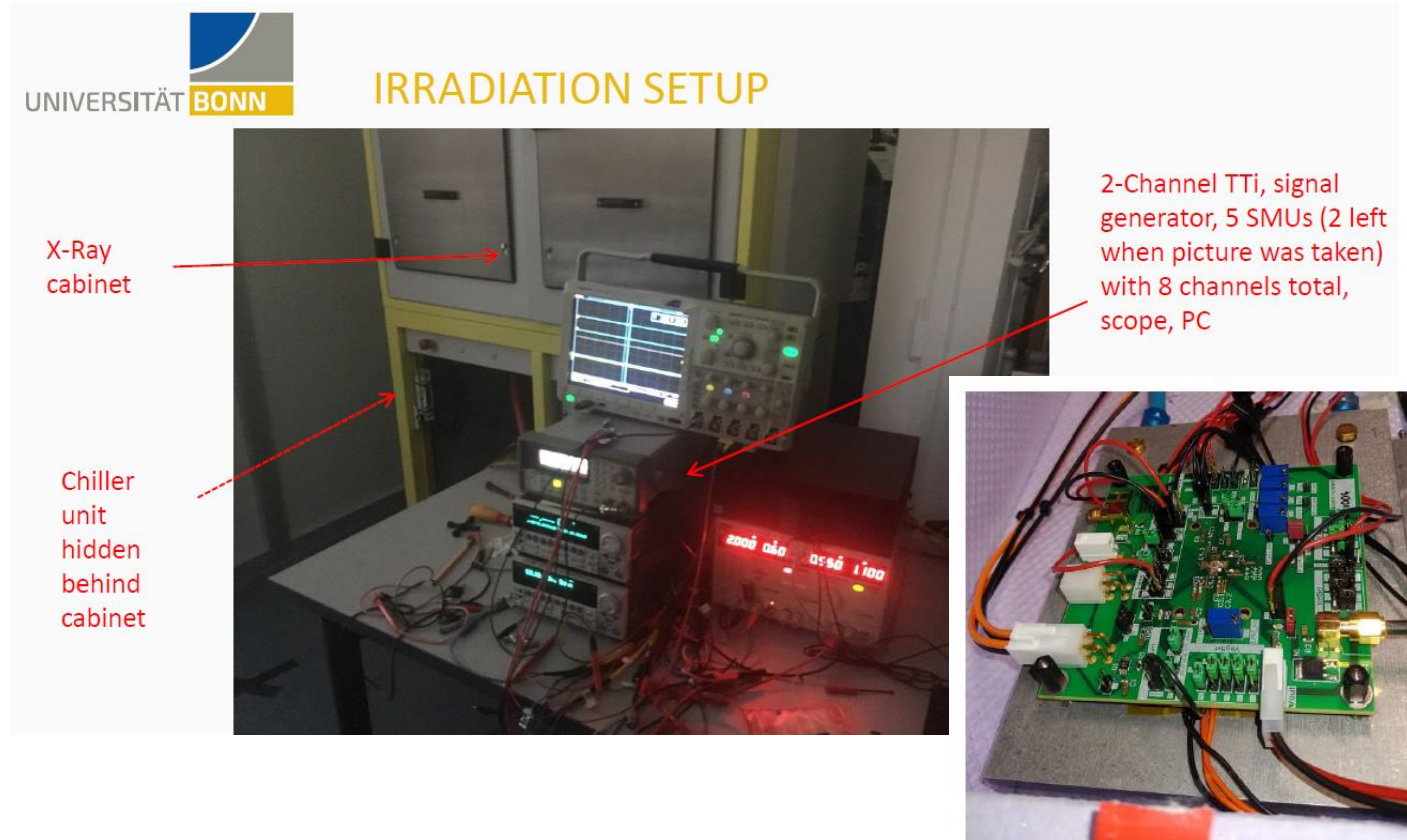
# Irradiation measurement

## CERN Irradiation setup



More details:

[https://indico.cern.ch/event/829670/contributions/3473422/attachments/1886884/3110807/CERN\\_SLDO\\_tests.pdf](https://indico.cern.ch/event/829670/contributions/3473422/attachments/1886884/3110807/CERN_SLDO_tests.pdf)



More details in Florian's talk:

<https://indico.cern.ch/event/829670/contributions/3473423/attachments/1886799/3110659/TID.pdf>

# Irradiation measurement

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➤ Testchip A up to 600 Mrad at 0C in March at CERN

- Line- and load regulation

[https://indico.cern.ch/event/829670/contributions/3473422/attachments/1886884/3110807/CERN\\_SLDO\\_tests.pdf](https://indico.cern.ch/event/829670/contributions/3473422/attachments/1886884/3110807/CERN_SLDO_tests.pdf)

➤ Testchip B up to 800 Mrad at -10C in June at Bonn

- Line- and load regulation
- New features overvoltage protection and undershunt protection

<https://indico.cern.ch/event/829670/contributions/3473423/attachments/1886799/3110659/TID.pdf>

➤ Testchip C currently being irradiated to 1Grad at Bonn TBC

# Testchip A irradiation: 1.6A

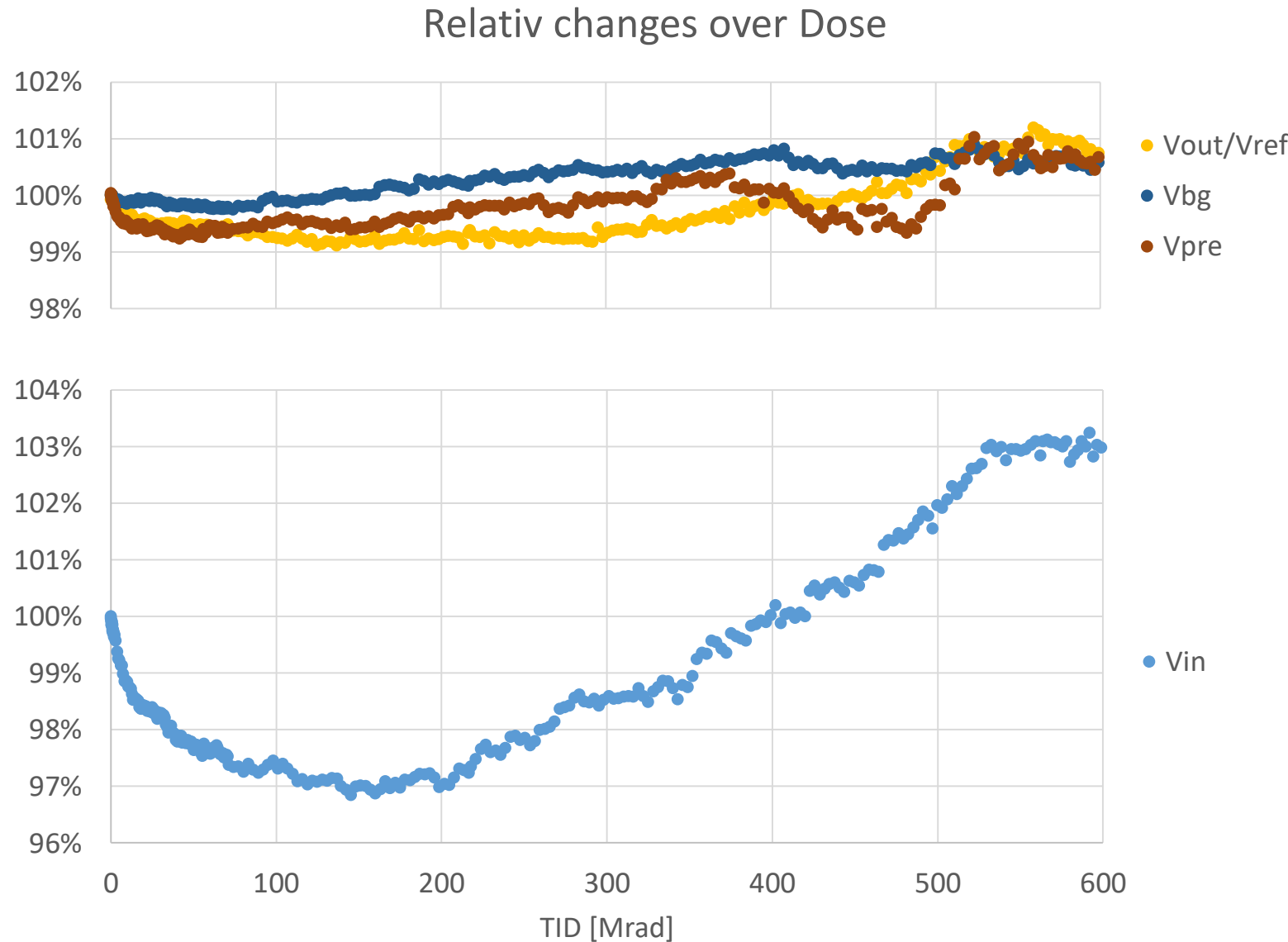
## Voltage trends over TID at lin =

Shunt-LDO is fully functional after 600Mrad:

- Output behaviour is very stable
- Bandgap voltages are very stable
- Variations of input behavior and Iref
  - Mainly due shift in Riref
  - Improved for RD53B

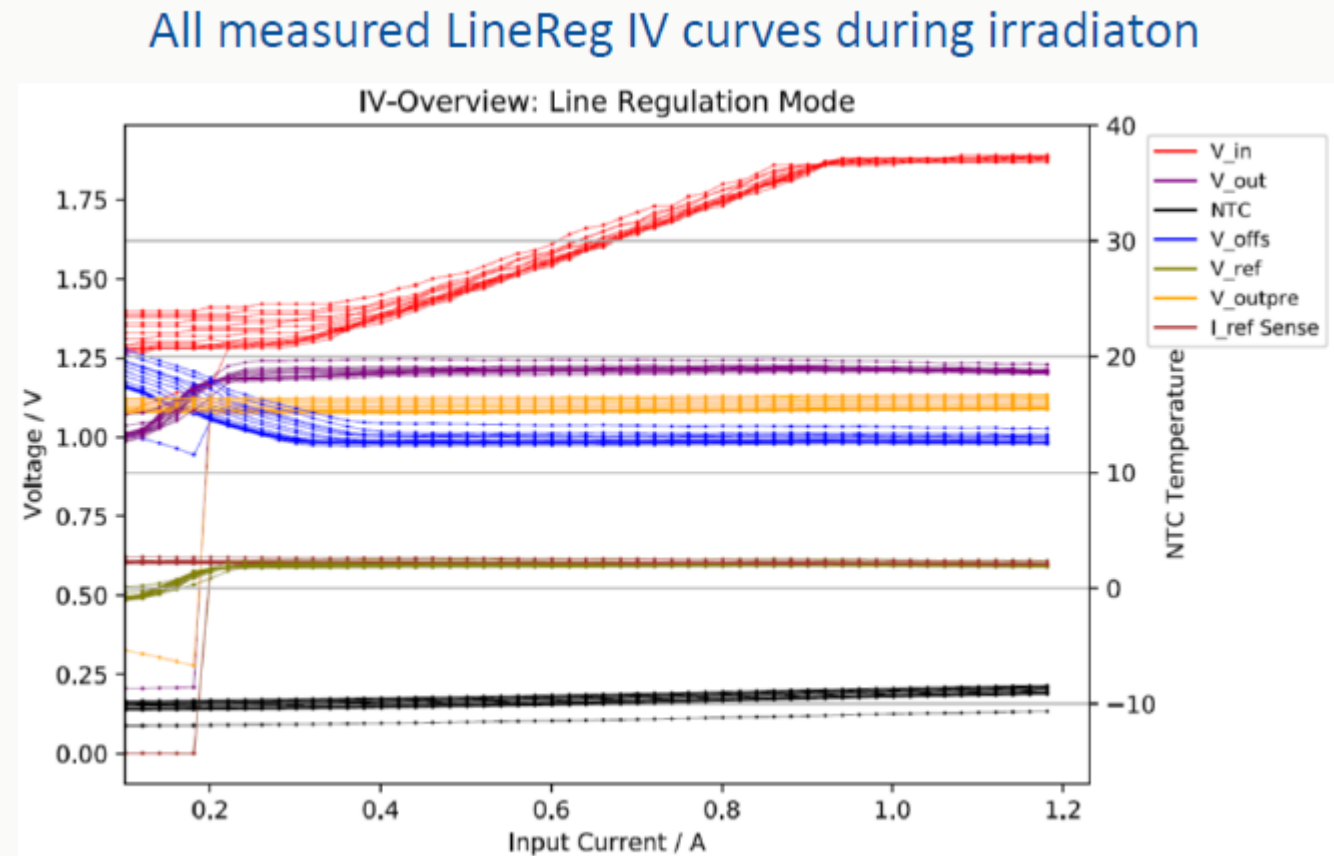
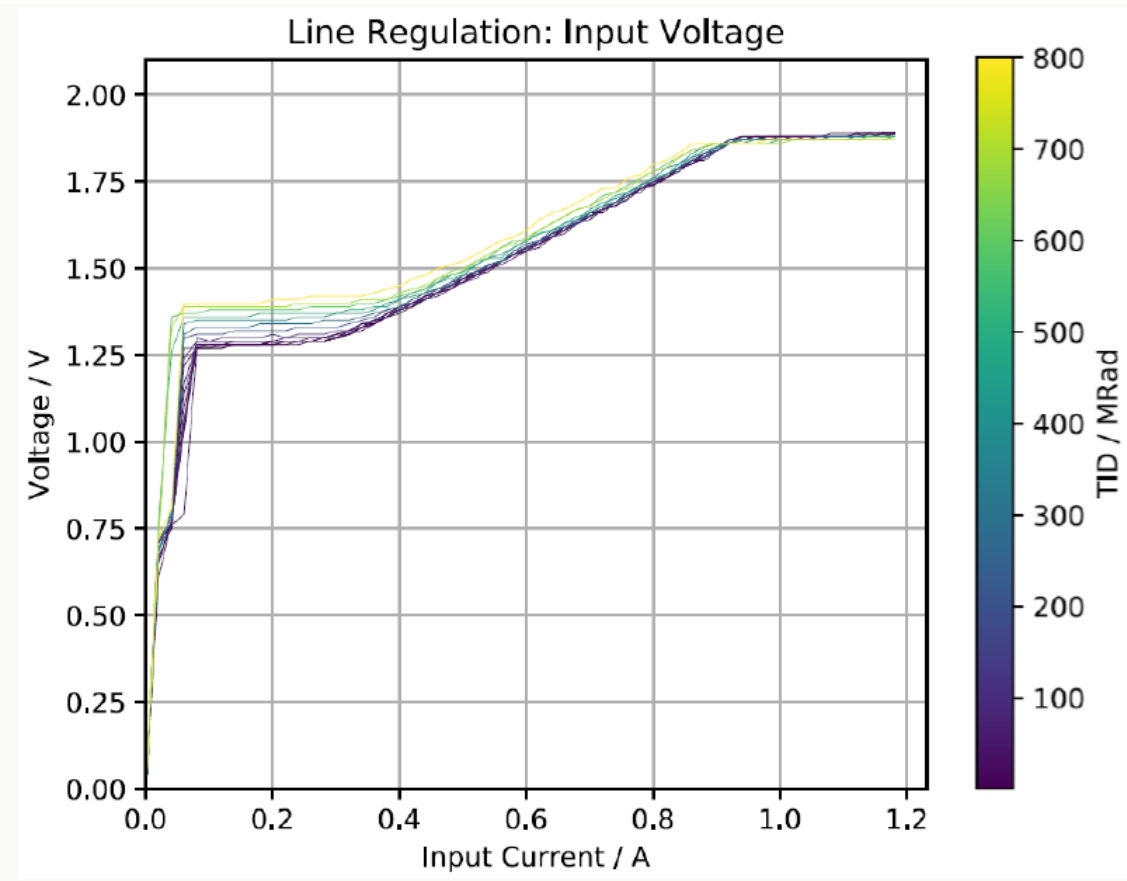
Reference values

	0 Mrad	600 Mrad	Delta
Vin	1.804	1.860	+56 mV
Vout/Vref	2.053	2.069	+0.80 %
Vbg	0.498	0.501	+ 3 mV
Vpre	1.141	1.148	+ 7mV



# Testchip B Irradiation:

# Line regulation



- ❑ Some variation of VIN can be observed, similar to testchip A, but less pronounced
- ❑ Overvoltage protection works well over TID

# Summary general

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## ❑ RD53A (and also all testchips)

- Differences in line regulation compared to simulation (Higher Slope, Lower offset)  
=> Fixed in RD53B
- Differences in line regulation compared

## ❑ Preregulator bandgap

- With increase  $V_{ref\_pre}$  is closer to 0.6V
- Measured mean of 0.59 V with  $V_{in} \approx 1.5V$

## ❑ Irradiation campaign

- Output and bandgap behavior very stable over TID (<1-2%)
- Some drift in VIN (slope and offset)
  
- Both worked well (apart of already fixed issues in A), but stopped working afterwards
  - Testchip A developed open behavior
  - Unclear why? (Maybe thermal, mechanical stress)