

Summary of SLDO tests

From RD53A to SLDO testchip C

Part 2

CMS SLDO review, 28. January 2020

<https://indico.cern.ch/event/879967/>

Overload/Undershunt protection

Measurements overview

❑ General

- Variation from wafer probing (Slope and Offset)
- Preregulator bandgap voltage increase in testchip C
- Load transient
- Overview of irradiation campaigns

❑ Undershunt protection

- Load regulation
- Dynamic behavior

❑ Overvoltage protection

- Line regulations with different configurations
- Dynamic behavior

❑ Start up

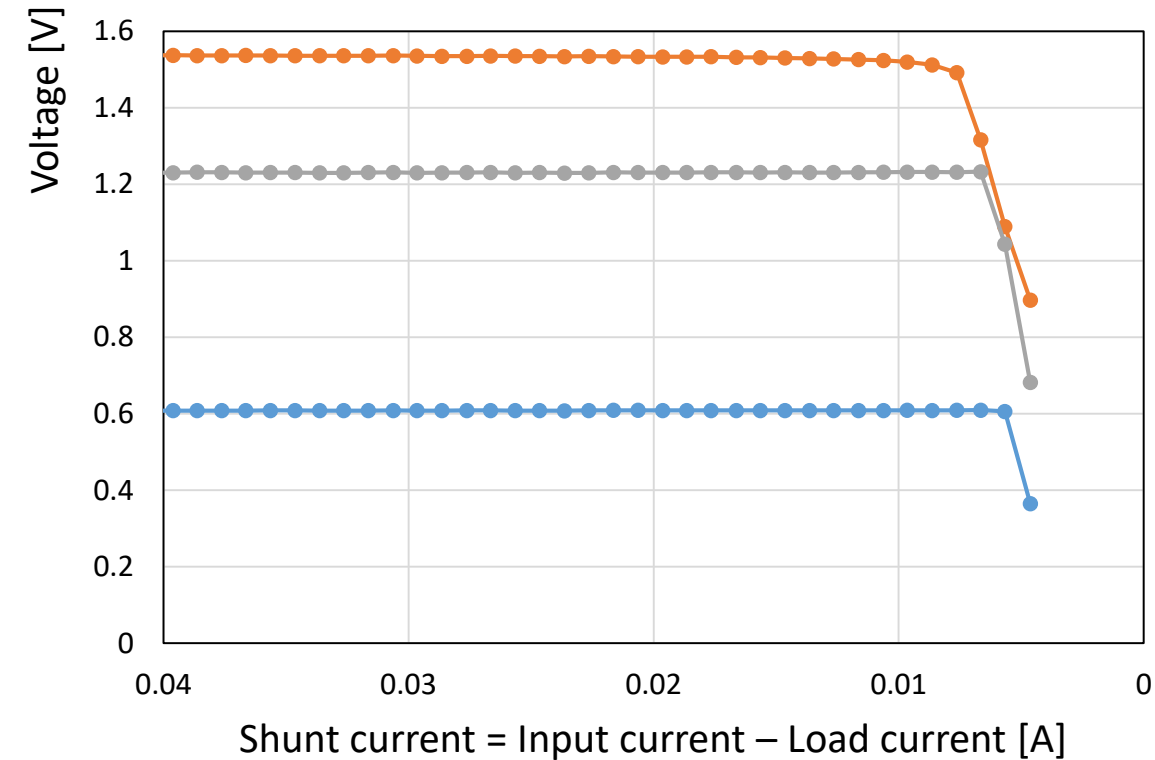
- Start up in RD53A
- Measurements with start up circuitry

❑ Low power mode

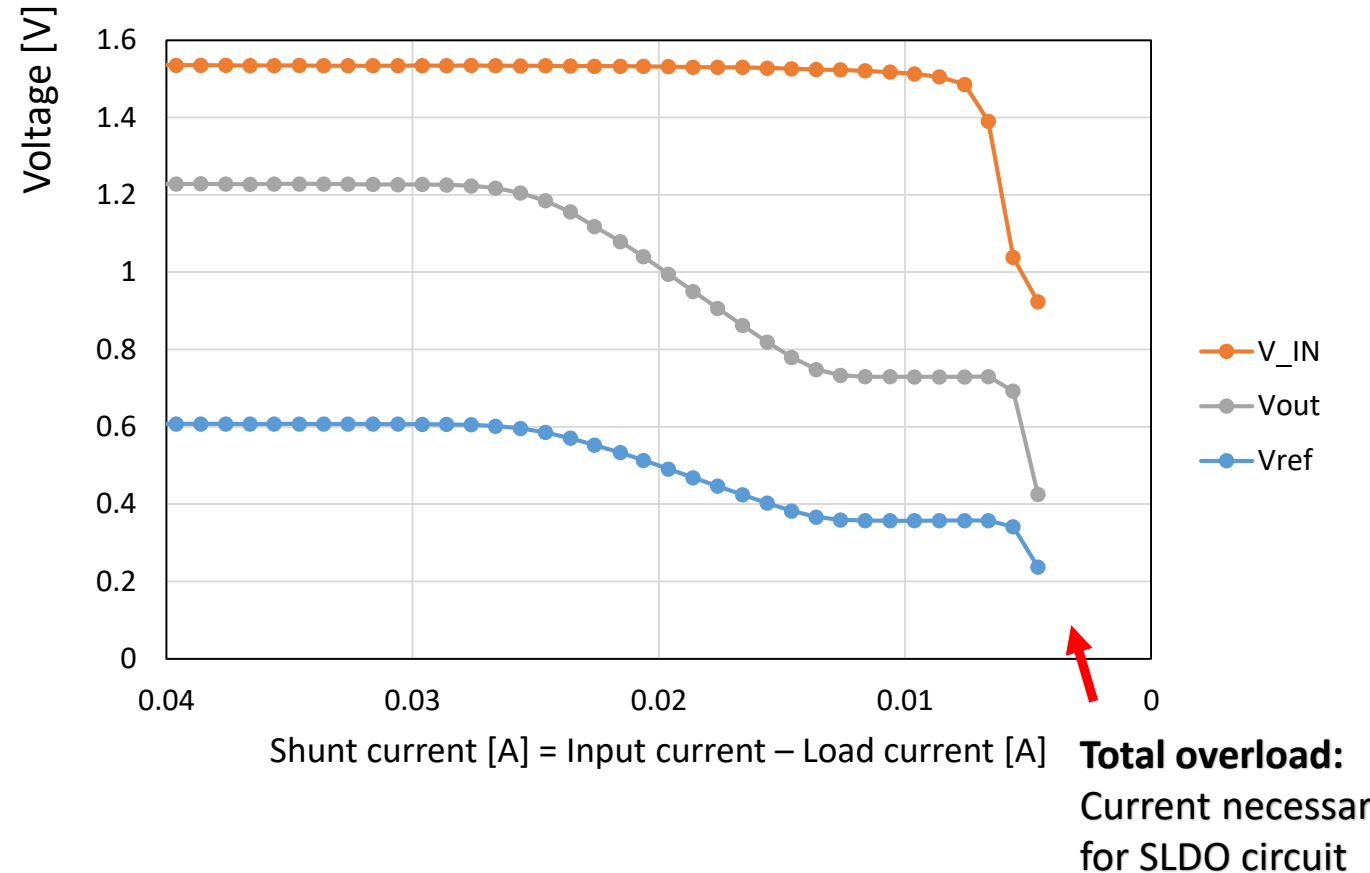
- With external signal (RD53B)
- With internal signal (not in RD53B)

Load regulation with under shunt protection

Under shunt protection **OFF**



Under shunt protection **ON**

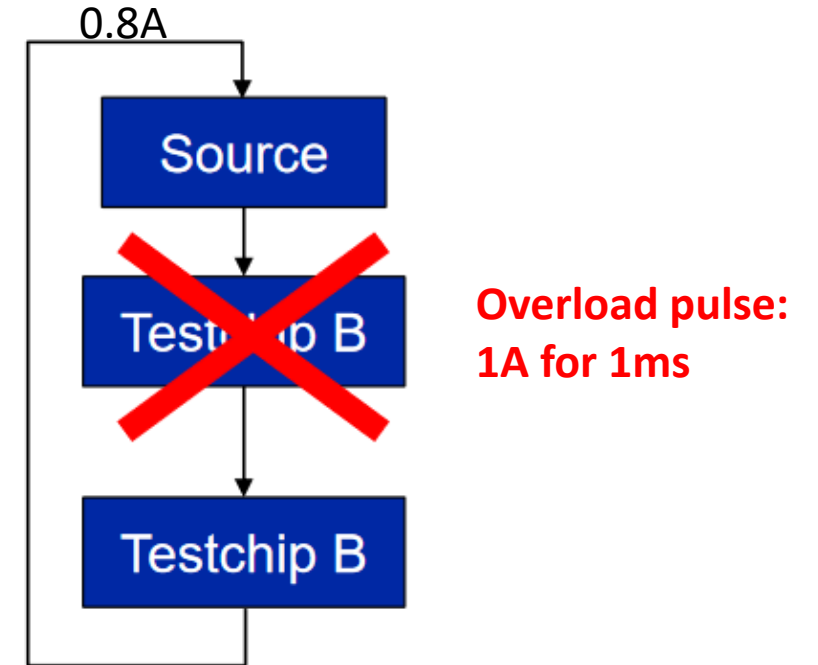


- When under shunt condition detected Vref and Vout are being reduced
- Threshold current when under shunt protection gets activated slightly higher than in simulations

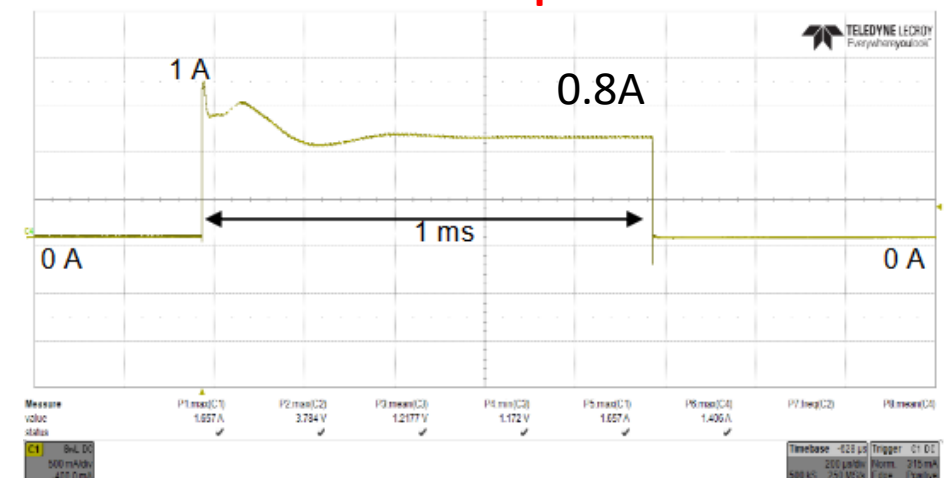
Overload scenario with two chips in series

- Two chips in series with same configuration
- Supply current = 0.8 A
- Creating overload on one chip

=> Measured response with and without undershunt protection



Measured 1ms overload pulse

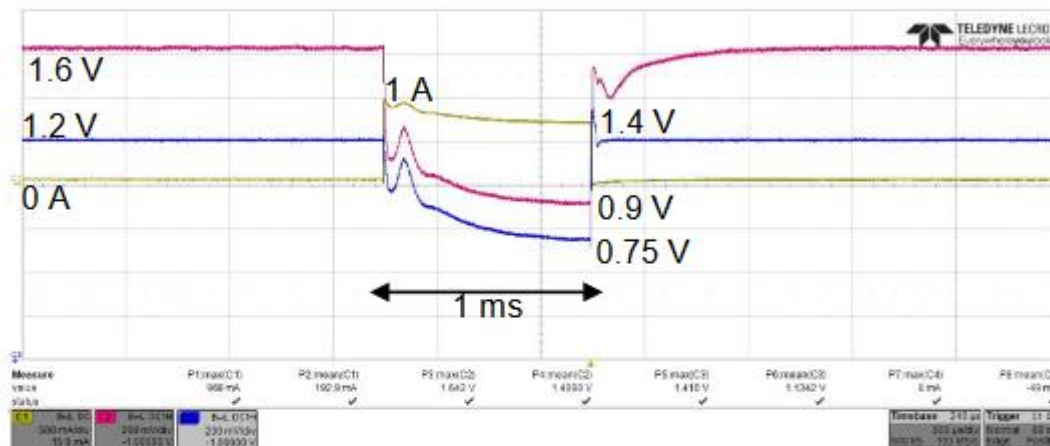


Overload example with 1 ms overload

Undershunt off

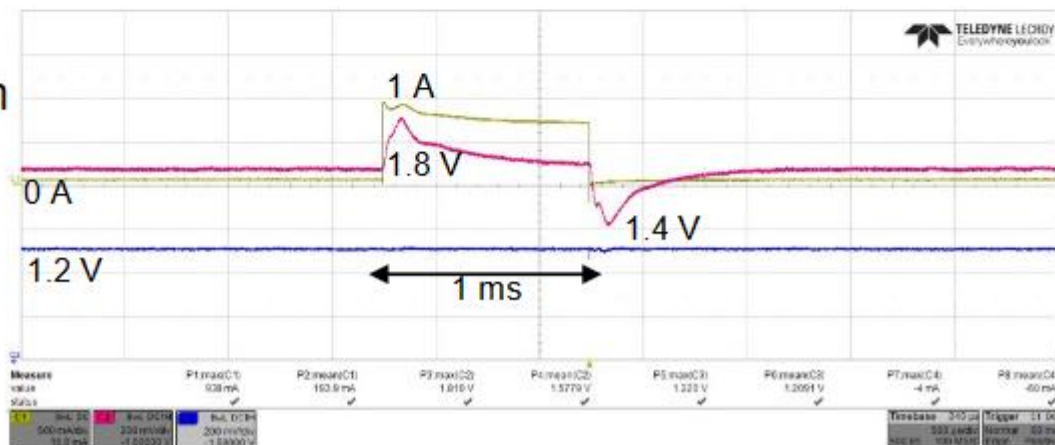
Upstream

- Iload
- Vin
- Vout



Downstream

- Iload
- Vin
- Vout



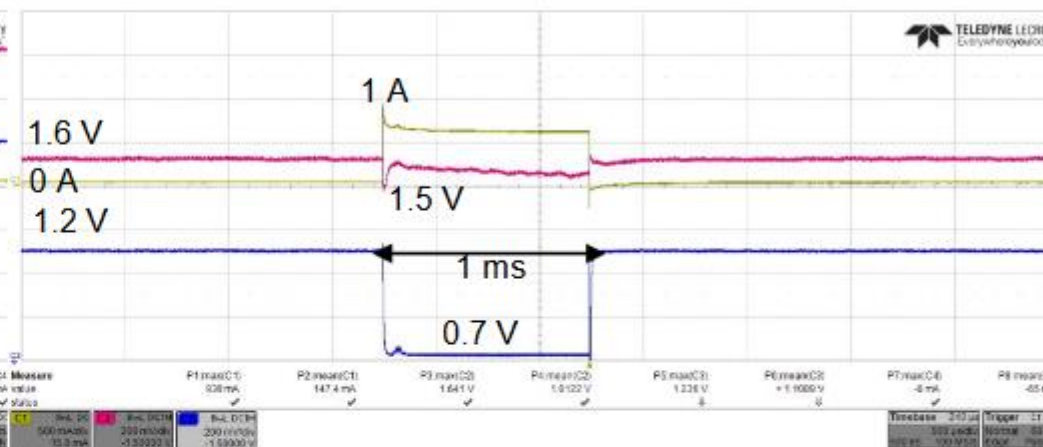
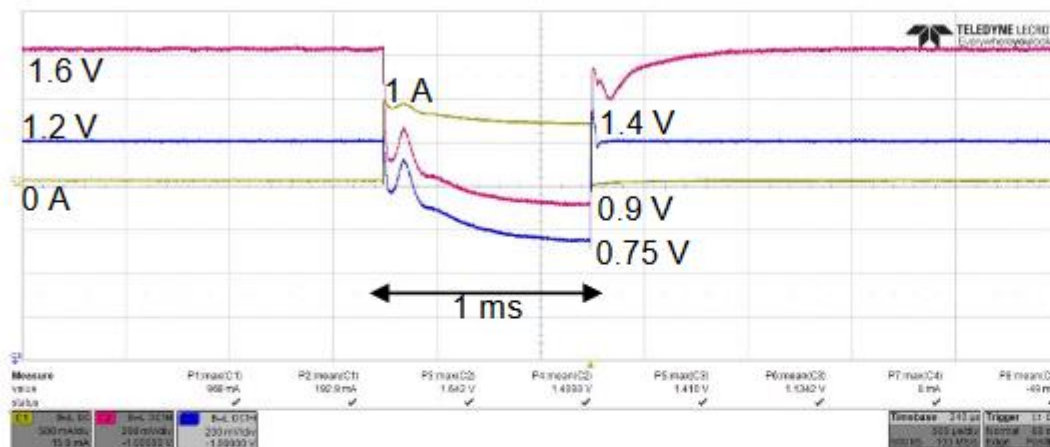
Overload example with 1 ms overload

Undershunt off

Undershunt on

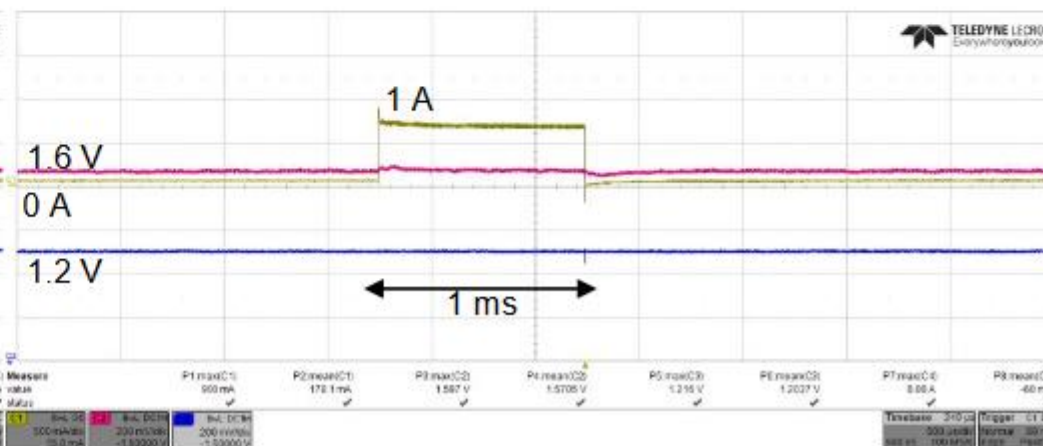
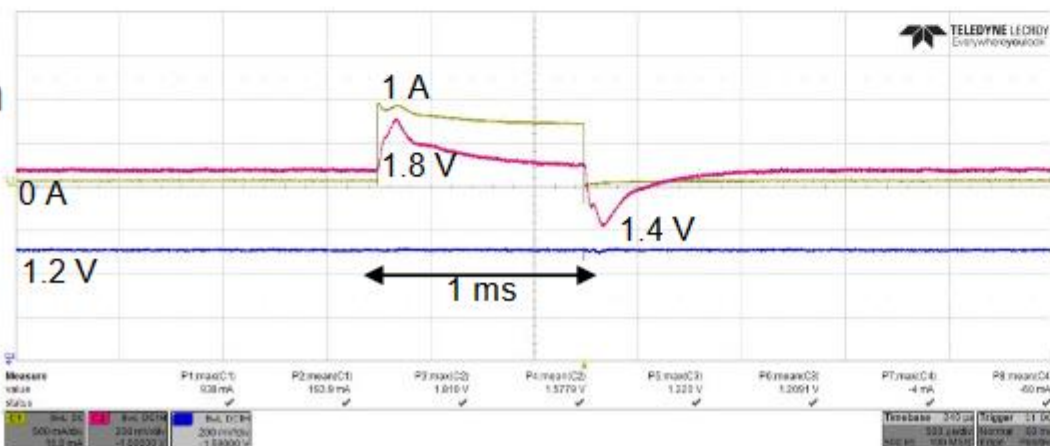
Upstream

- Iload
- Vin
- Vout



Downstream

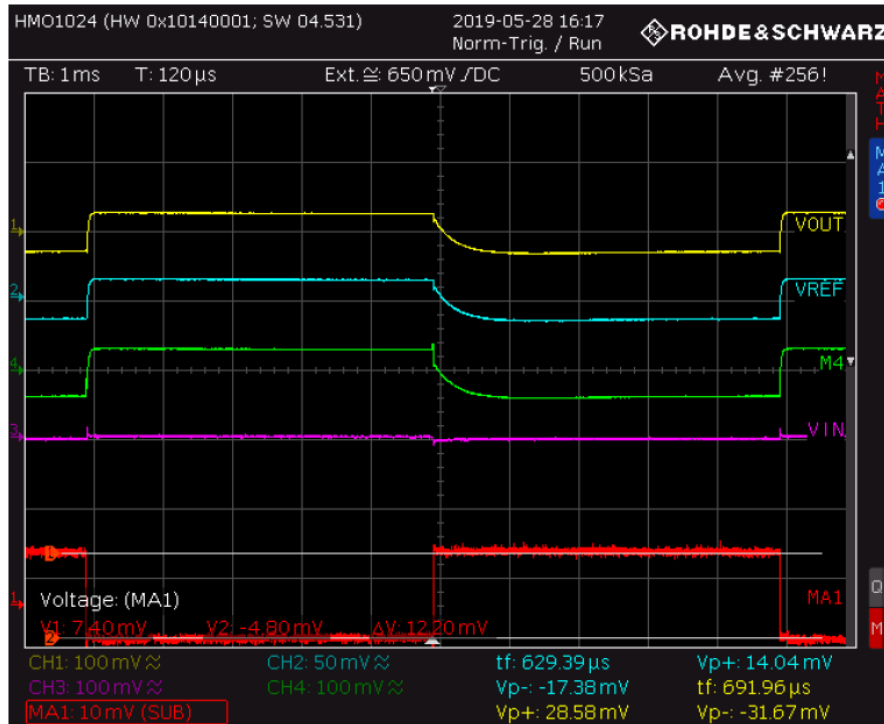
- Iload
- Vin
- Vout



➤ Overload protection decreases overload transients to propagate to other chips

Overload example with 5 ms overload

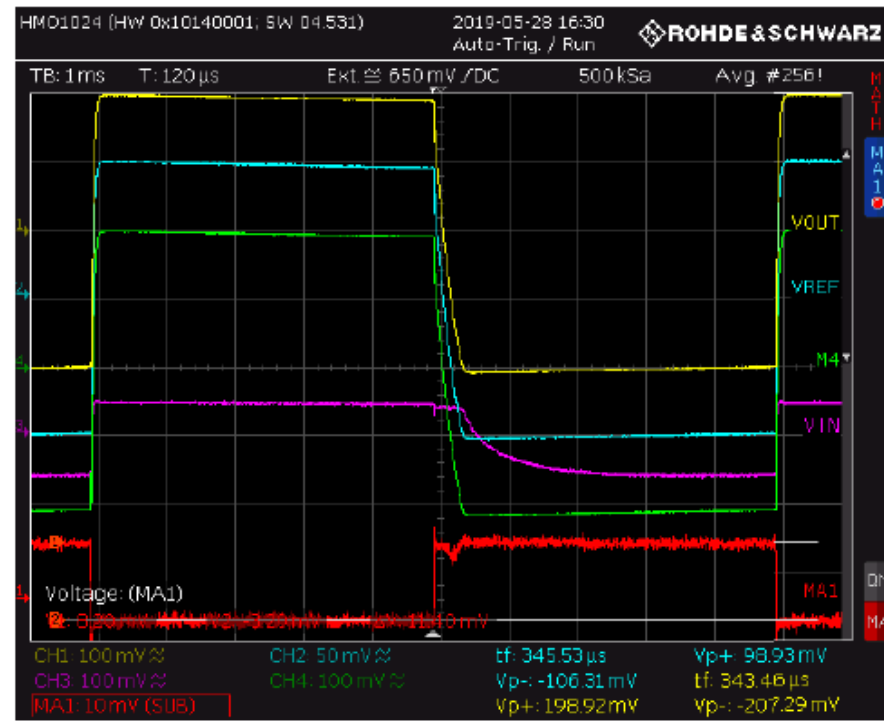
Overload caught by protection



VIN stays stable



Overload too big for protection



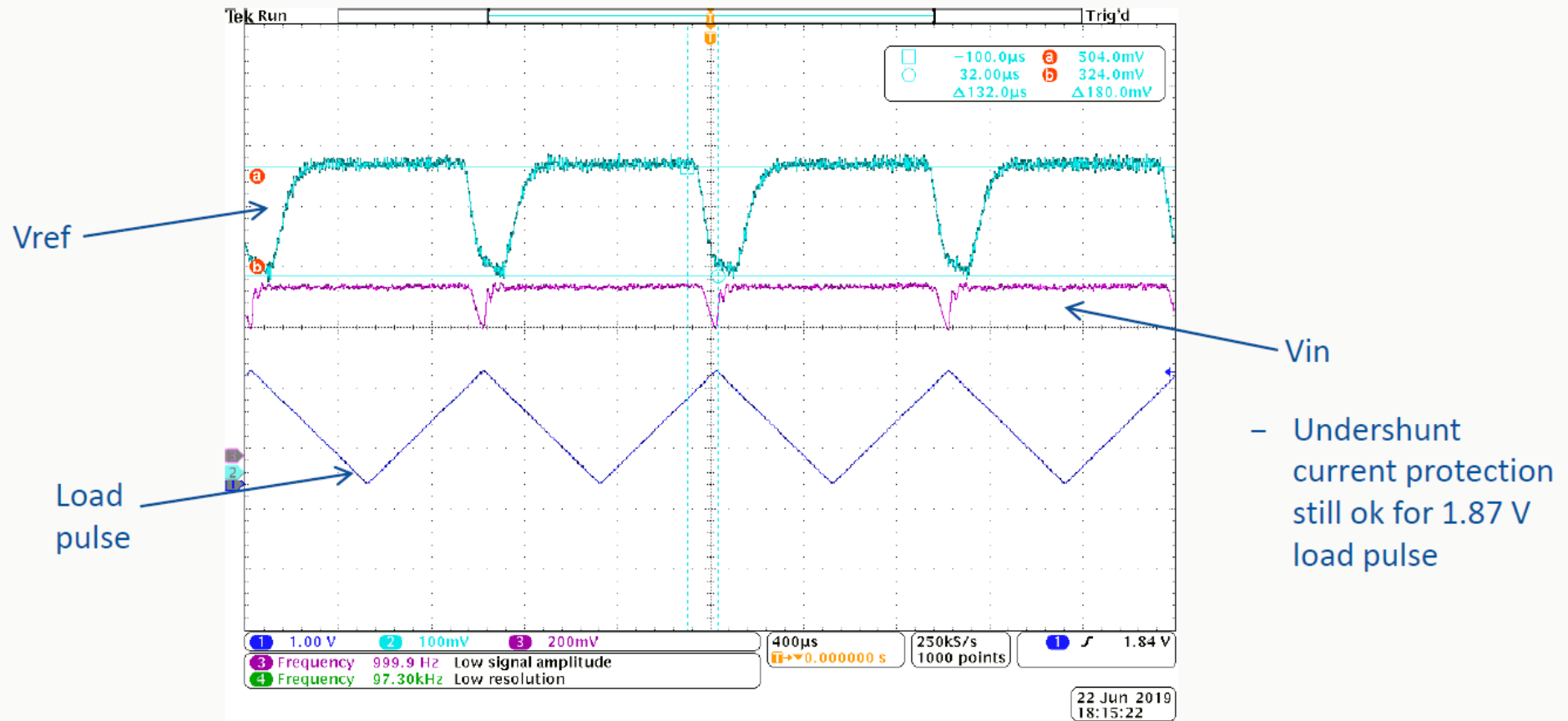
Transient on VIN



➤ Not all overload conditions are caught by under shunt protection

Undershoot protection after irradiation

700 MRAD



➤ Undershoot protection still working after 700 Mrad

Summary under shunt (overload) protection

- ❑ **Limits output voltage to a minimum of $\approx 0.7V$**
 - Reduces the transients propagated to VIN and other chips
- ❑ **Does catch only some overload conditions**
 - Does not catch e.g.: Shorts with $R_{LOAD} < 0.7V/I_{in} (\approx 1\Omega)$
- ❑ **Still functional after 700 Mrad**
 - Maybe some shift in the threshold current when it gets activated
- ❑ **Reduces slightly (1-2%) the available headroom**
 - Neglectable, unless very power efficient operation required

Overvoltage protection

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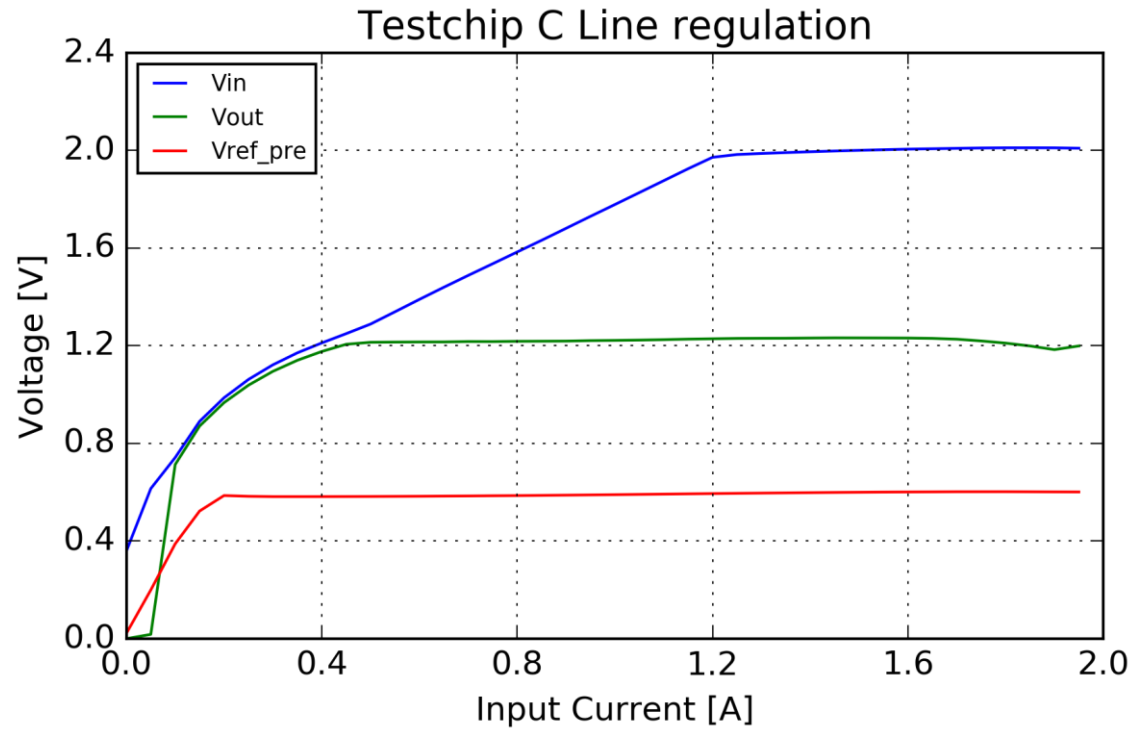
- Start up in RD53A
- Measurements with start up circuitry

❑ Low power mode

- With external signal (RD53B)
- With internal signal (not in RD53B)

Overvoltage protection testchip C – Line regulation

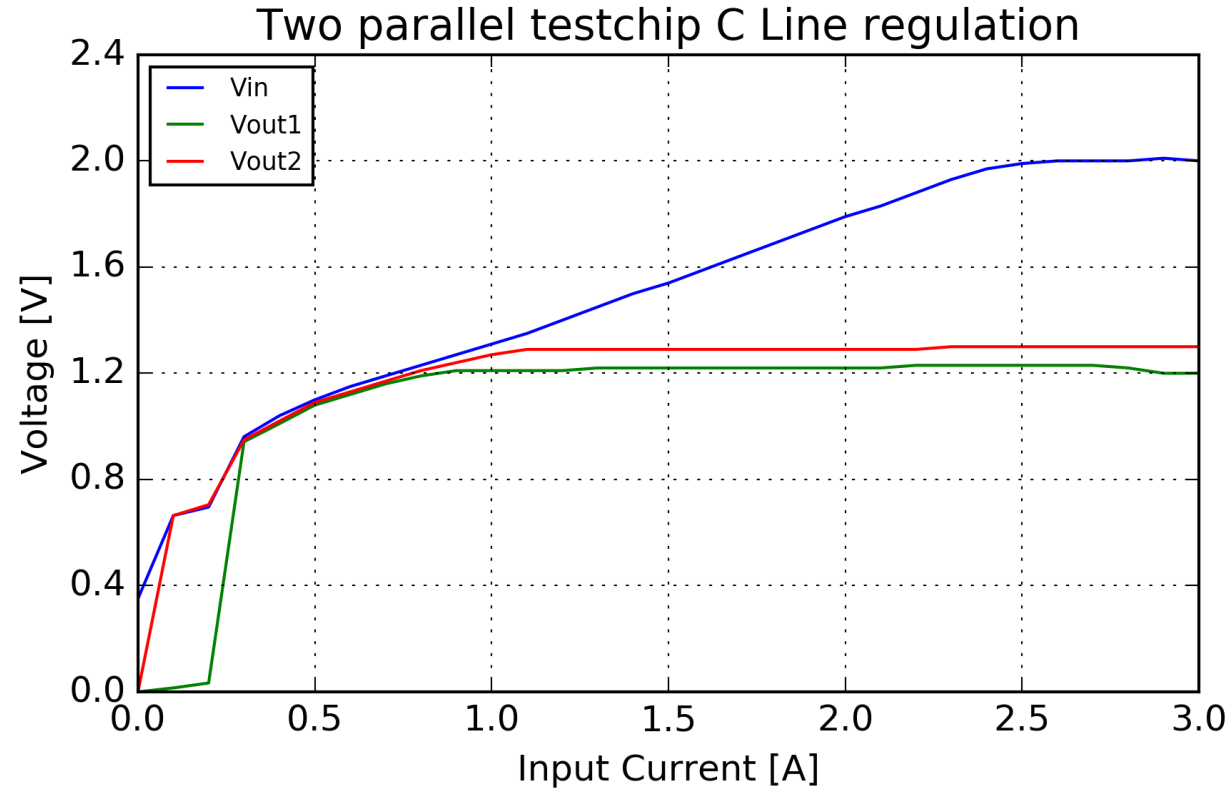
- Vofs = 0.85V
- Startup enabled
- OVP on
- Vref_ovp = Vref_pre



- Early start up (warm, unirradiated)
- OVP limits close to 2.0V ($\approx 3.3 * 0.6$ V)
 - Increased bandgap voltage in test chip C (like in RD53B)

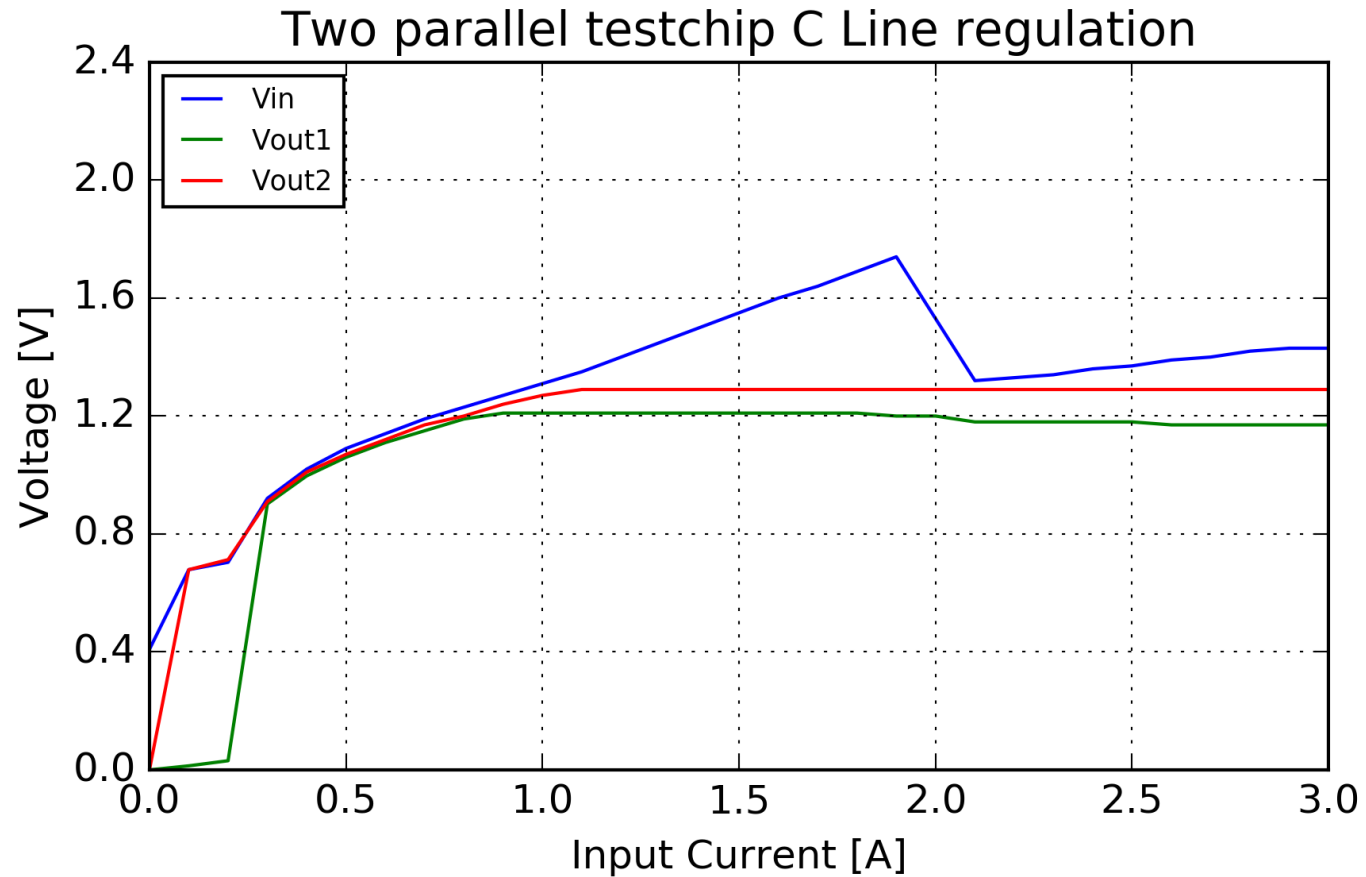
Overvoltage protection testchip C – Line regulation

- $V_{ofs} = 0.85V$
- Startup enabled
- OVP on
- $V_{ref_ovp} = V_{ref_pre}$



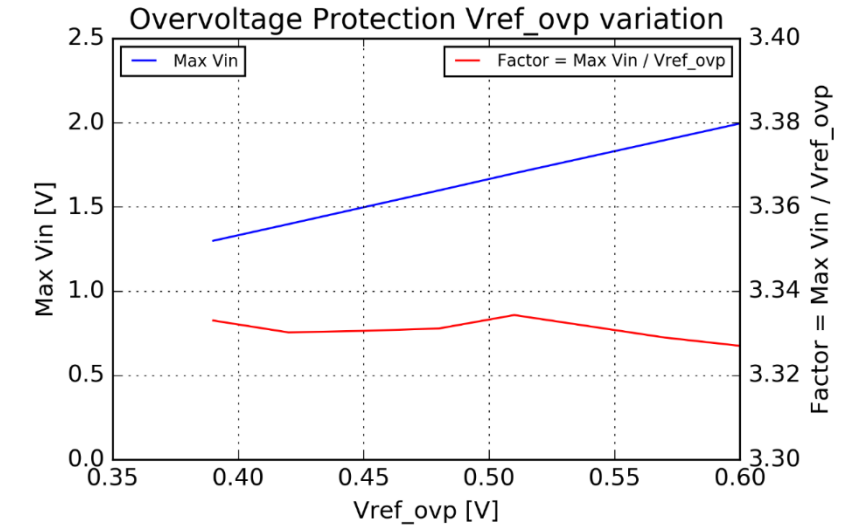
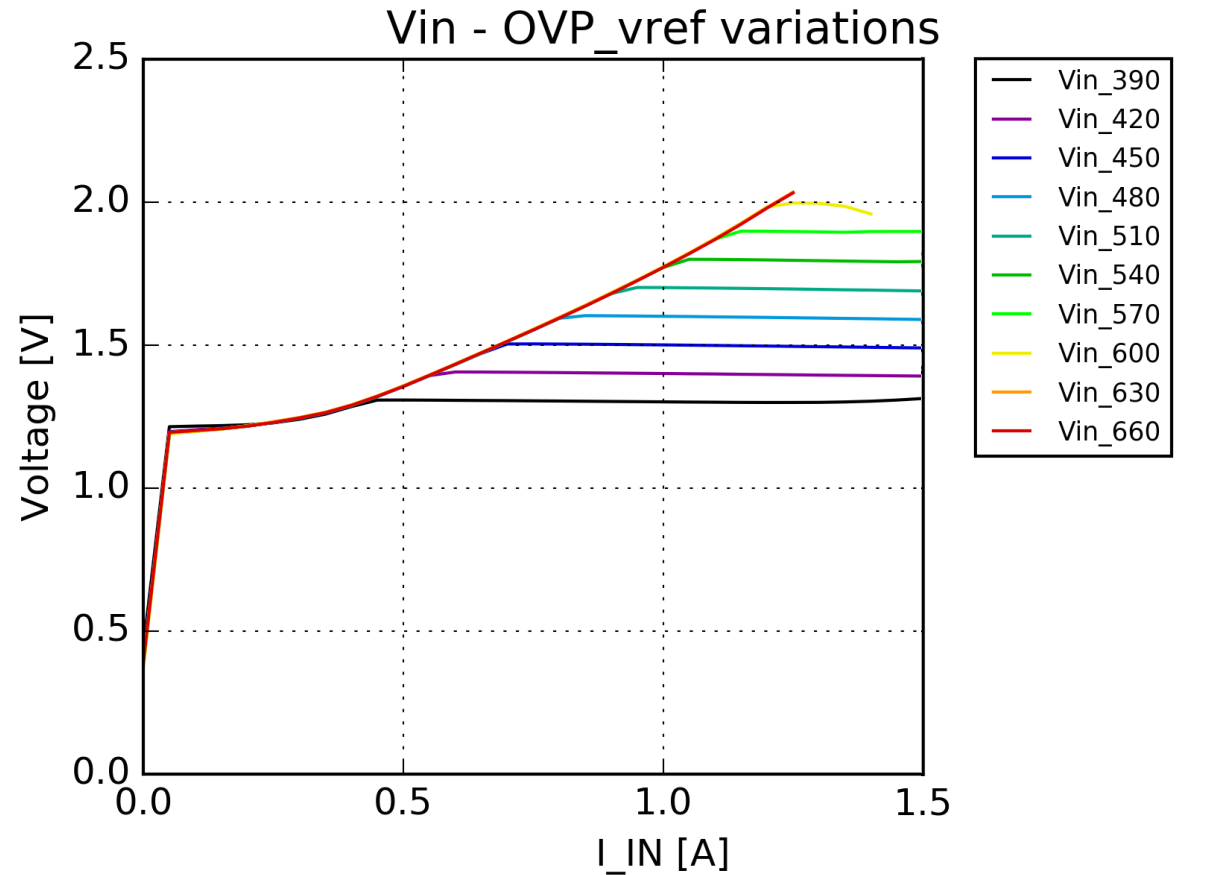
- Similar behavior for two testchips C in parallel
- When OVP gets active non linear behavior
 - Extra current over 2.5 A is not shared equally

OVP Failure case: Floating Vref_ovp



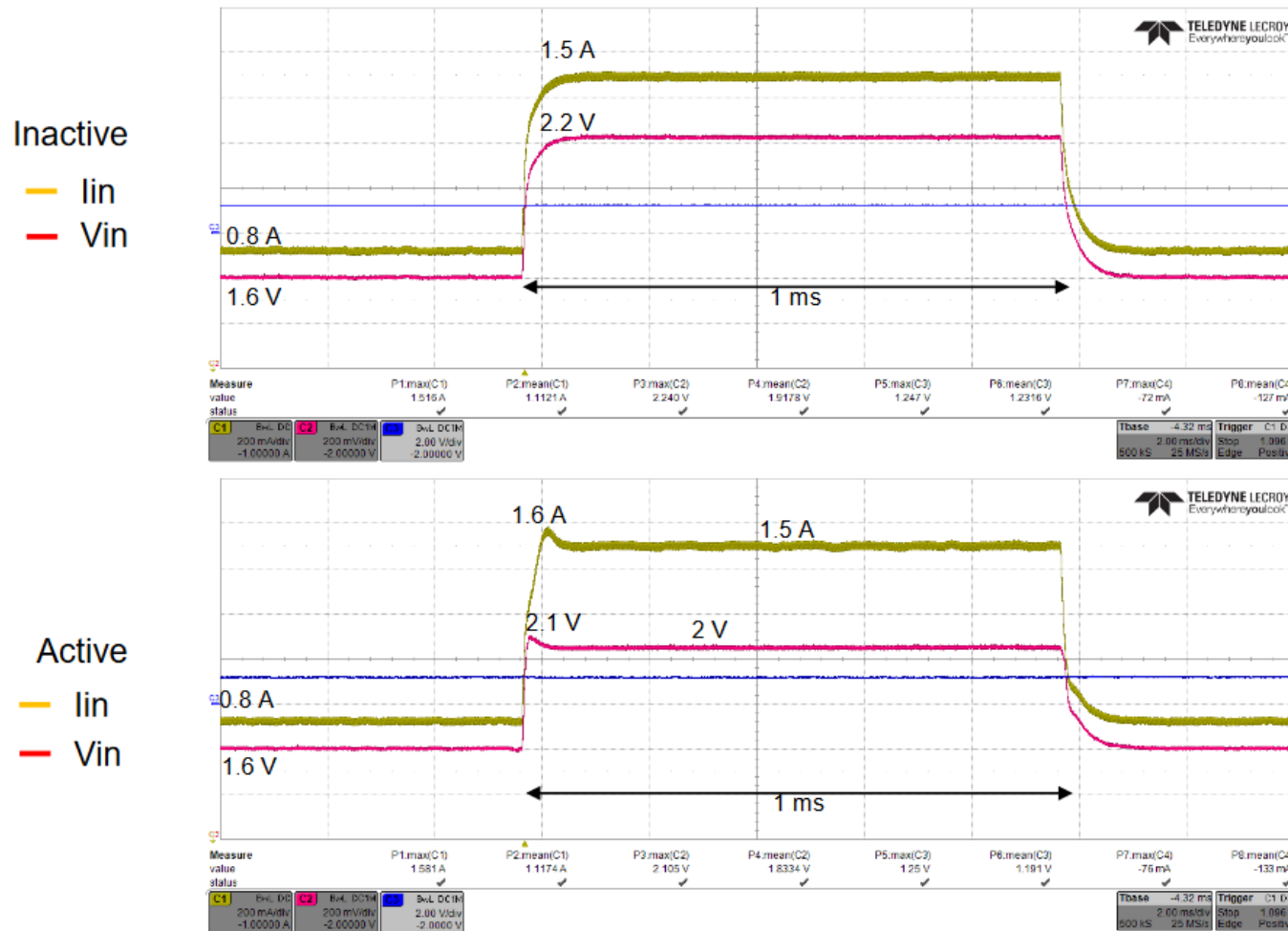
- Overvoltage protection with floating reference creates unstable Vin

Overvoltage protection testchip B – Different maximum voltages



- Tested with different configured maximum voltages
 - Limiting Voltage = **3.33** * Vref_ovp
- Overvoltage protection limits the maximum voltage very well
- **Variations in reference Voltage propagate proportionally to maximum voltage**

Overvoltage protection dynamic behavior



Umberto Molinatti

- Overvoltage protection limits maximum Vin
- Small overshoot before reaching stable maximum voltage
- Correct recovery when overvoltage condition is removed

Summary overvoltage protection

❑ Limits voltage very well

- Very accurate maximum ($3.33 * Vref_ovp$)
- Dynamic behavior also good

❑ Reference voltage $Vref_ovp$

- Per default connected to $Vref_pre$
 - Coarse and not trimmable
 - With increased bandgap voltage close to 2.0 V

❑ Only one way to disable:

- Connect $Vref_ovp$ to high reference voltage
 - In tests used $Vpre$ (~1.1V)
 - Use VIN instead? Is VIN (up to 2V) too high?

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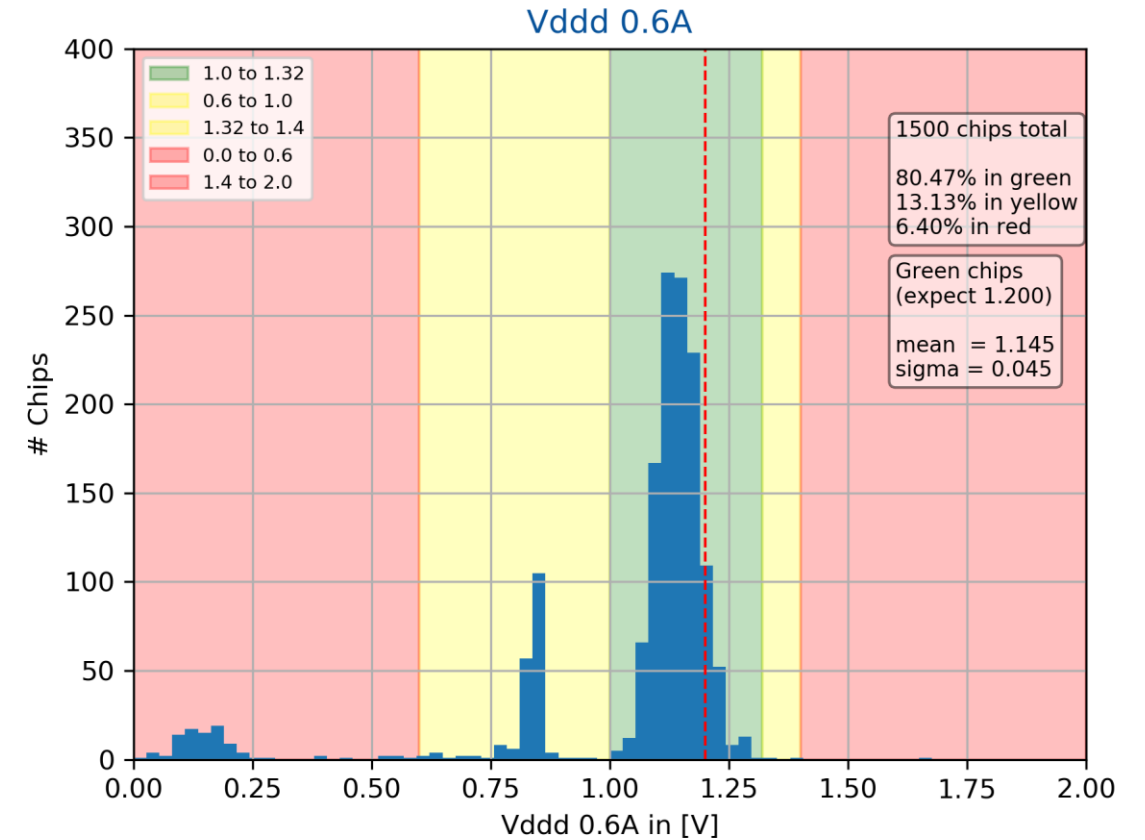
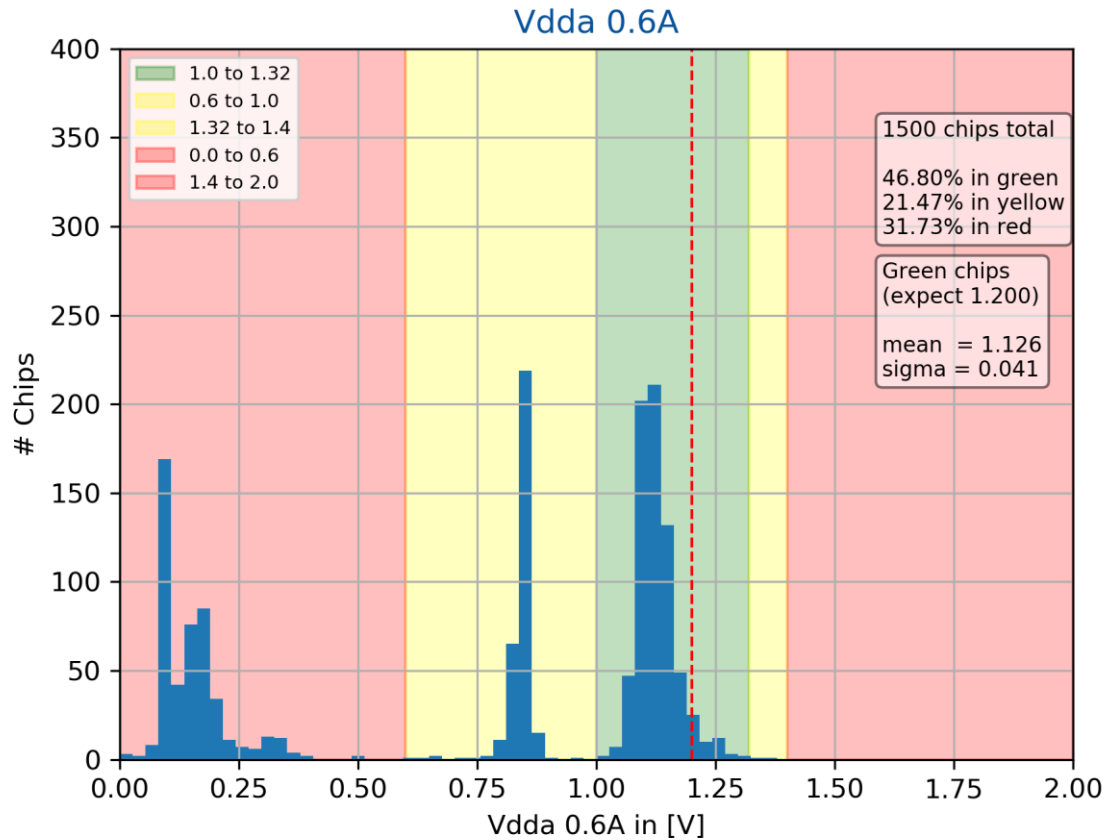
❑ Start up

- Start up in RD53A
- Measurements with start up circuitry

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- With external signal (RD53B)
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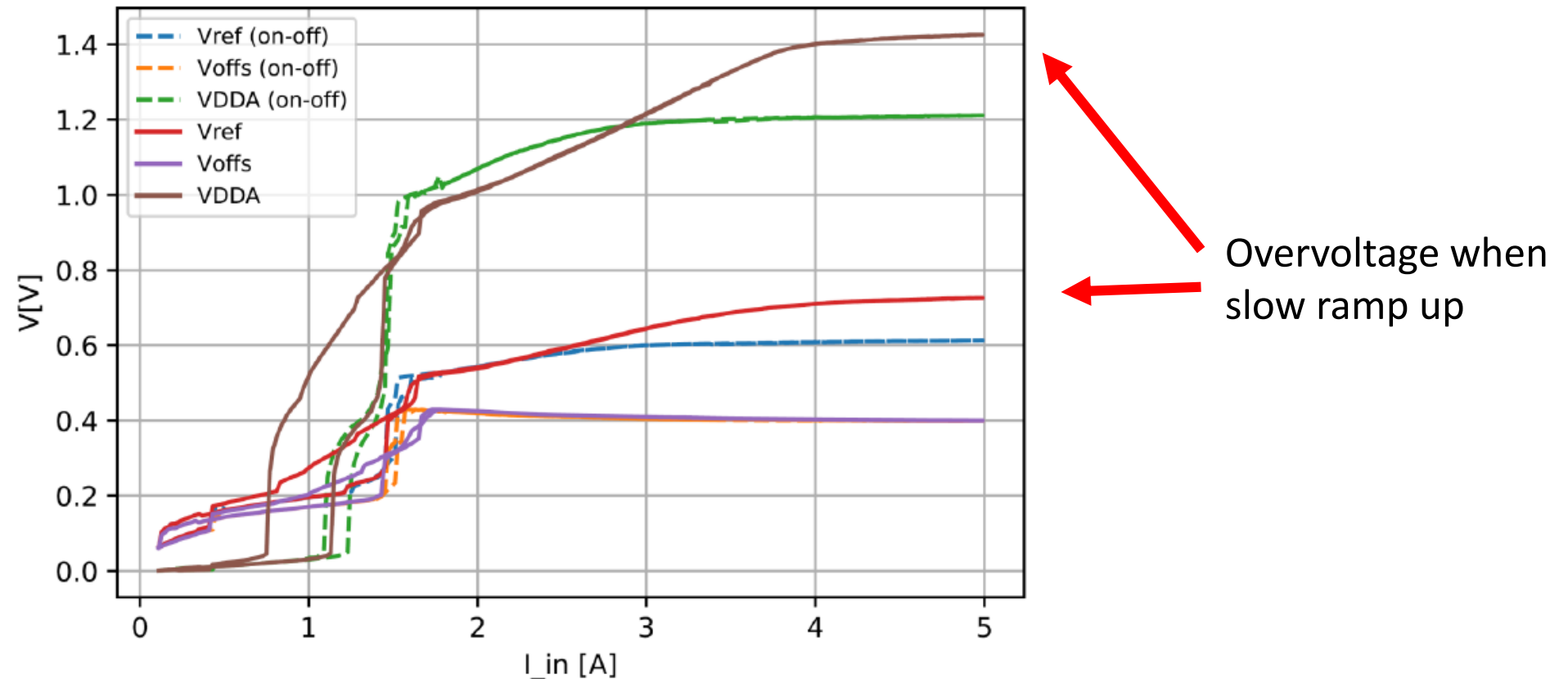
Wafer probing: VDD measurements at $I_{lin} = 0.6A$ (fast power up)



➤ Noticed difference between Analog and Digital in wafer probing
=> Analog started up later than digital (33% less green chips)

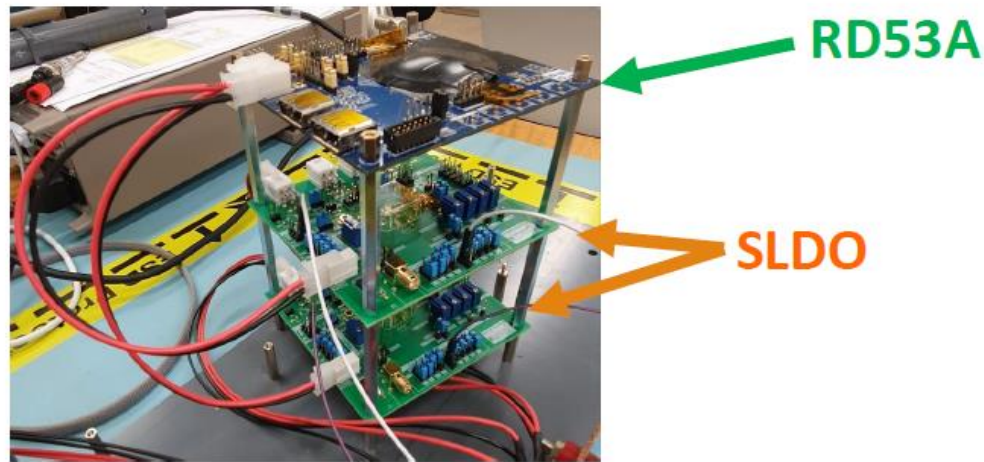
Quad modules: Different behavior of Vref depending on ramp up

- ❑ Only seen on **two (out of 20), unprobed** RD53A Quad modules (4 RD53A chips in parallel)



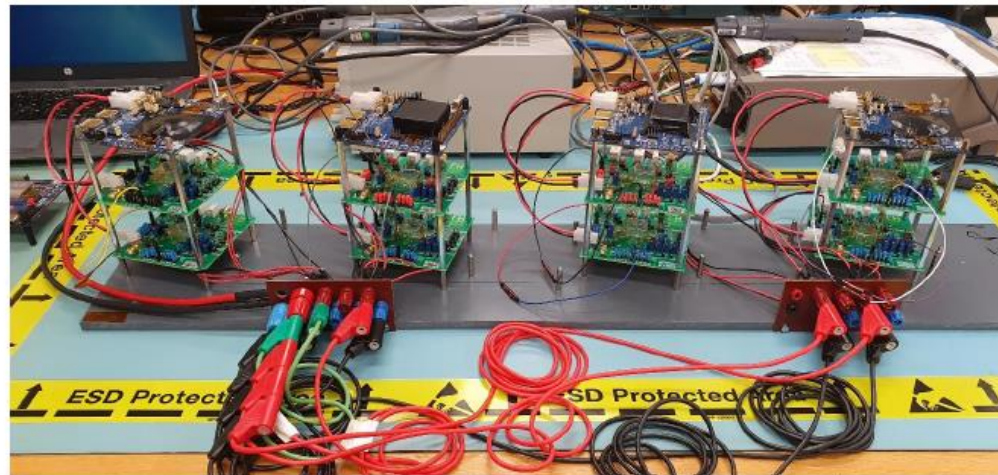
- ❑ With slow O(100s) ramp one Vref exceeded 0.7V causing overvoltage of VDD
- ❑ With fast O(<1s) ramp (on-off) normal behavior of Vref and VDD

Powering RD53As with SLDO testchips C



Setup

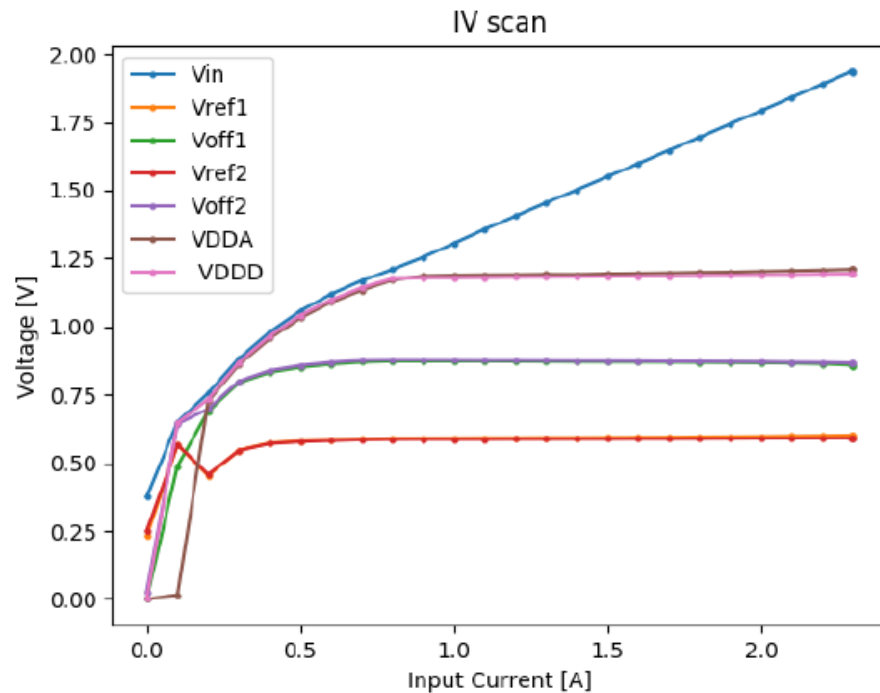
- RD53A SCCs powered in direct mode by two SLDO test Chip C
 - One each for Analog/Digital mode
- Standard bench PS (Tti PL303QMD-P)
- CAENels current source
<https://indico.cern.ch/event/848677/>
- KEITHLEY 2000 multimeter with scanner card
- TELEDYNE LECROY oscilloscope



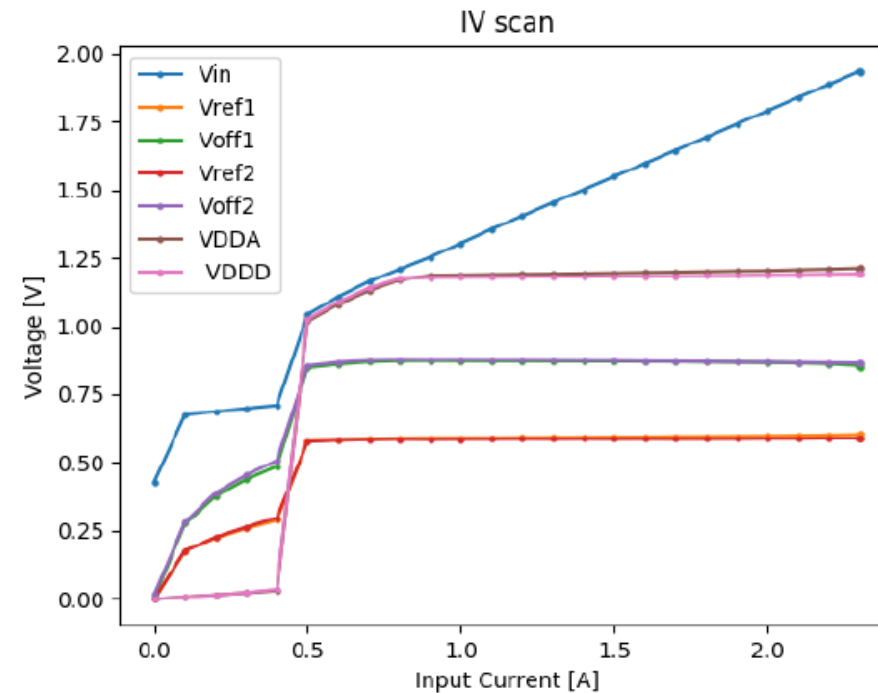
Start up of a RD53A powered by two SLDO test chips C

- ❑ Improved startup with start up circuit

STARTUP ON



STARTUP OFF



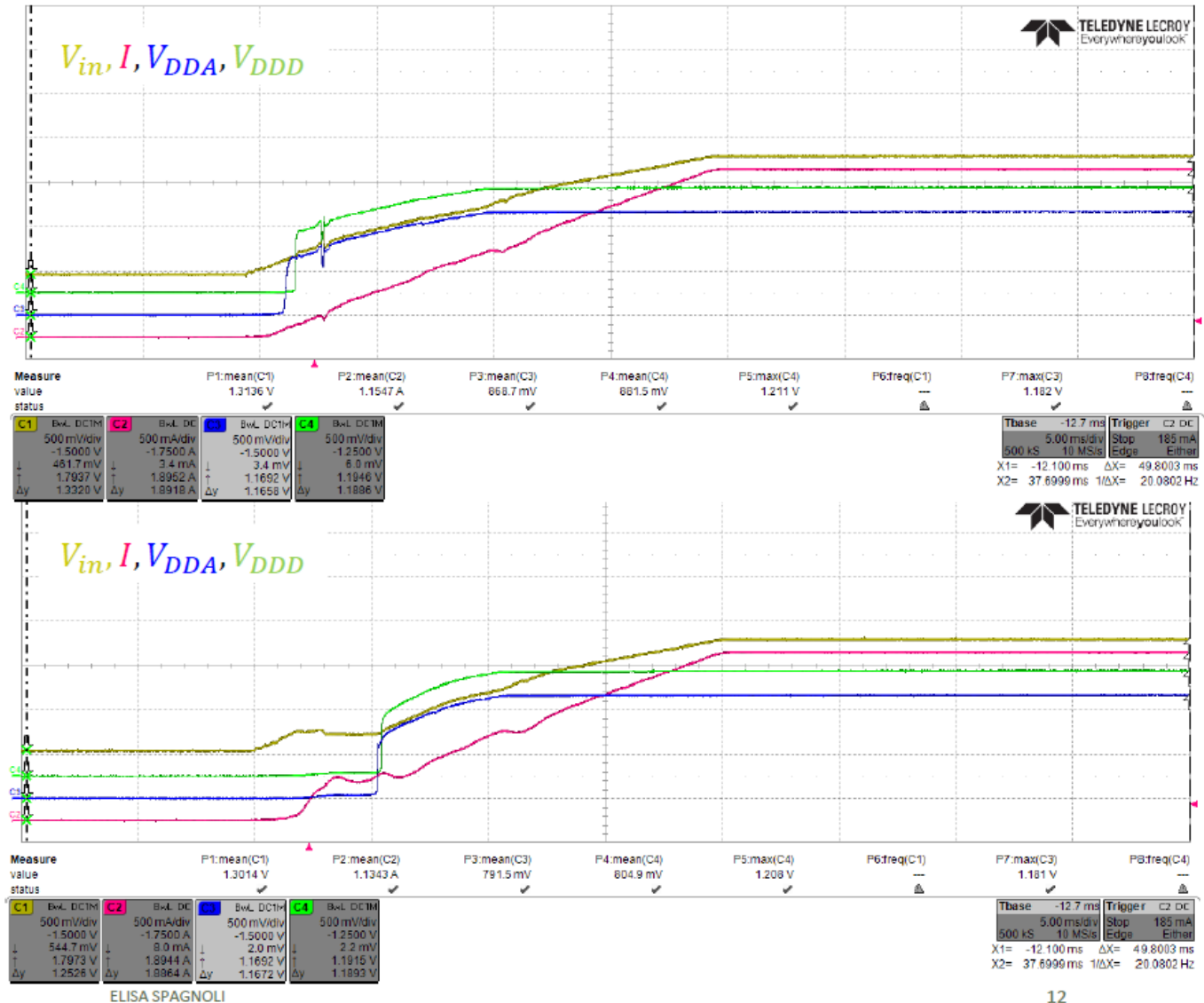
Start up of a RD53A powered by two SLDO test chips C

Startup on

Single Chip
100A/s ramp

Startup off

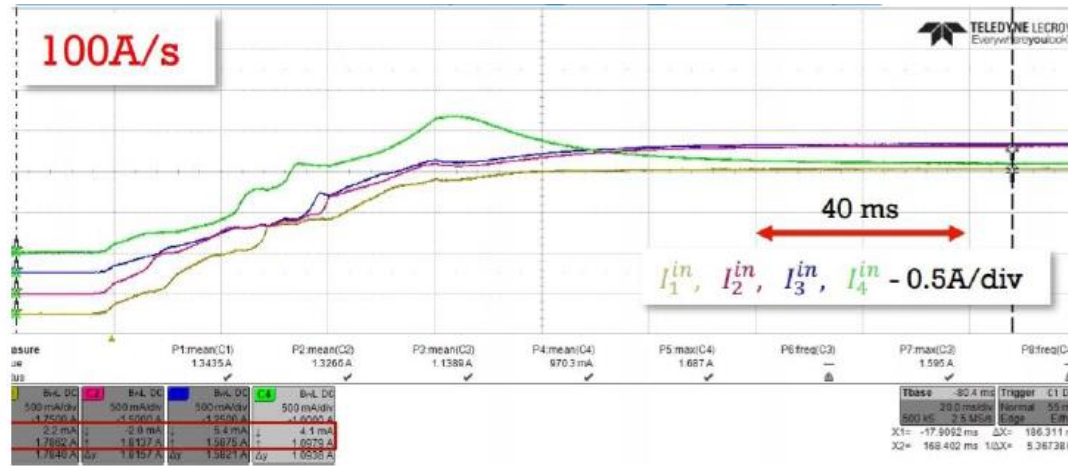
10/25/2019



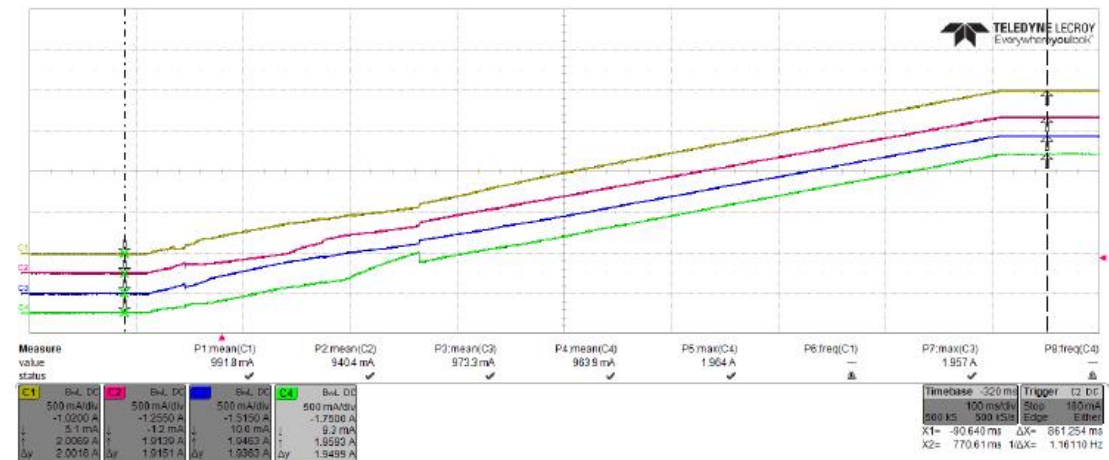
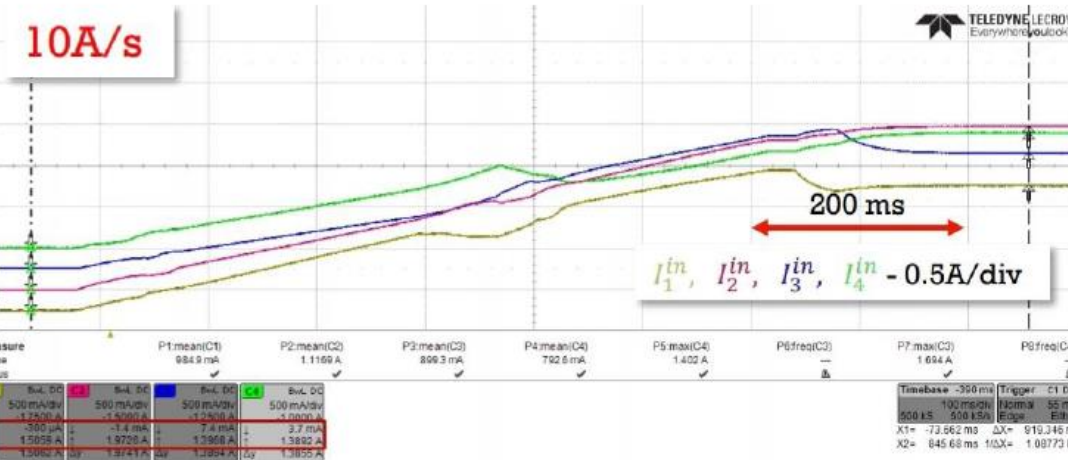
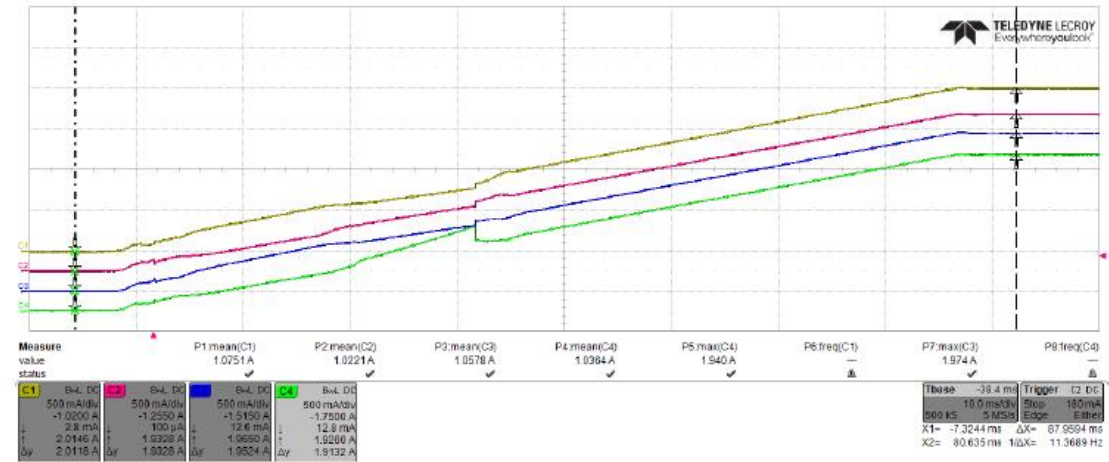
Start up of 8 SLDOs in parallel

- Current sharing is much smoother with start up circuit

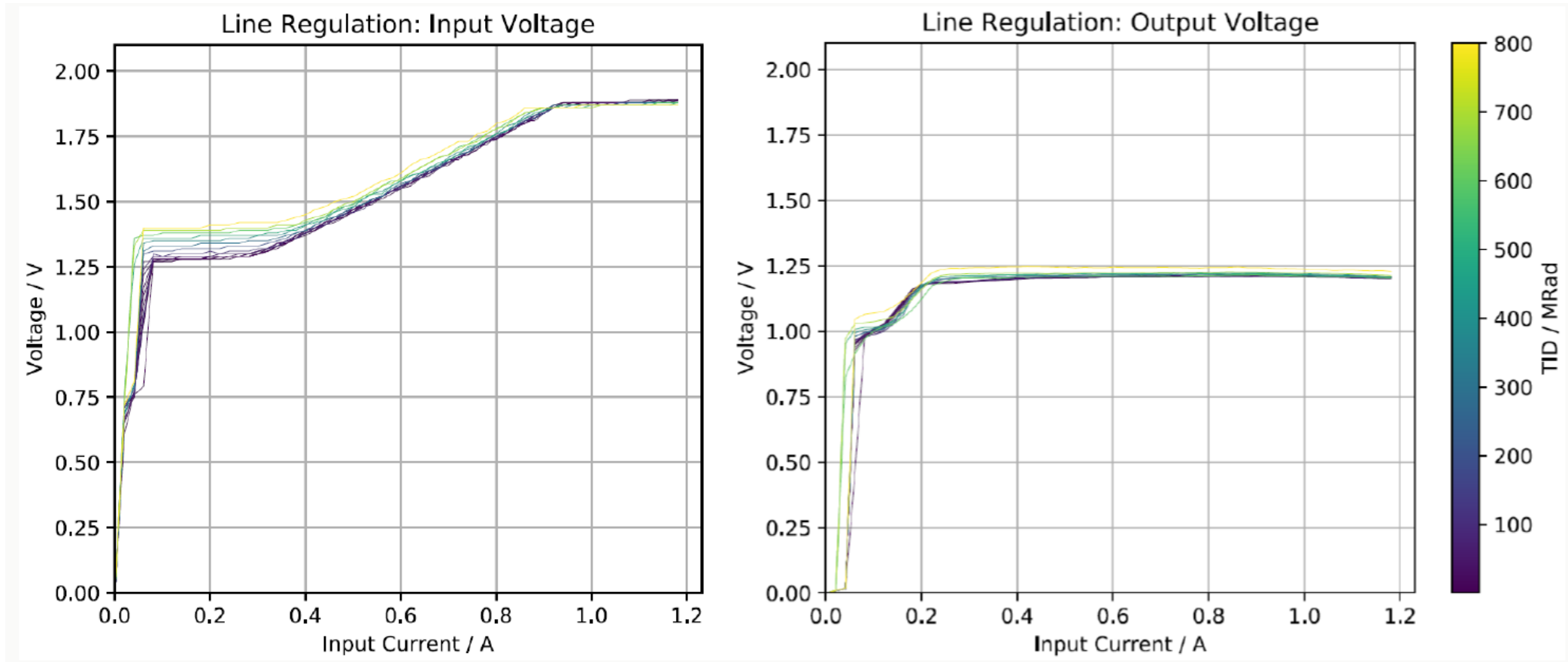
4 RD53A chips



4 RD53As powered by 8 test chip C



Testchip B Irradiation:



- ❑ Start up very good, even after irradiation (Reminder: Testchip A degraded significantly)

Summary start up

□ RD53A

- Wafer probing
 - Difference in startup between analog and digital observed
 - Low yield of chips with power efficient start up ($\approx I_{SLDO} < 0.6A$)
- RD53A quad modules
 - VDD overvoltage due to Vref on two unprobed chips with slow ramp up speed O(100s)

□ Improvements due to start up circuitry (testchip B+C)

- Significant improvement in start up
- Even after irradiation start up works well at -10C

Low power mode

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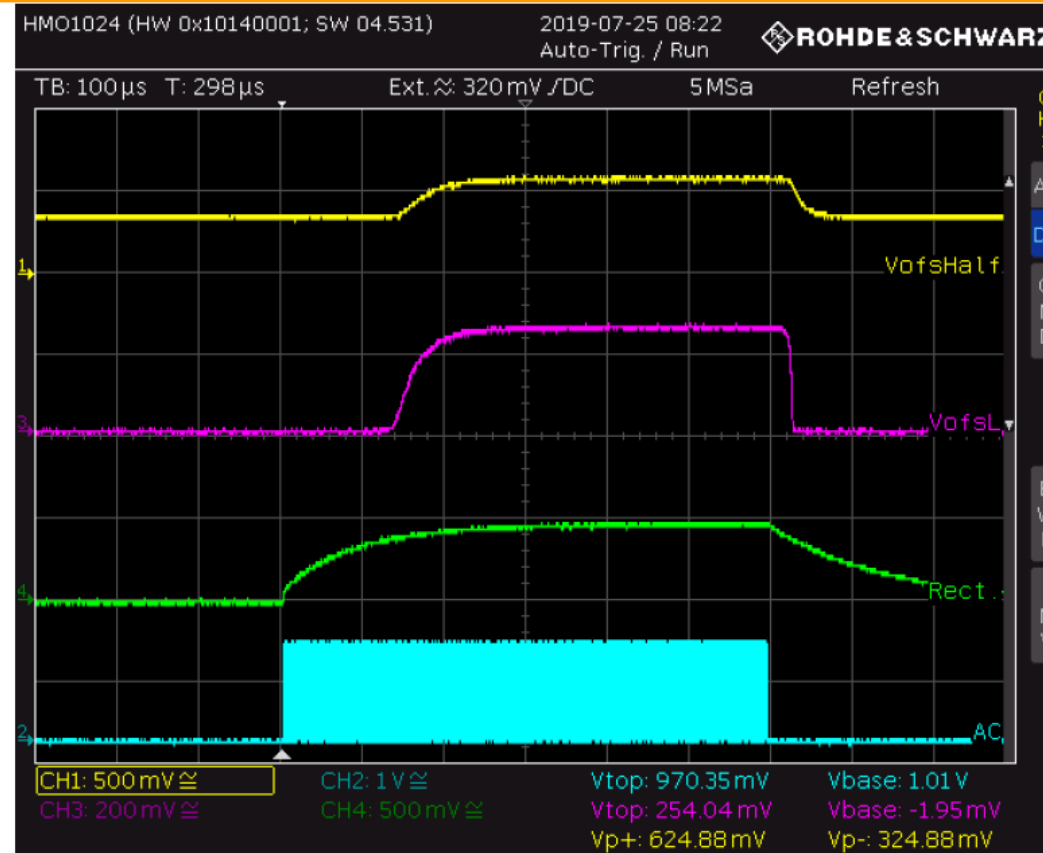
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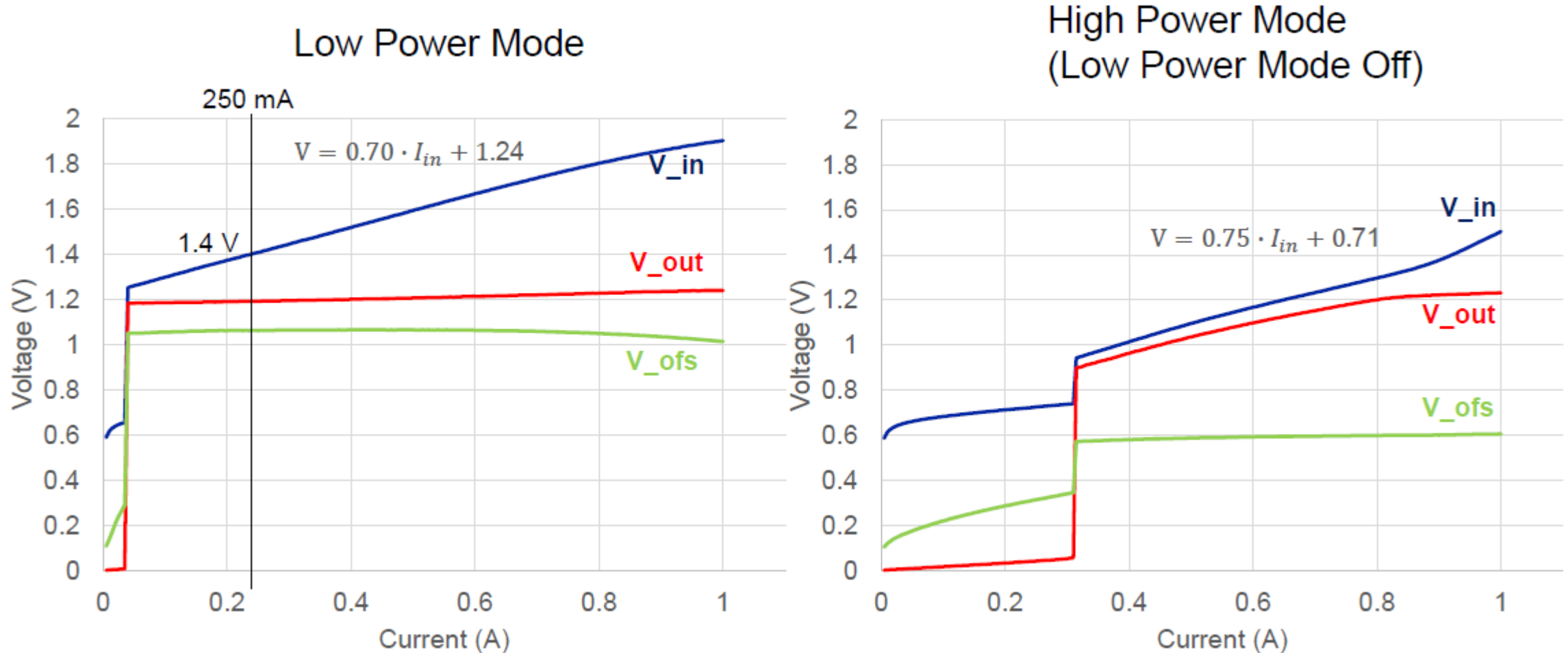
Low power mode with AC rectifier

Low Power Mode (AC-Rectifier)



- Applying the AC signal enables the additional offset resistor creating a higher Vofs

Low power mode with AC rectifier

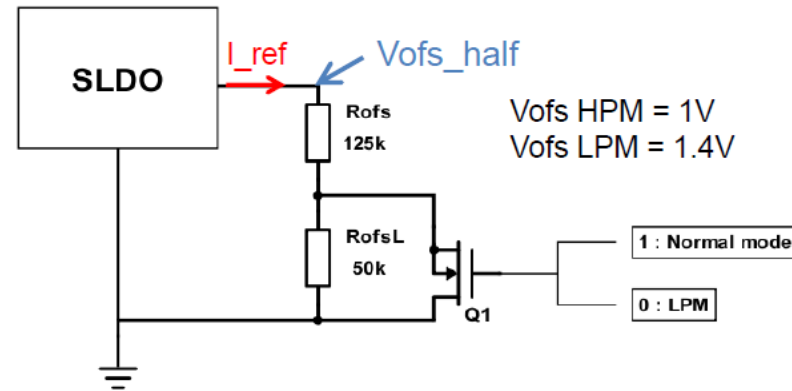


- With higher V_{ofs} the input voltage reaches 1.4 V with lower currents

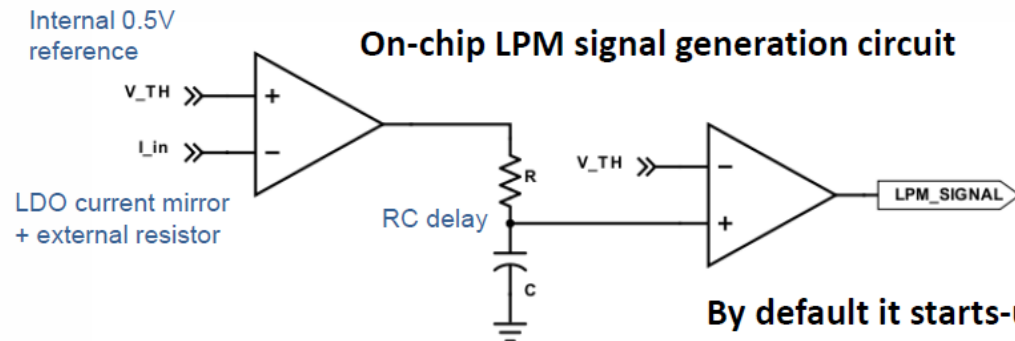
Internal Low power mode (not in RD53B)

1. Low power mode

LPM general scheme



On-chip LPM signal generation circuit



By default it starts-up in HPM, and after some time (delay) with low I_{lin} it changes to LPM

Summary low power mode

LPM with AC rectifier

- Seems to work well
- Requires external signal

LPM with internal enabling

- Works quite well on testchip B
- Some potential drawbacks
 - Threshold reference voltage is not very accurate
 - Some parallel chips may end up in high power mode
=> Common Vofs solves the problem

The LPM can be disabled by shorting the RofsL