

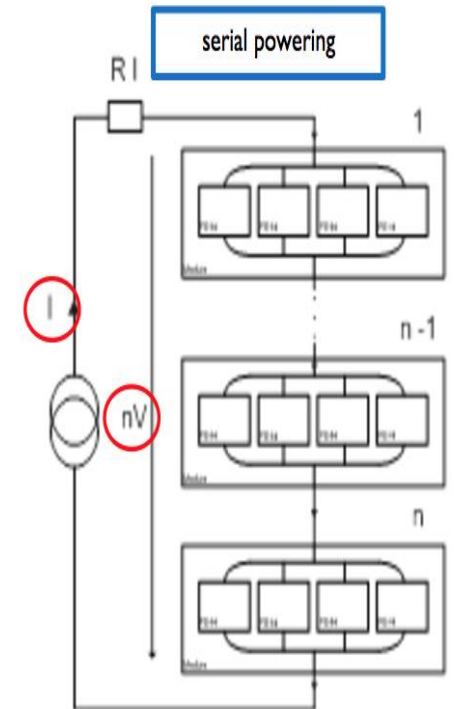
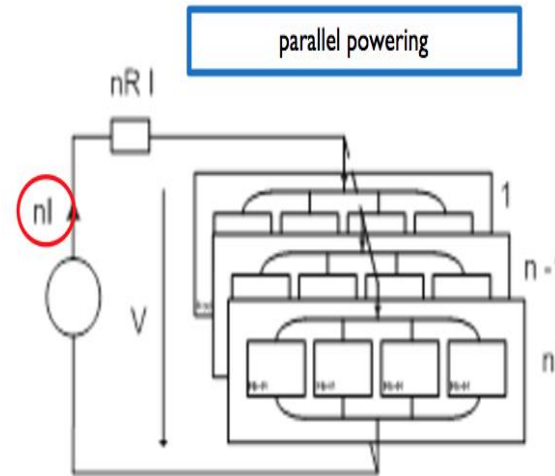


# Serial Powering Testing for Phase 2 Inner Tracker

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CMX coffee seminar 25/8/2017

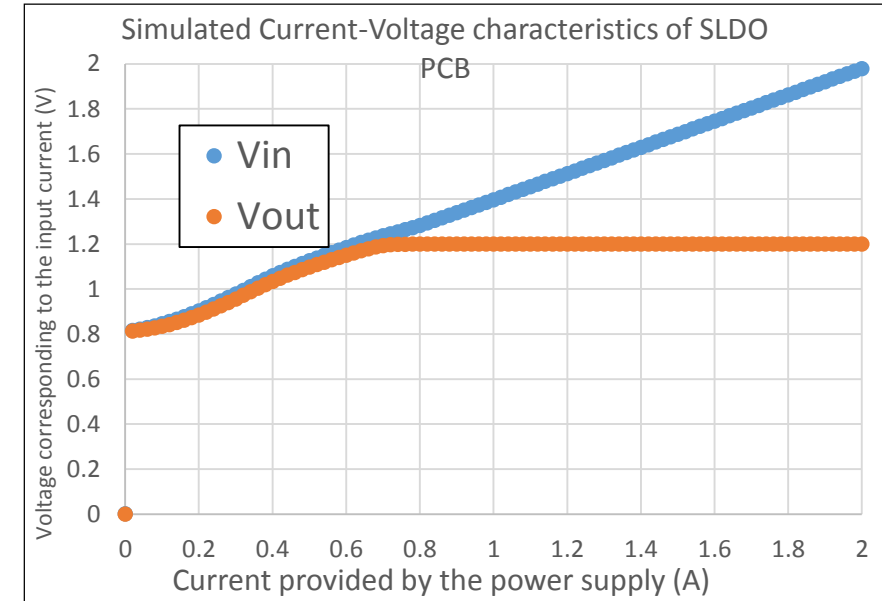
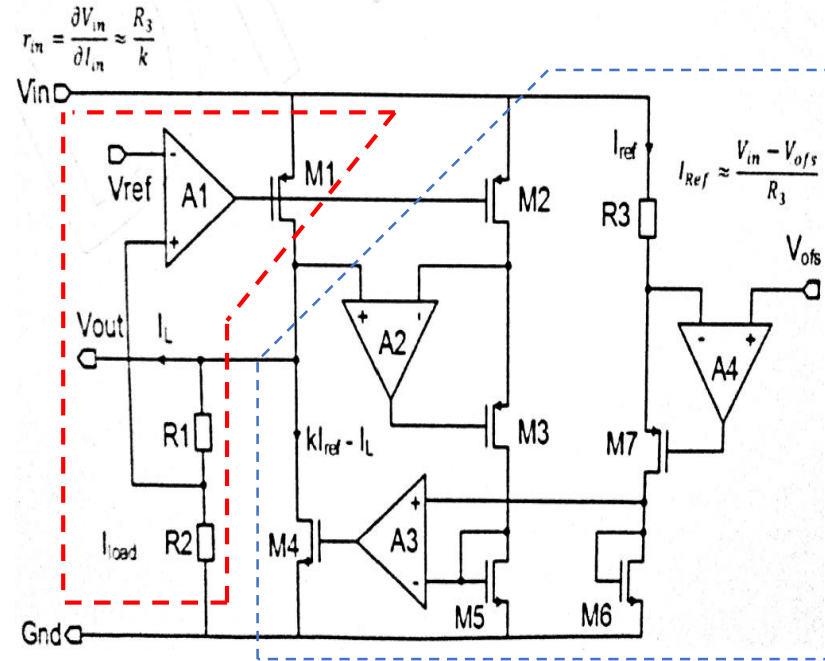
- Serial Powering Attractive (only viable solution for low mass)
  - ~1/3 material in power cables
  - ~1/3 power losses in cables
  - No remote DC/DC with associated mass and integration problems
  - On chip integrated solution (radiation hard)
  - Can Possibly be even more advantageous :
    - Higher voltage drop on local power cables can possibly be supported
    - Long distance power cabling not a problem
  - Major Worries : Noise Injection, Failure propagation, Grounding



# Shunt-LDO regulator

- Idea and design by M.Karagounis (Hochschule Hamm-Lippstadt)
- Voltage regulation loop (**LDO**) :  
Constant  $V_{out} = 2 * V_{ref}$
- Current Regulation loop (**shunt**) :  
keeps current through the regulator constant
- Ohmic input characteristics :

$$R_{in} \approx \frac{V_{in}}{I_{in}} \approx \frac{R_3}{k}$$



$$V_{out} = 2 * V_{ref}$$

$$V_{in} \approx V_{offset} + I_{in} * R_3$$

# RD53A Shunt-LDO

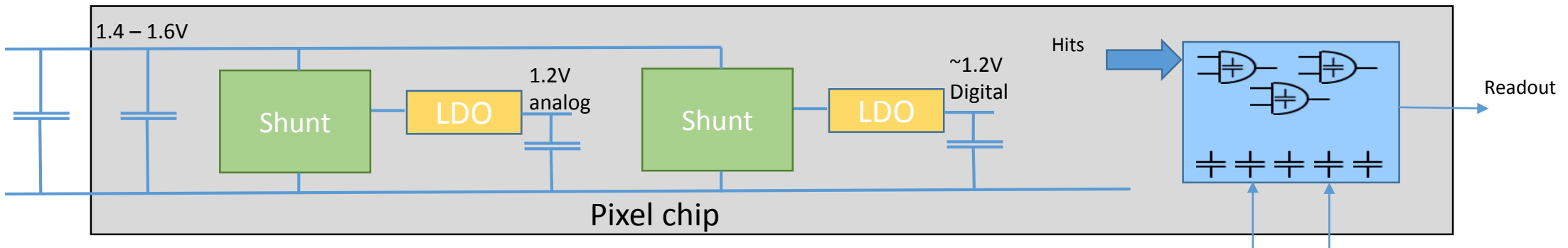
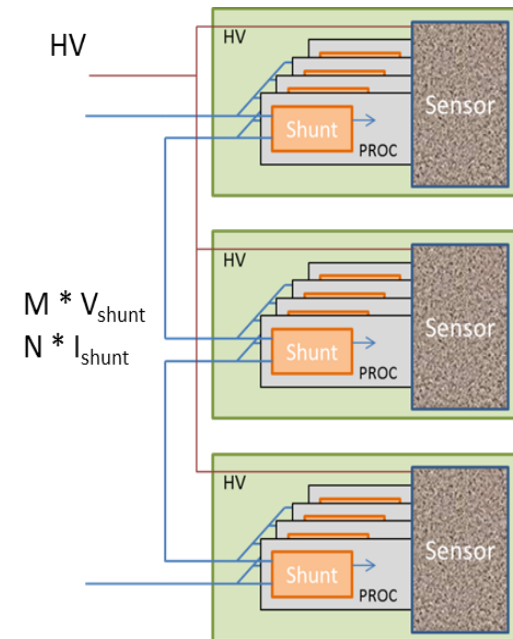
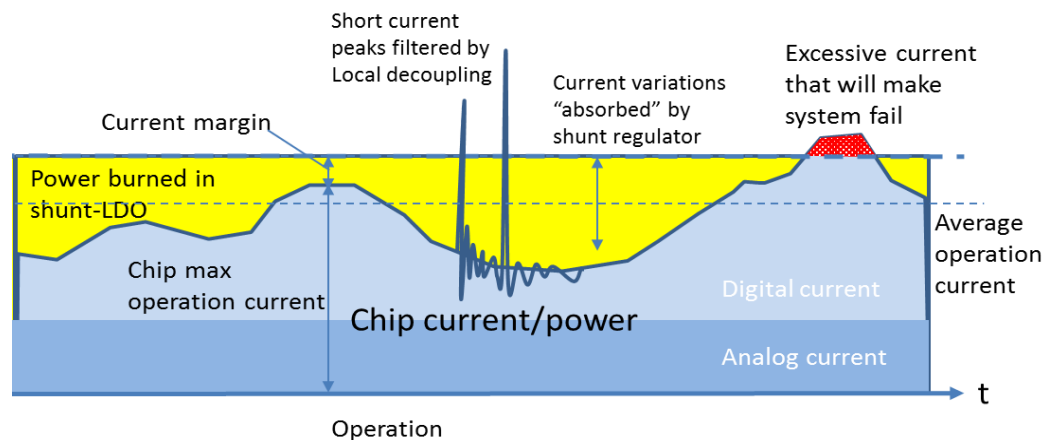
- Serial powering set-up: A constant current power supply generates a current  $I$ : This current is fed in a chain of modules. Each chip is equipped with regulators to generate the supply voltages.

- Nominal operation average IC current:  $2 \times 0.8A$  (analog and digital) @  $1.2v/1.2v$

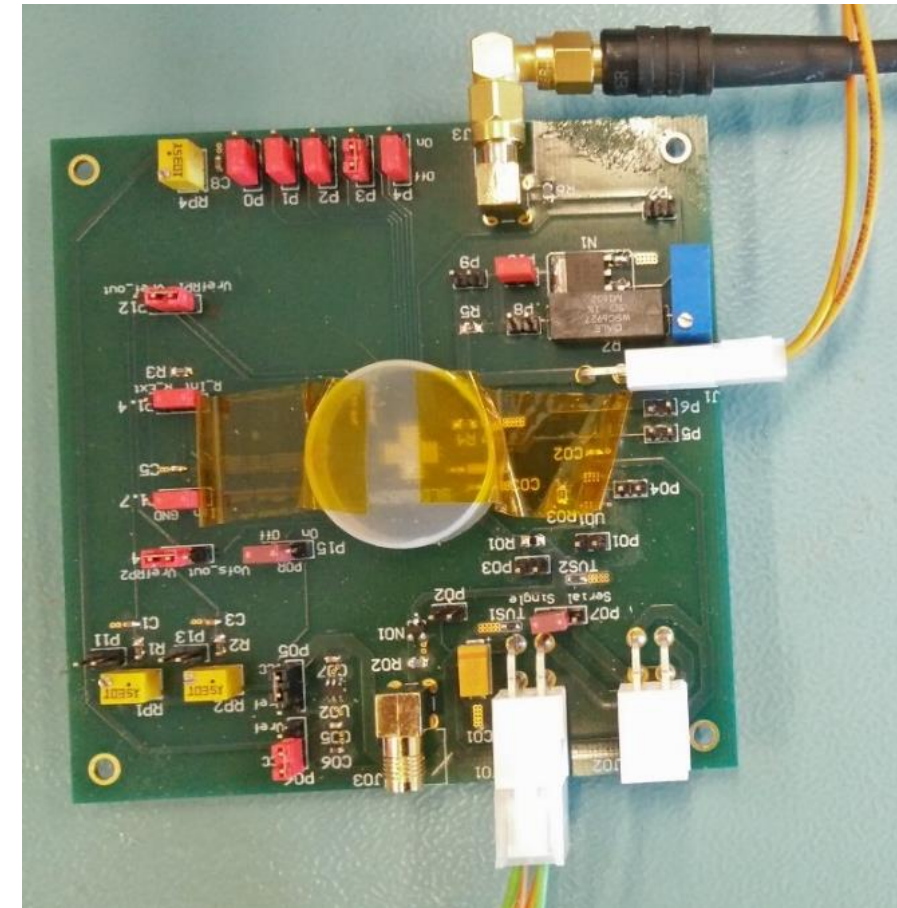
Nominal shunt current:  $\sim 25\%$

- Total current  $\sim 2 \times 1A$
- Note: This is what allows serial power to run with constant currents despite load variation

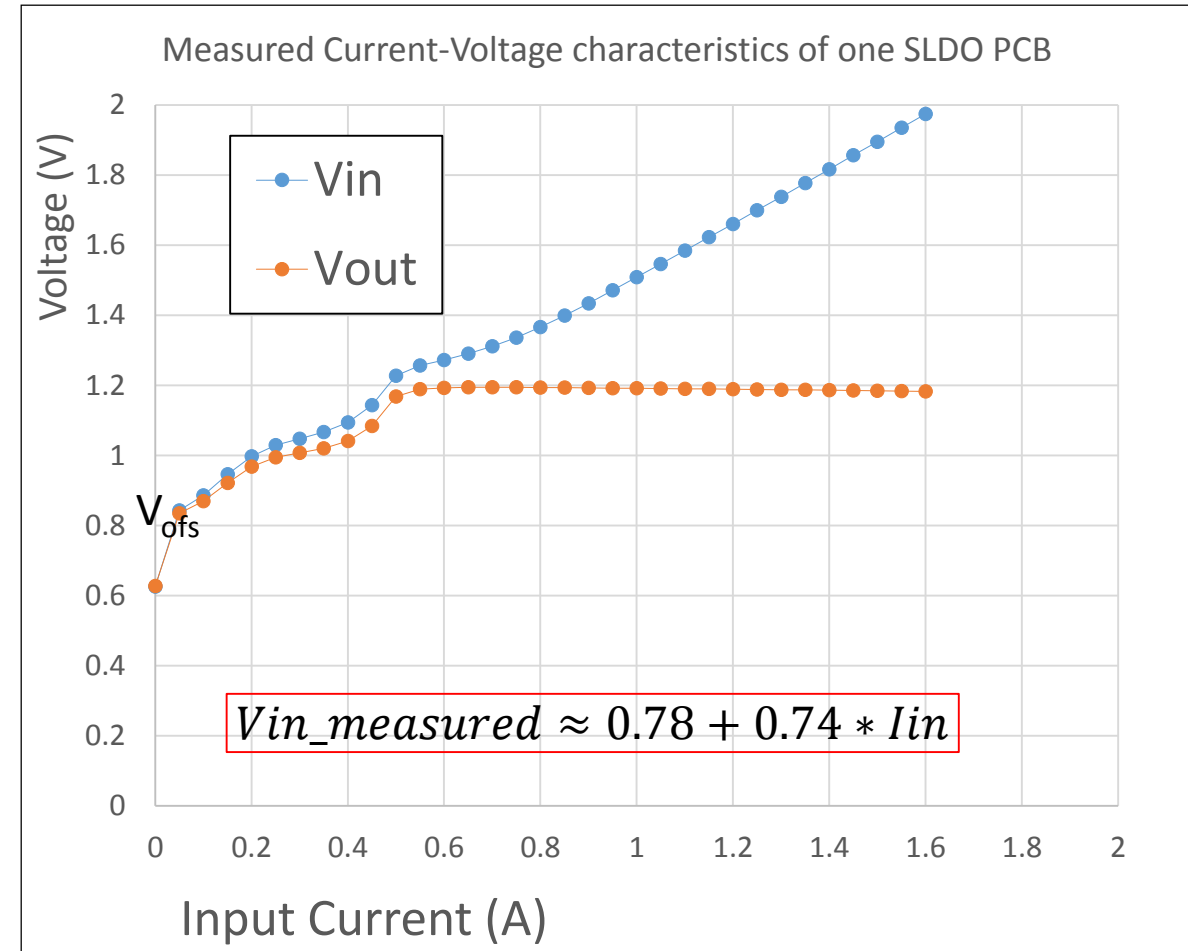
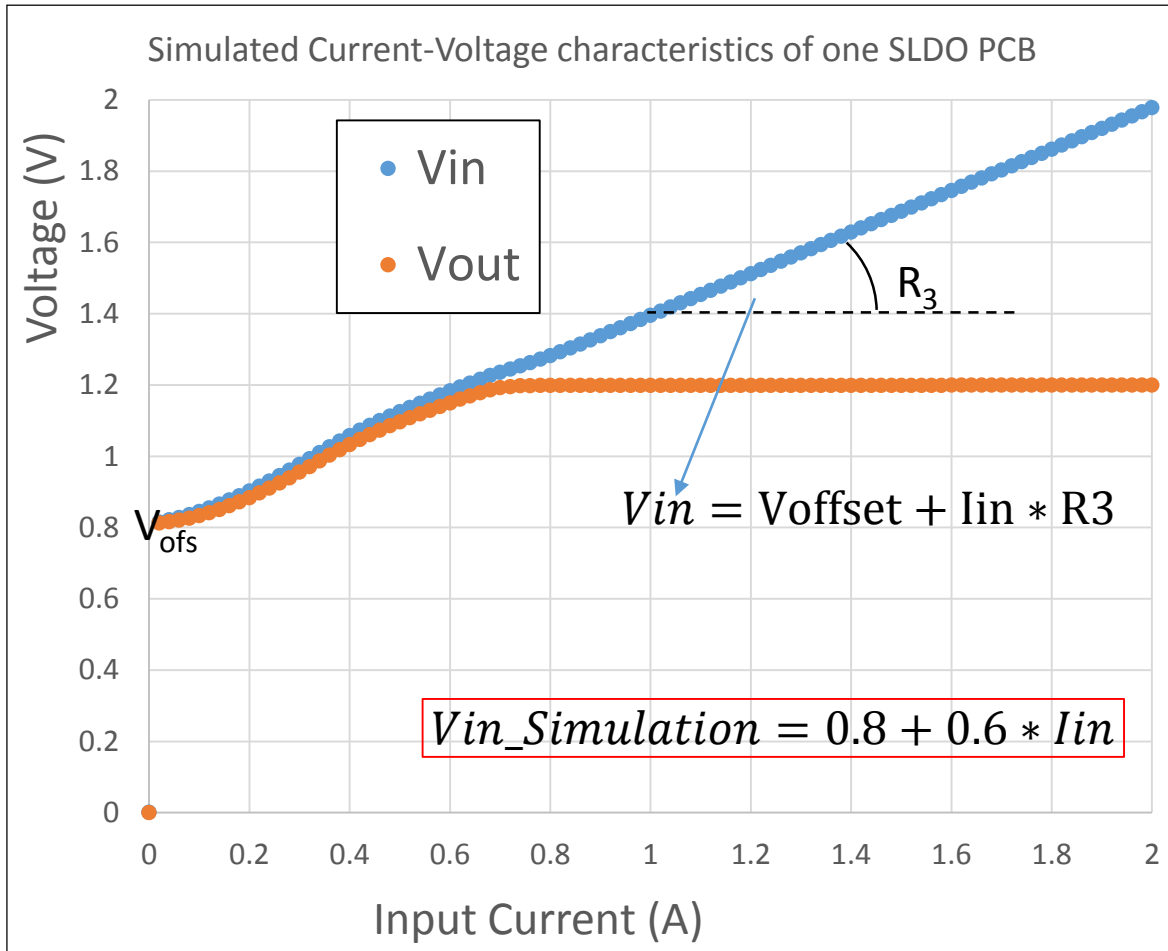
- Each RD53A chip has 2 shuntLDO (one for analog, one for digital). The shuntLDO is an IP block of the RD53A chip itself. Each shuntLDO is design for 2A to allow safe operation also during failures.



1. Single ShuntLDO 2A test chip behavior
2. Transient tests with 2 PCBs in series
3. Parallel VS Serial tests
4. Failure Scenarios (open, short)
5. References



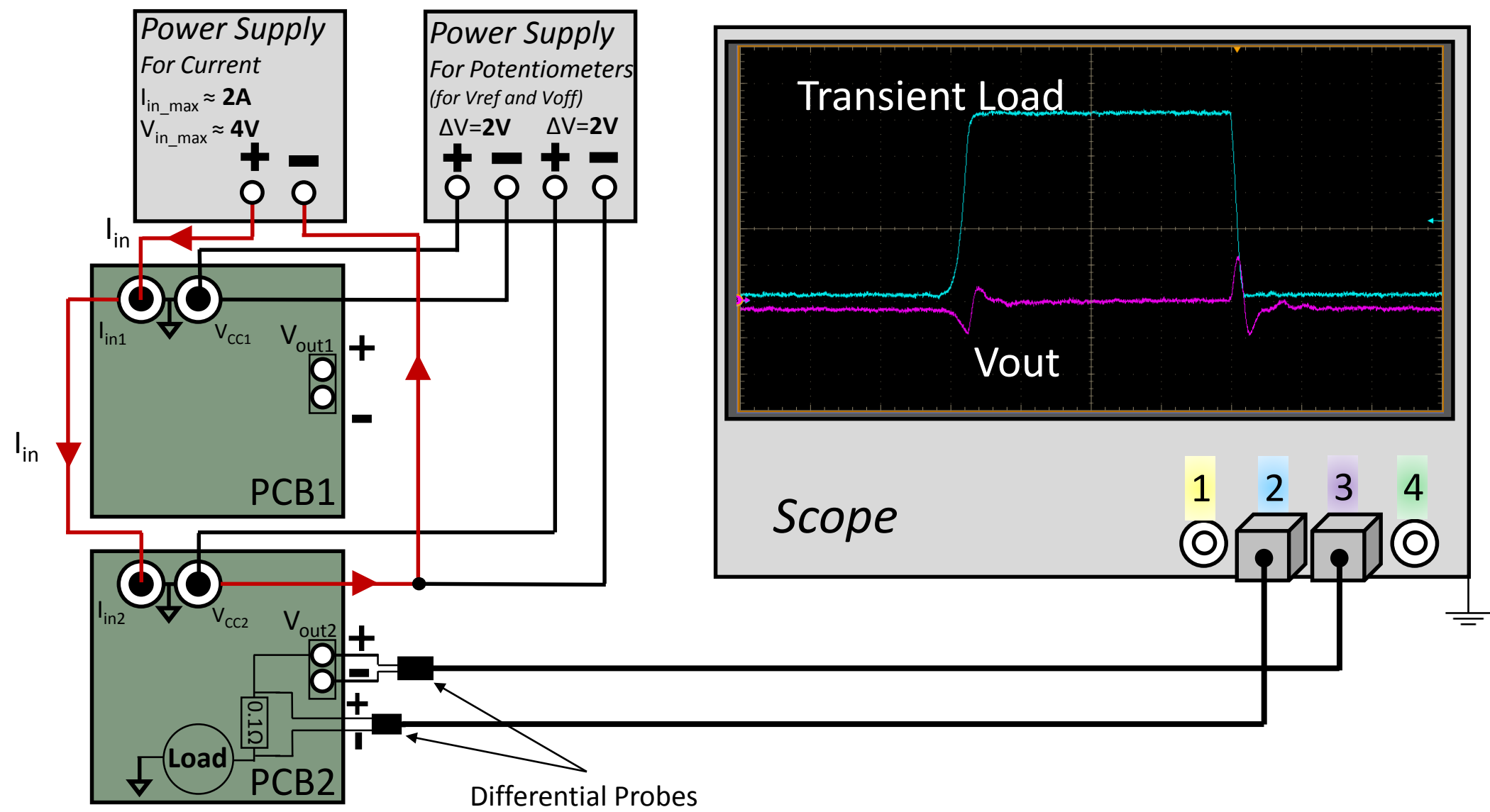
# 2A testchip ShuntLDO Behavior



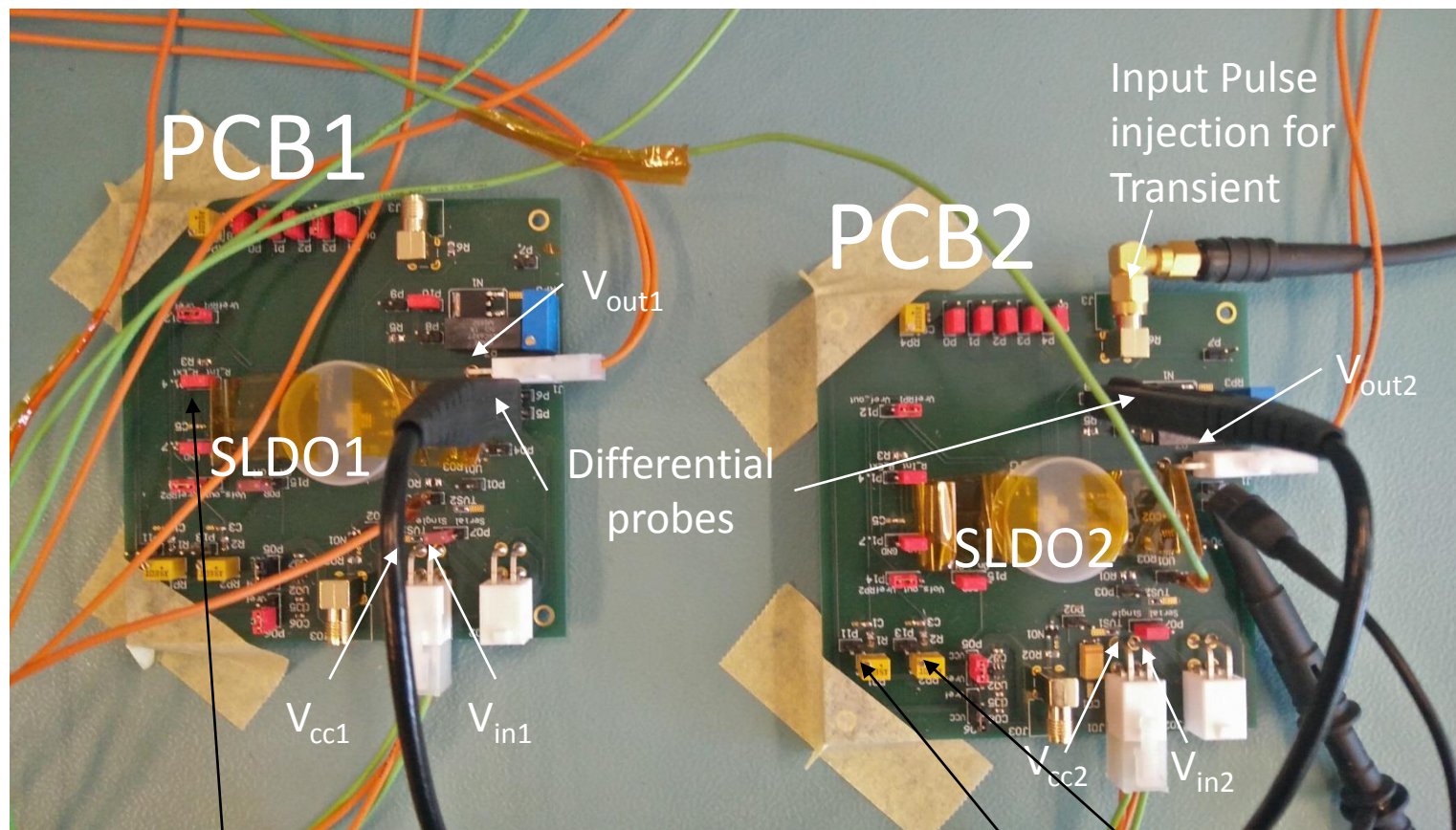
$$V_{out} = 2 * V_{ref}$$

$$V_{in} \approx V_{offset} + I_{in} * R_3$$

# Transient Test Setup Schematic



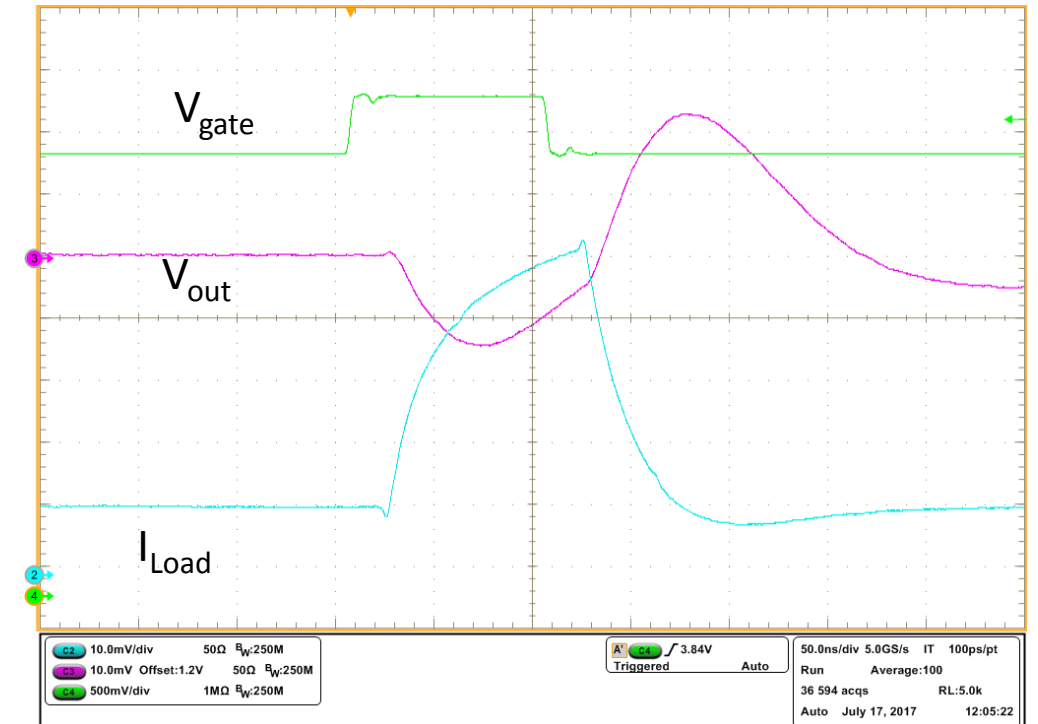
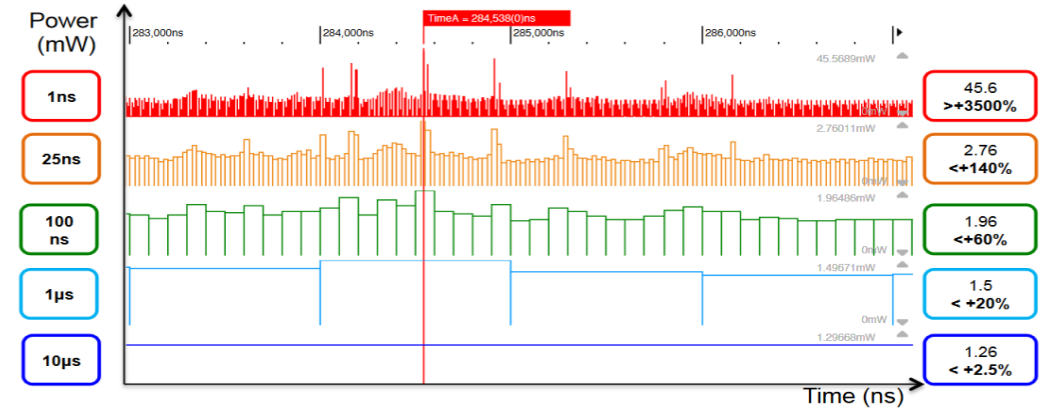
# Transient Test Setup



$R_3$  is either  $R_{in}$  or  $R_{ext}$  depending on the jumper's position

$V_{cc}$  Provides voltage to the potentiometer providing the voltage for  $V_{ref}$  and  $V_{Offset}$

- A Load can be drawn at the output of the SLDO to emulate the chip activity. There are two ways of emulating the load :
  - On-board: a potentiometer for static load or a transistor for dynamic load
  - Instruments: programmable load, sourcemeters,...
- The  $V_{gs}$  of the transistor is controlled by a Pulse Generator
  - Example of input : The Input Pulse of the Transistor is a square Pulse of a 100ns for a 1 $\mu$ s Period from 1.75V to 2V
  - The current drawn by the Transistor has the shape of a charging capacitance
- We can change different parameters :
  - The Input Current
  - The dynamic load (Period, Width and Height, Edge)
  - $V_{offset}$
  - $R_{ext}$
  - Topology
  - ...



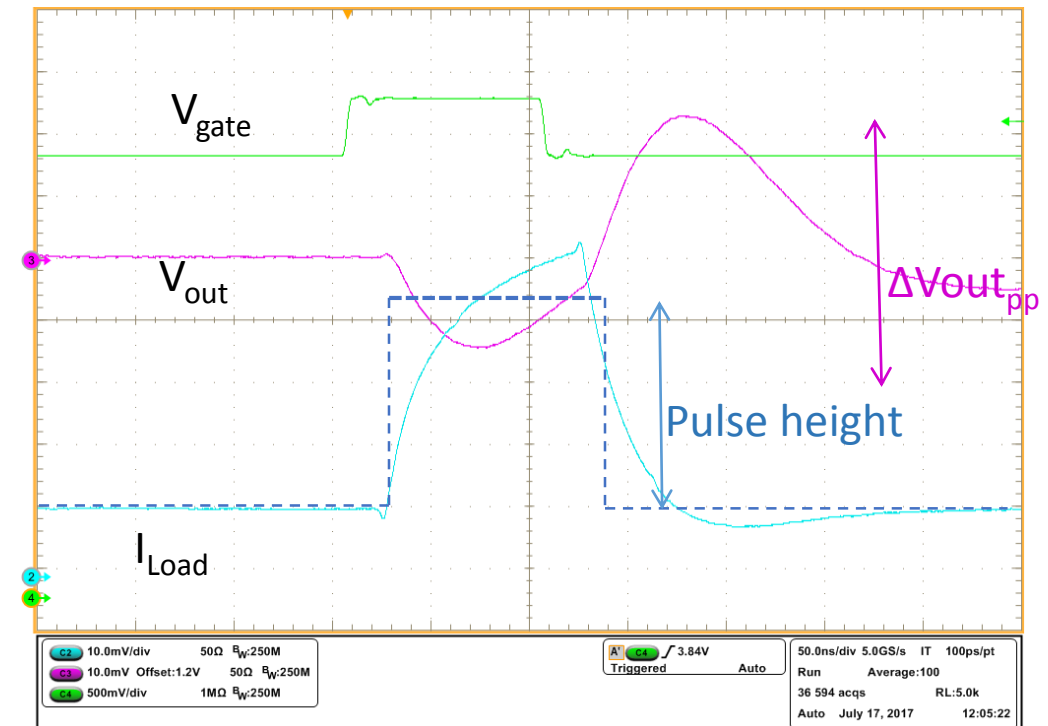
# Transient Tests

A problem with the transistor load was the fact that the load is not a square pulse, so the load pulse cannot be used as a reference as such. Some references were suggested :

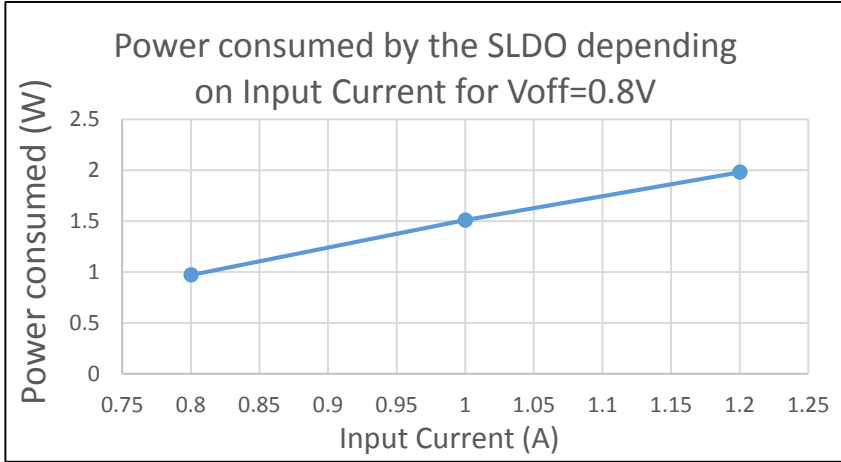
- **Mean Value** : One possible reference is to use the mean value of the load, but there is a problem when the duty cycle is low and the mean may not be really representative of the load.
- **Pulse Area** :

The problem is that the pulse can be really high and so short that the impact is barely visible, and the reference will be overestimated

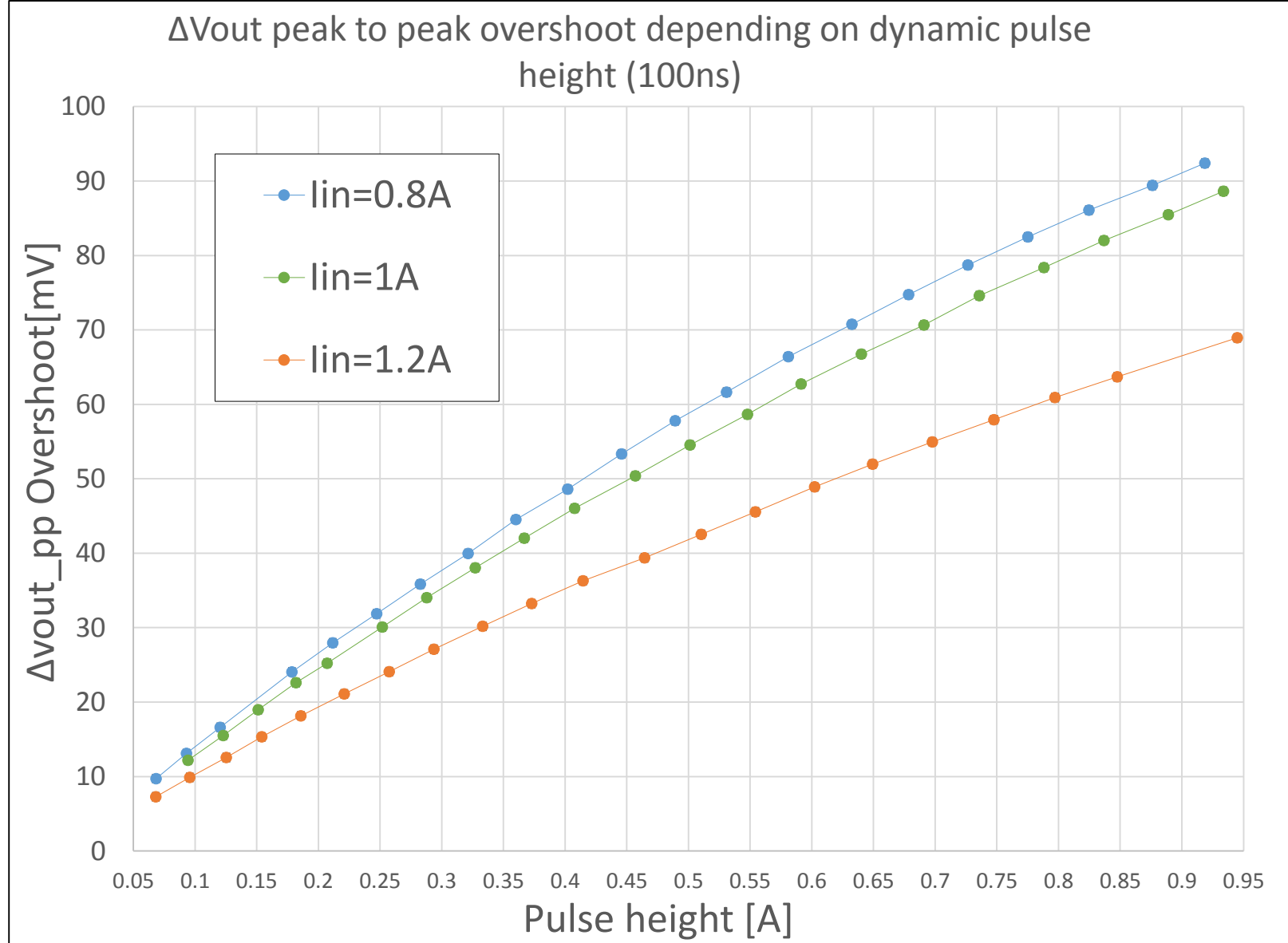
For the Next Plots, The Equivalent height of pulse will be used as a reference for the transient tests



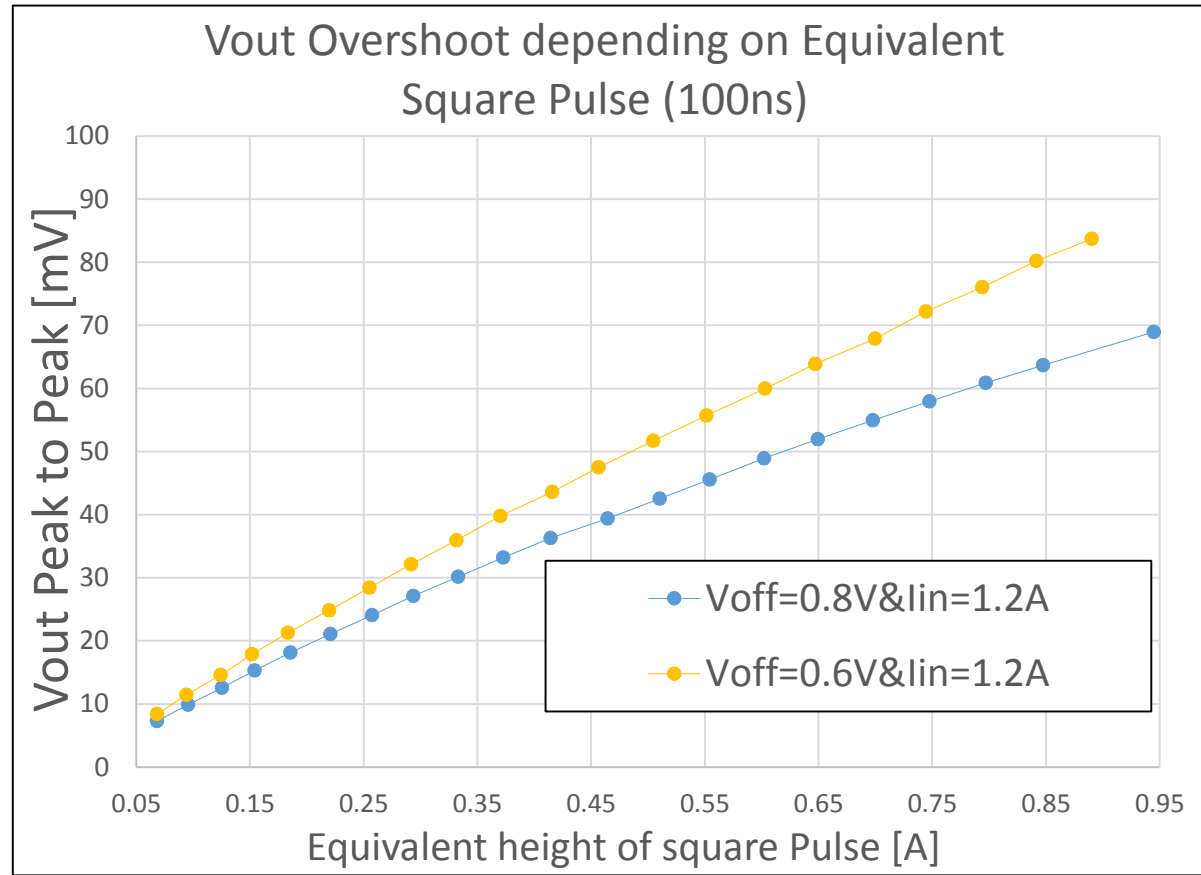
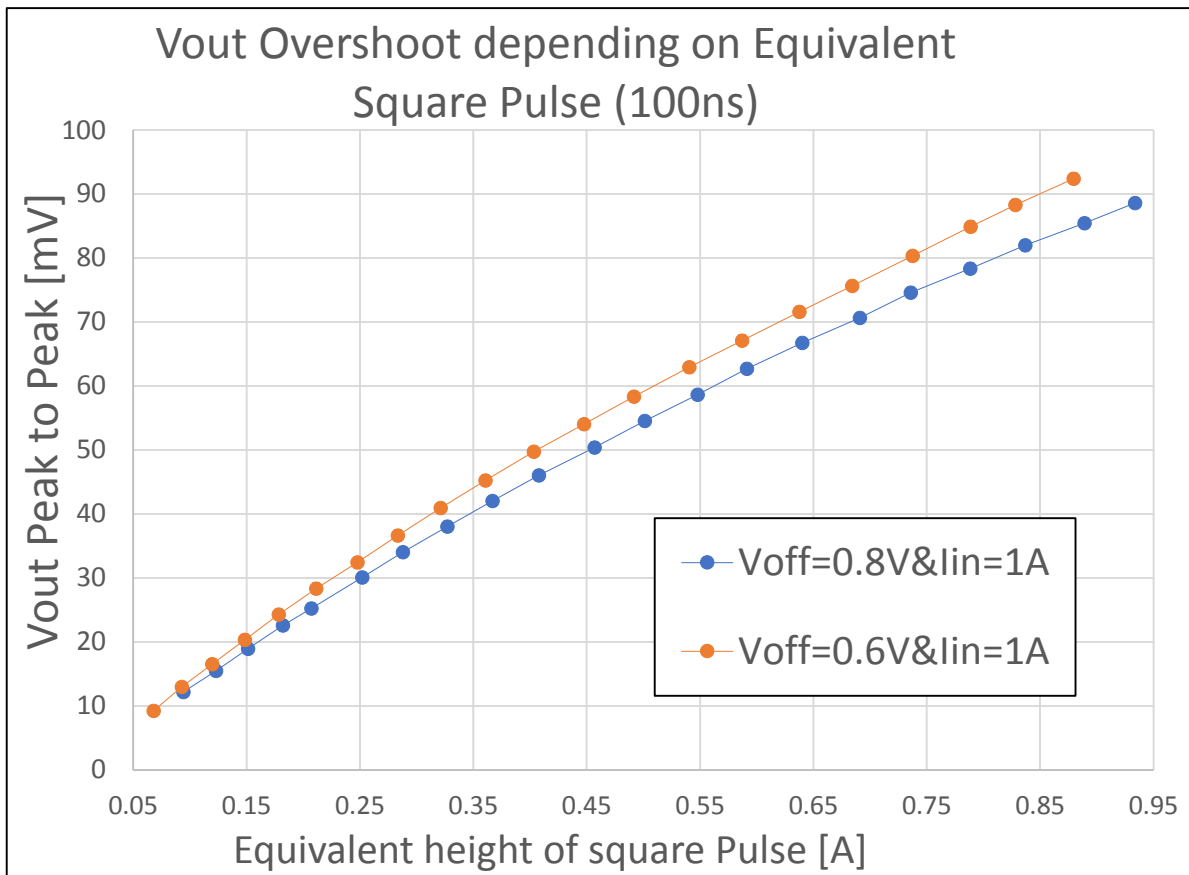
# Transient Tests – Influence of Input Current



- Measuring Vout peak to peak from a SLDO with a dynamic load superimposed to a static load of about 0.4A.
- Voff=0.8V for all 3 cases
- Increasing the input current seems to have a positive influence on the Vout overshoot.
- Going from 0.8A to 1.2A reduces the Vout overshoot by 1/3, but almost double power is consumed by the chip, going from 0.97 to 1.98.
- Improving the performance comes with a power penalty, a compromise must be found.



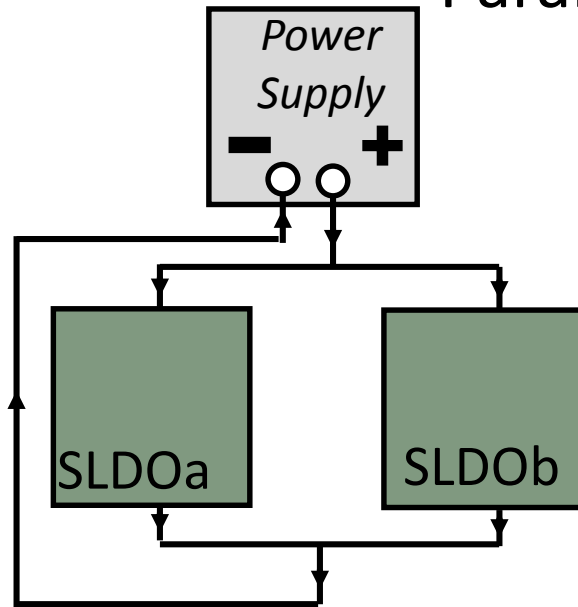
# Transient Tests – Influence of the offset Voltage



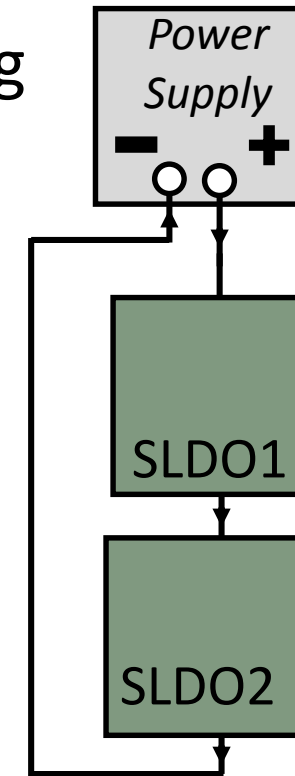
SLDO seems to prefer operating with higher Voff (and so higher Vin), especially for high input currents.

- Monitoring the effect of a dynamic load to a neighboring SLDO for both serial and parallel powering.
- No effect from transient of one SLDO to the other.
- Simulations had shown a small effect (1-10%) which is not possible to measure (lower than the noise levels of the setup)

## Parallel Powering

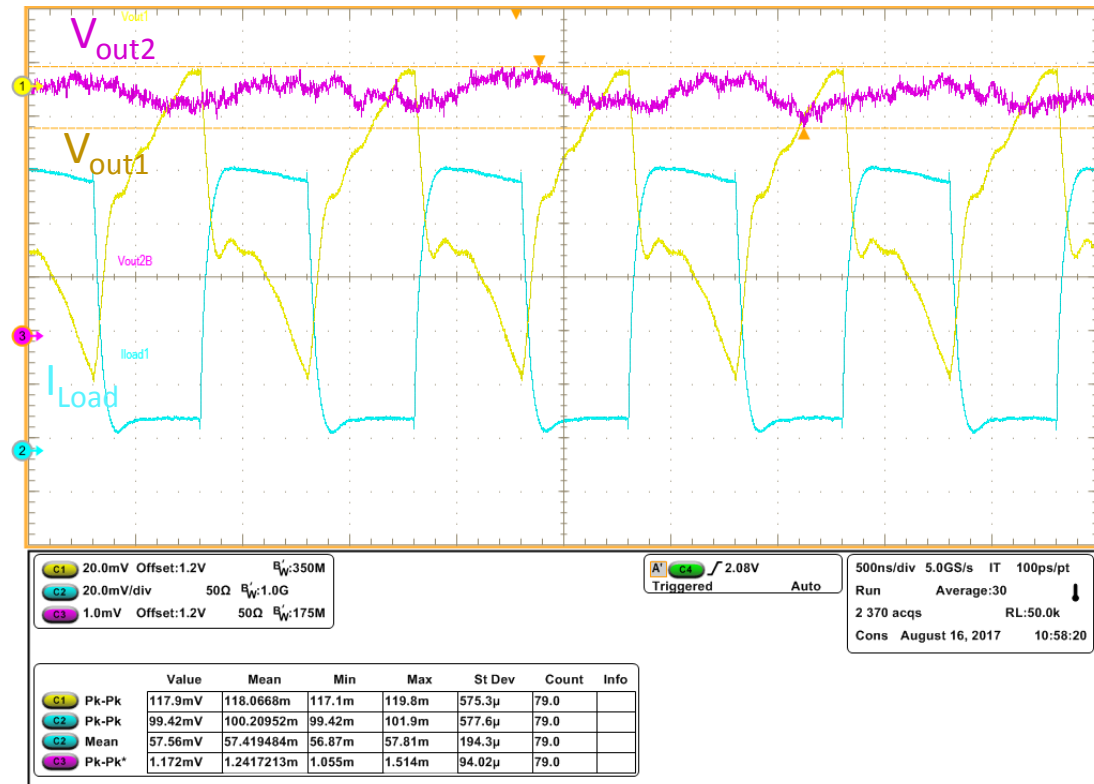


## Serial Powering



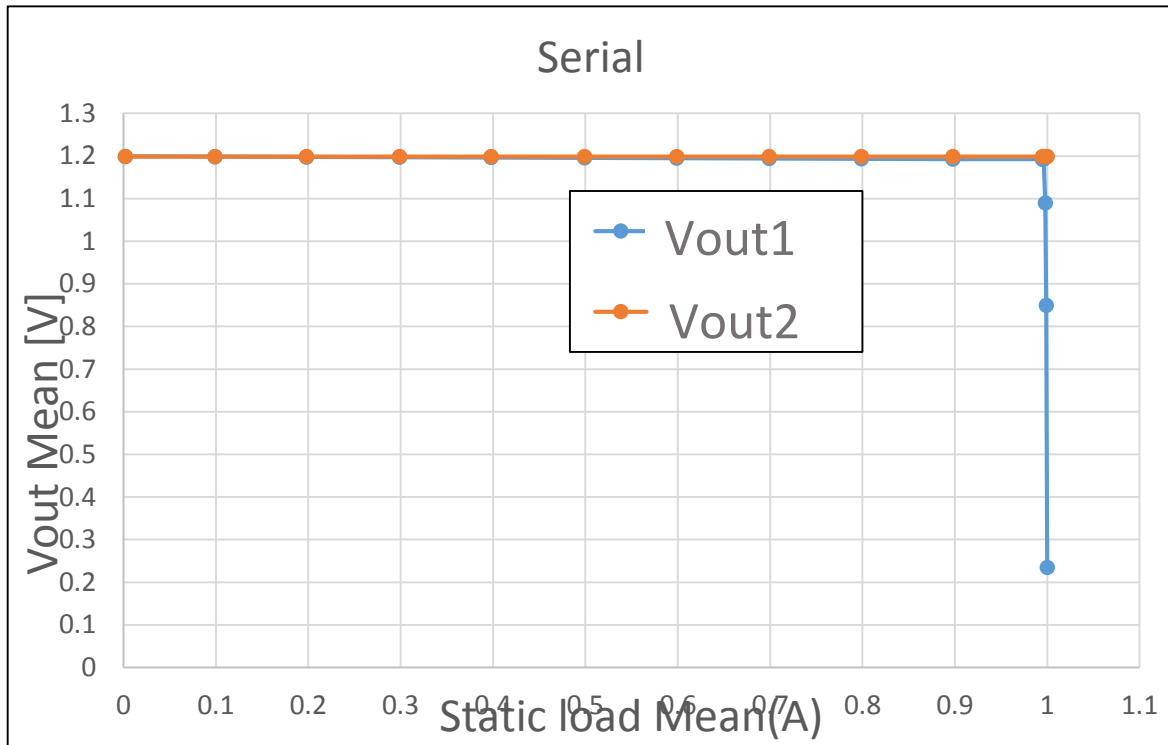
## Parallel powering of 2 chips

- The load goes from 0.1A to about 1.1A for 500ns
- Voltage peak to peak of the SLDO1 with load exceeds 110mV
- A negligible change in the Voltage of the neighboring SLDO , its spread is a bit less than 1.3mV

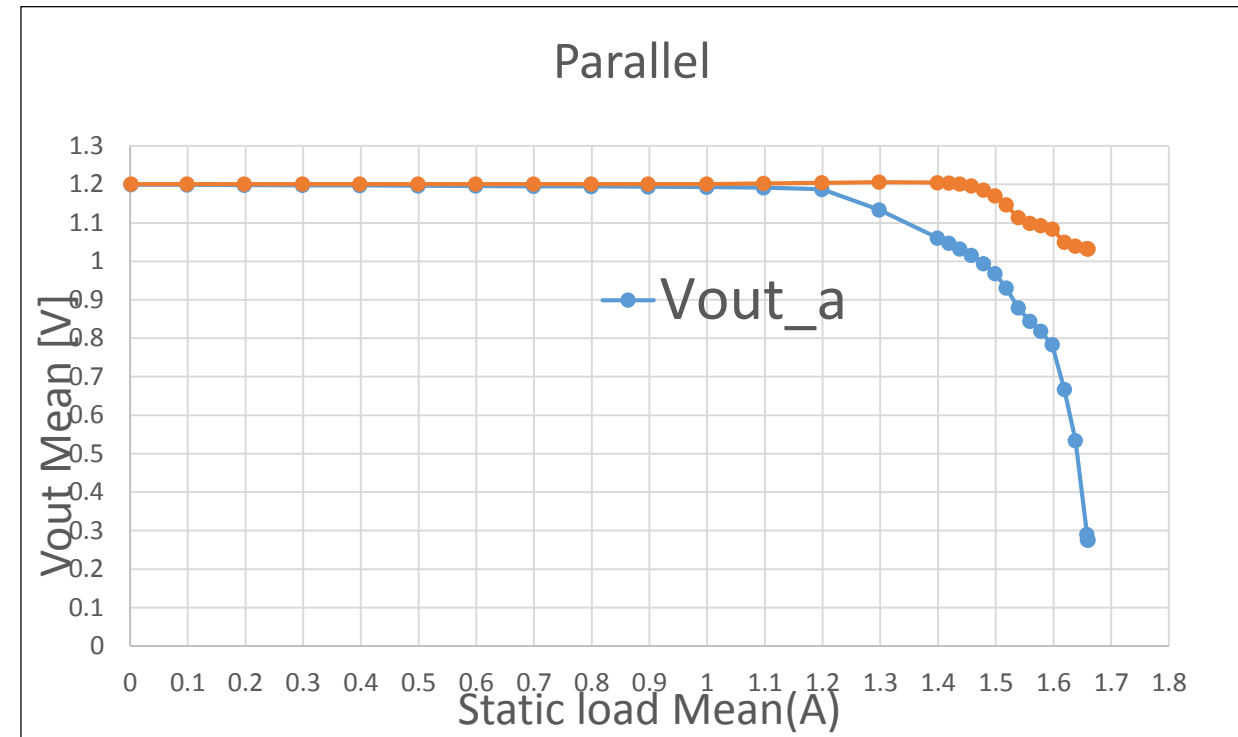


# Parallel VS Serial - Behavior for high load

- In this configuration, 1A per SLDO. The static load is drawing current from PCBa, and the value of the load increases with the horizontal axis.



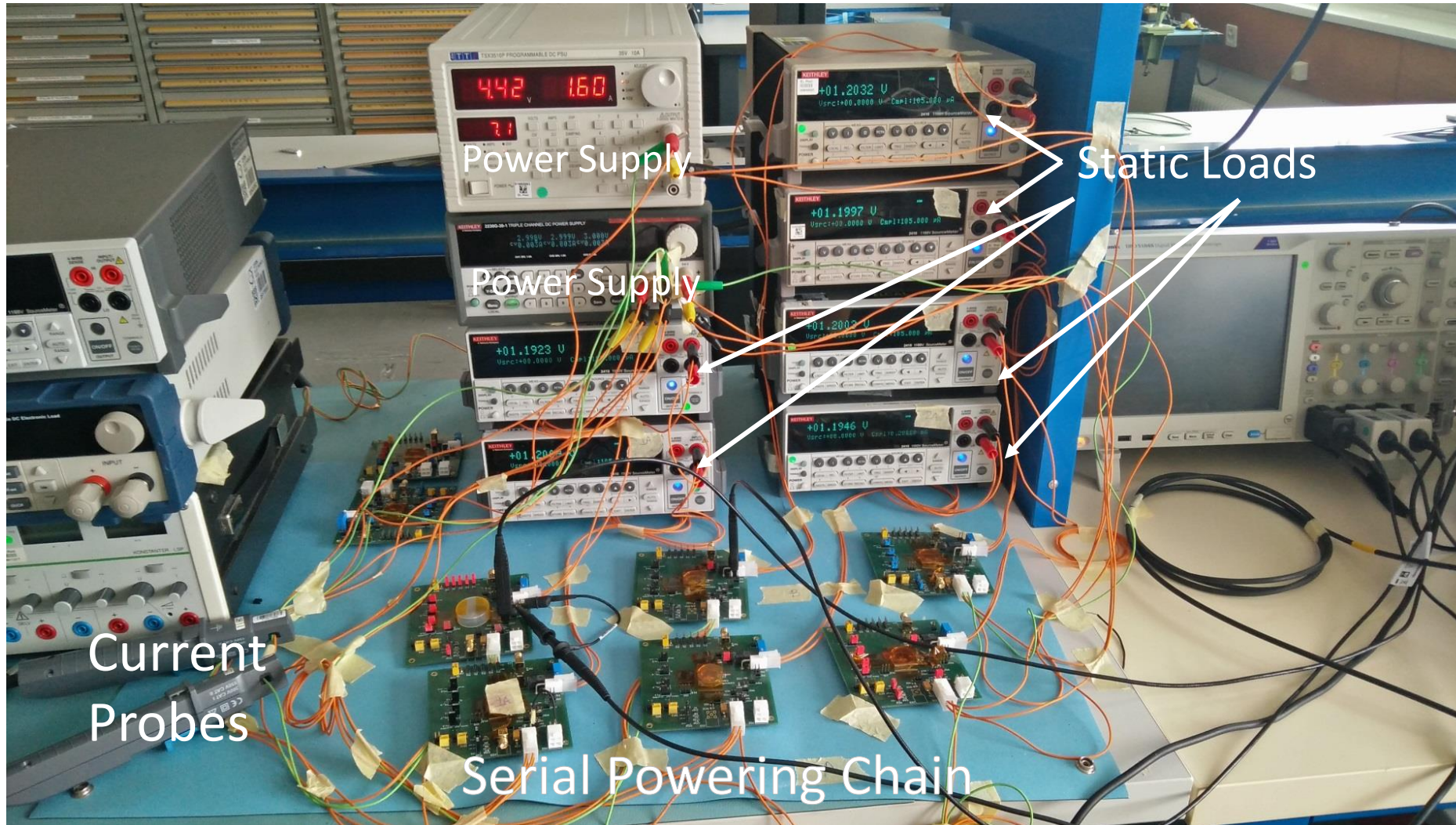
- The static load can draw up to 1A before the SLDO crashes
- The load on PCB1 does not affect PCB2, as expected



- We notice here that the load can draw a bit more than 1A, after that both PCBs crash.

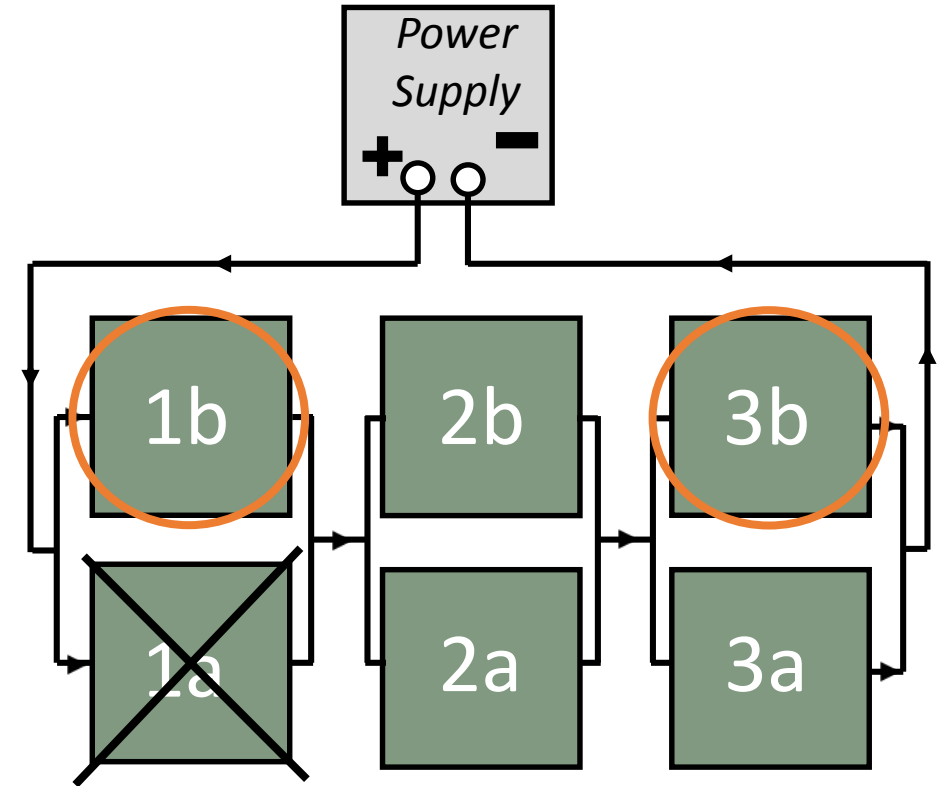
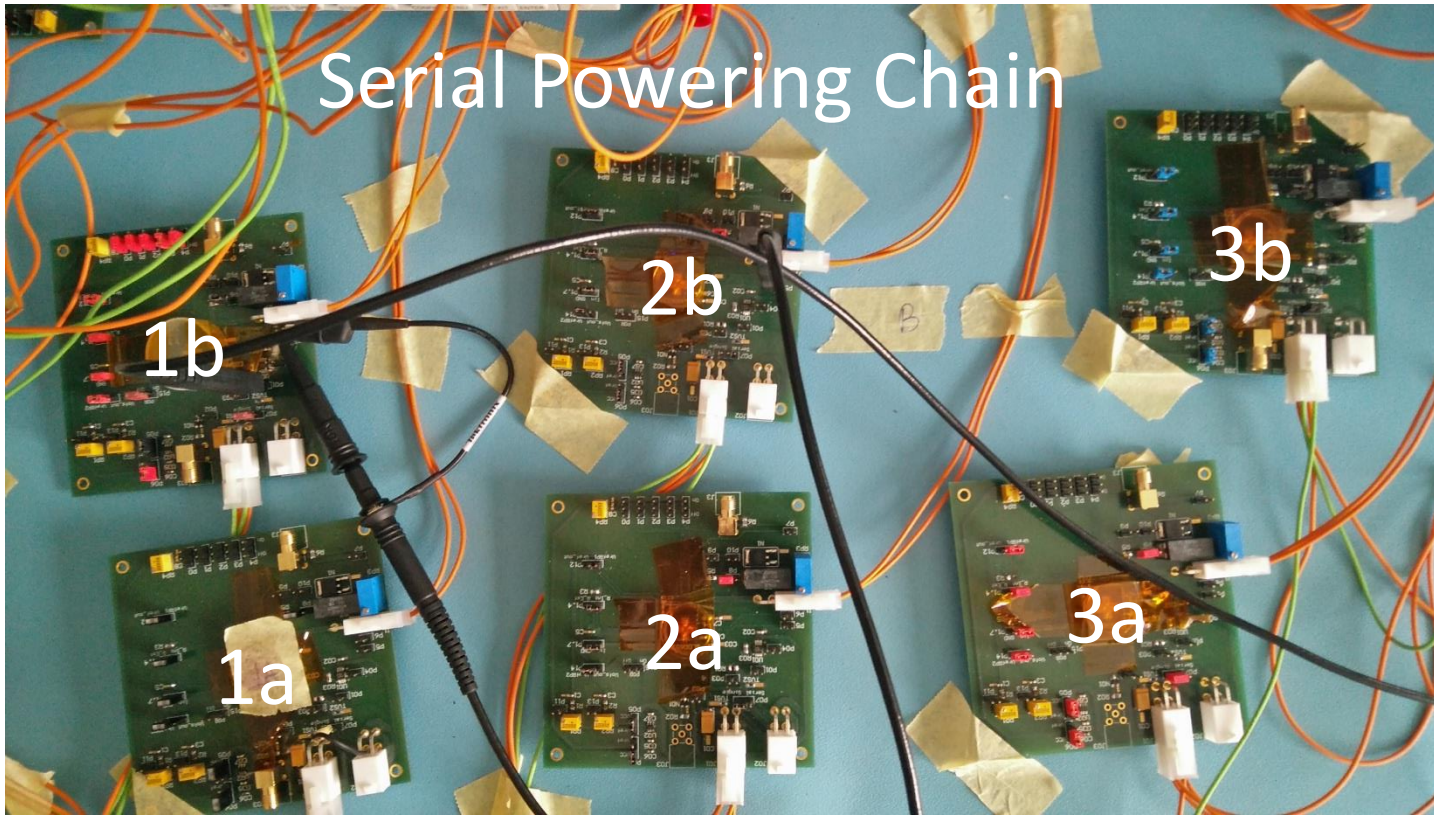
# Serial Powering chain Setup

## Failure Scenarios in the Serial powering Chain



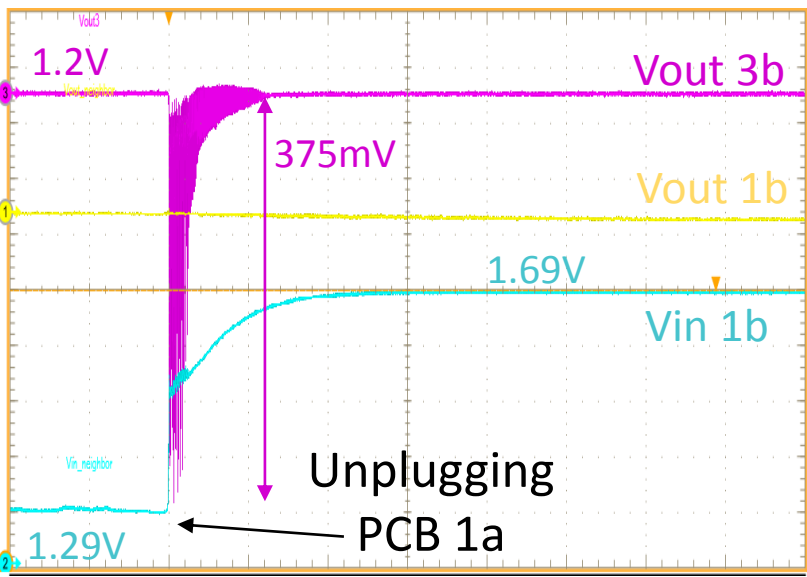
# Serial Powering Chain: Failure Scenarios

Serial Powering chain Setup: 3 levels of 2 SLDOs in Parallel

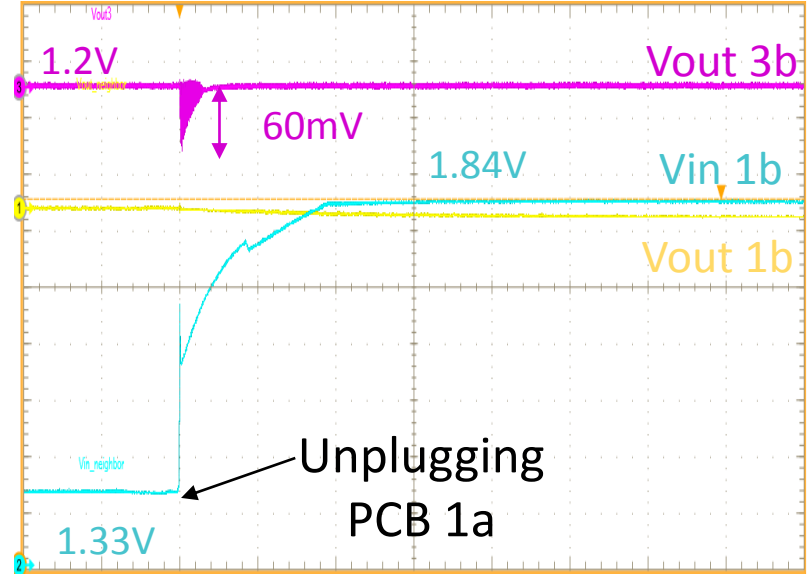


# Failure Scenarios

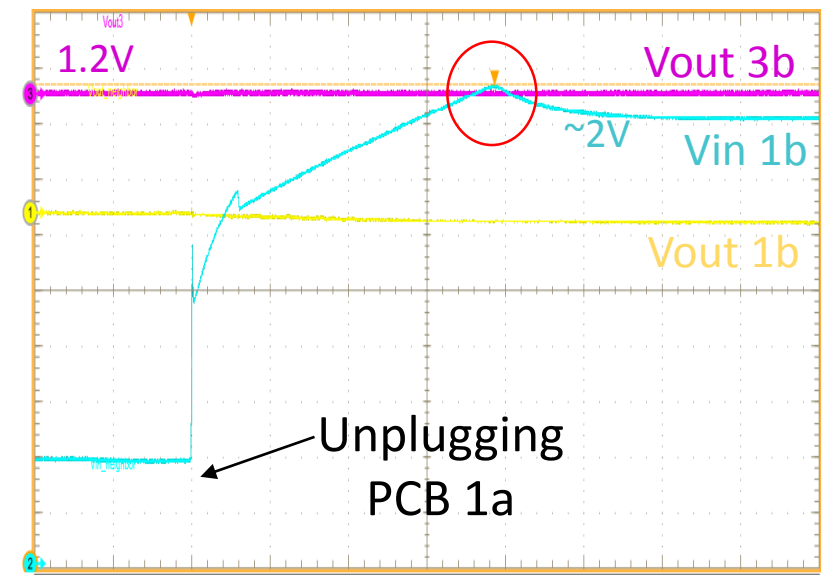
0.3A load for every SLDO



Chain Input Current = 1.2A



Chain Input Current = 1.4A

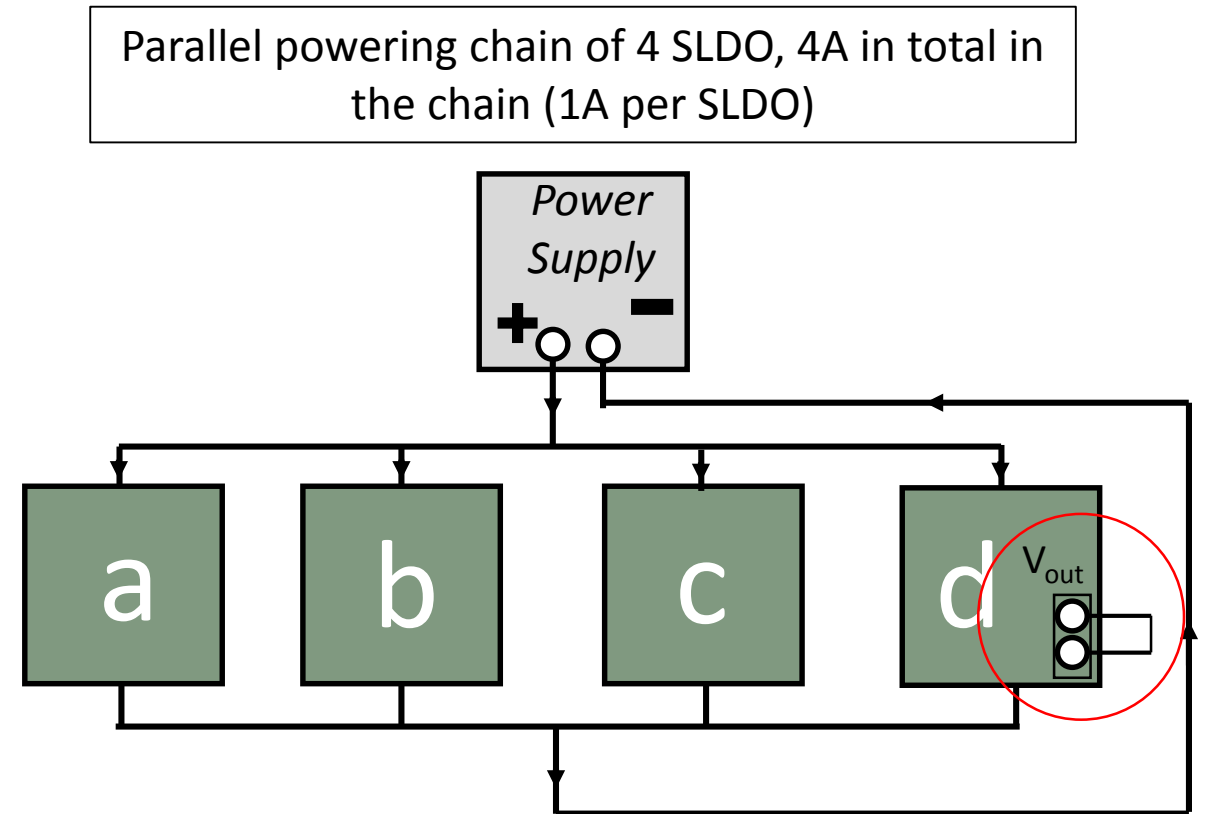


Chain Input Current = 1.7A

The overshoot in Vin is caused by the Power Supply. The power Supply tries to regulate the current because of the failure, but the limiting voltage (due to compliance limit) is limiting the speed of the transient.

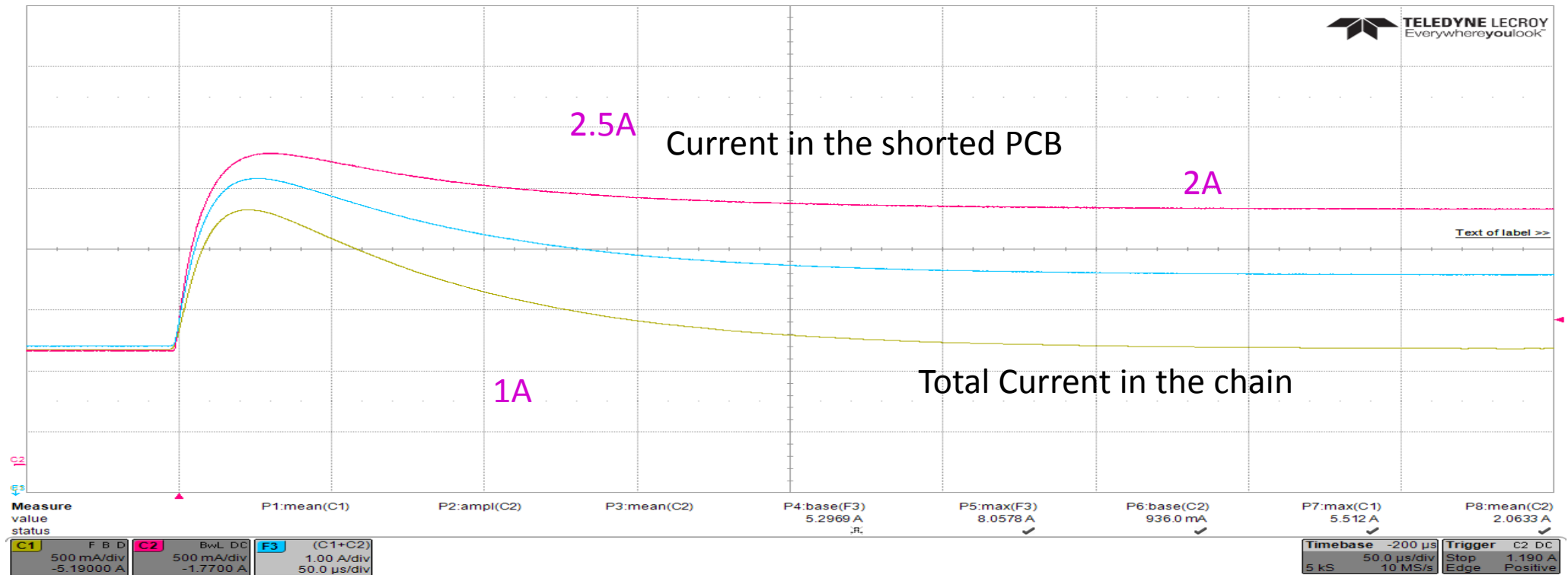
## Serial Powering chain Setup (1 level of 4 PCBs)

- This Failure scenario emulates a short-circuit scenario from one of the SLDO
- The short-Circuit is emulated by connecting  $V_{out}$  to the ground of the SLDO for a short period a time



# Failure Scenarios

## Short Circuit Failure Scenario (4A Input Current in the chain)



When shorted, the SLDO suddenly takes 2.5A, but taking 2.5A for a brief amount of time doesn't seem to have damaged the SLDO . The current settles at 2A in the shorted SLDO.

## **SLDO IV characteristics**

- The SLDO Current-Voltage Characteristics is different in simulation than when measured.

$$V_{in\_Simulation} = 0.8 + 0.6 * I_{in} \quad V_{in\_measured} \approx 0.78 + 0.74 * I_{in} \quad (\text{Using Rint})$$

## **Transient Tests**

- Transient Tests seem to show that the SLDO prefers to receive higher input current when exposed to a dynamic load
- SLDO also seem to prefer having a higher  $V_{off}$  (so a higher  $V_{in}$ ), especially for high input current.

## **Parallel Powering VS Serial Powering**

- When in serial powering mode, it seems like transient have no effect whatsoever on SLDO present in another level of the chain.
- When in parallel powering, having a load on 1 PCB drawing too much current can crash both SLDOs. This is not observed in serial powering.

## **Failure Scenarios**

- When a failure scenario happens, the SLDO can either be shorted or in open-circuit
- When the chain is powered with very low current,  $\Delta V_{out}$  can exceed 350mV peak to peak
- With higher currents in the chain,  $\Delta V$  reduces to less than 10mV
- $V_{in}$  can rise above the 2V limit, the Power Supply Design has to take that in consideration

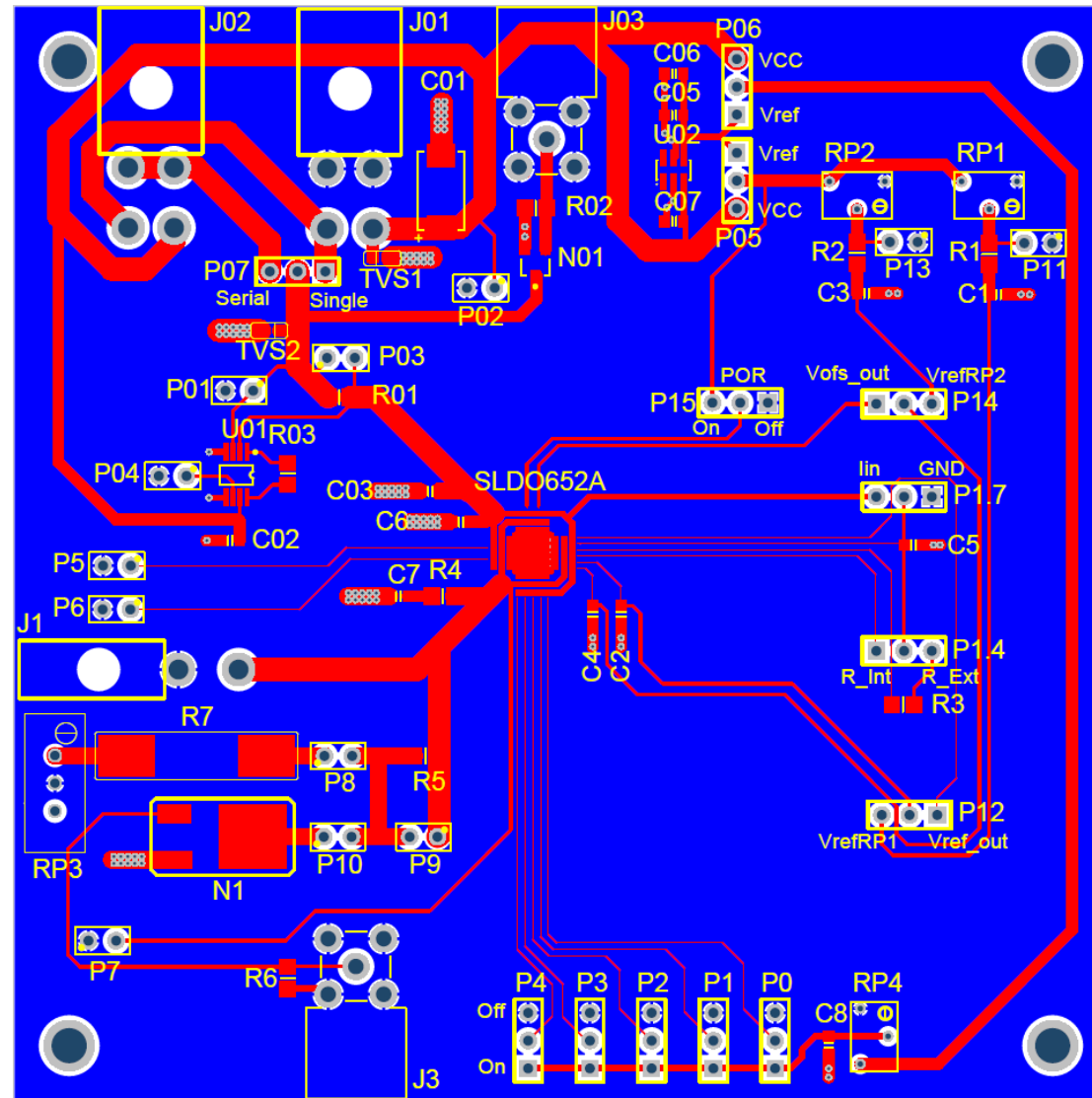
## References - Publications

- D.B. Ta, T. Stockmanns, F. Hügging, P. Fischer, J. Grosse-Knetter, Ö. Runolfsson, N. Wermes. Concept, realization and characterization of serially powered pixel modules (Serial Powering). *Nuclear Instruments and Methods in Physics Research*. 565 (2006) 113–118
- D.B. Ta, T. Stockmanns, F. Hügging, P. Fischer, J. Grosse-Knetter, Ö. Runolfsson, N. Wermes. Serial powering: Proof of principle demonstration of a scheme for the operation of a large pixel detector at the LHC. *Nuclear Instruments and Methods in Physics Research*. 557 (2006) 445–459
- L. Gonella, D. Arutinov, M. Barbero, A. Eyring, F. Hügging, M. Karagounis, H. Krüger and N. Wermes. A serial powering scheme for the ATLAS pixel detector at sLHC. *Journal of Instrumentation* SEPTEMBER 2010, 20–24
- S. Marconi, S. Orfanelli, M. Karagounis, T. Hemperek, J. Christiansen and P. Placidi. Advanced power analysis methodology targeted to the optimization of a digital pixel readout chip design and its critical serial powering system. *Journal of instrumentation*. 2017 JINST 12 C02017

*Thank You for Your Attention*

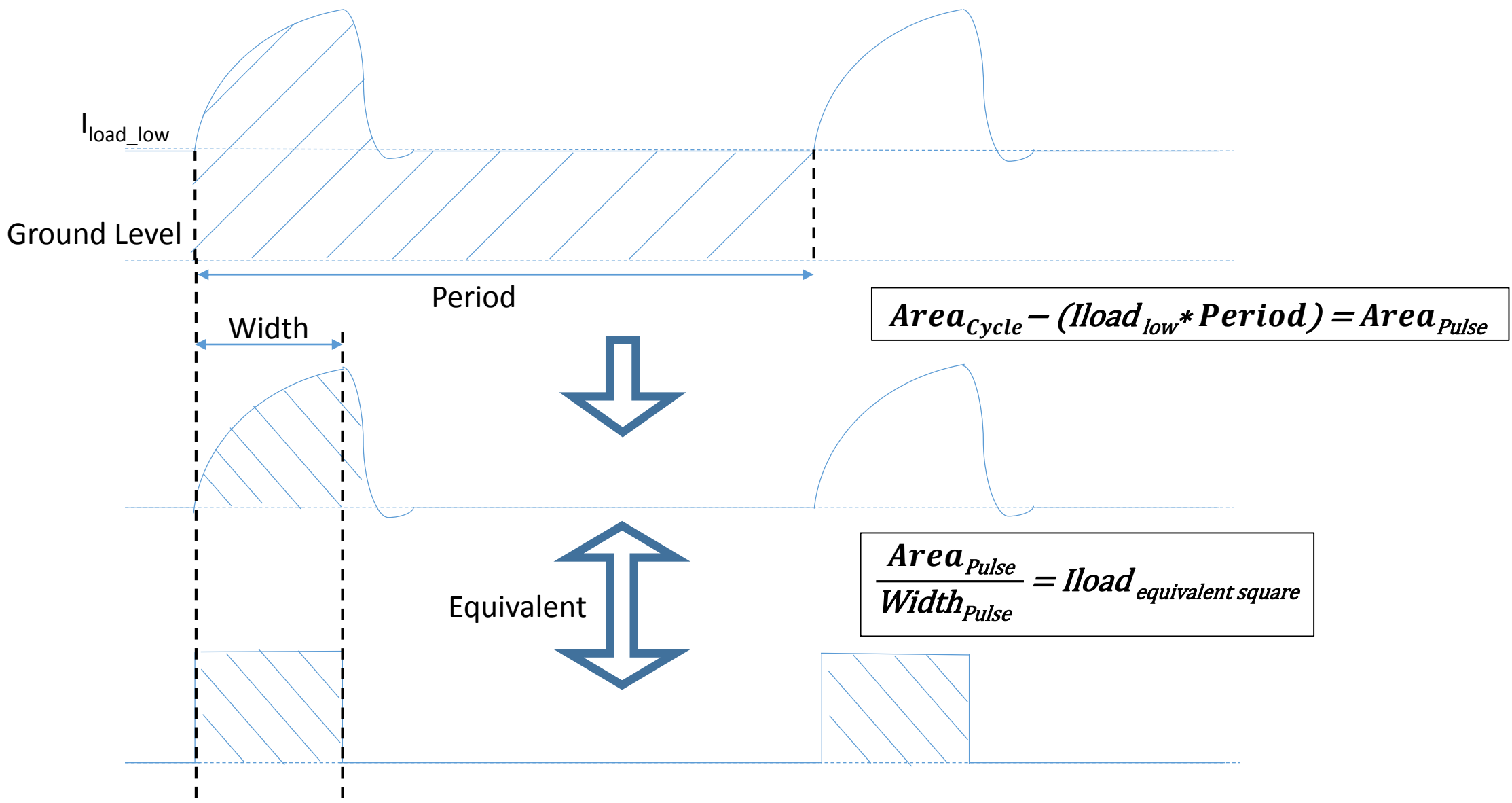
*Questions?*

# Serial Powering – Extra Slides

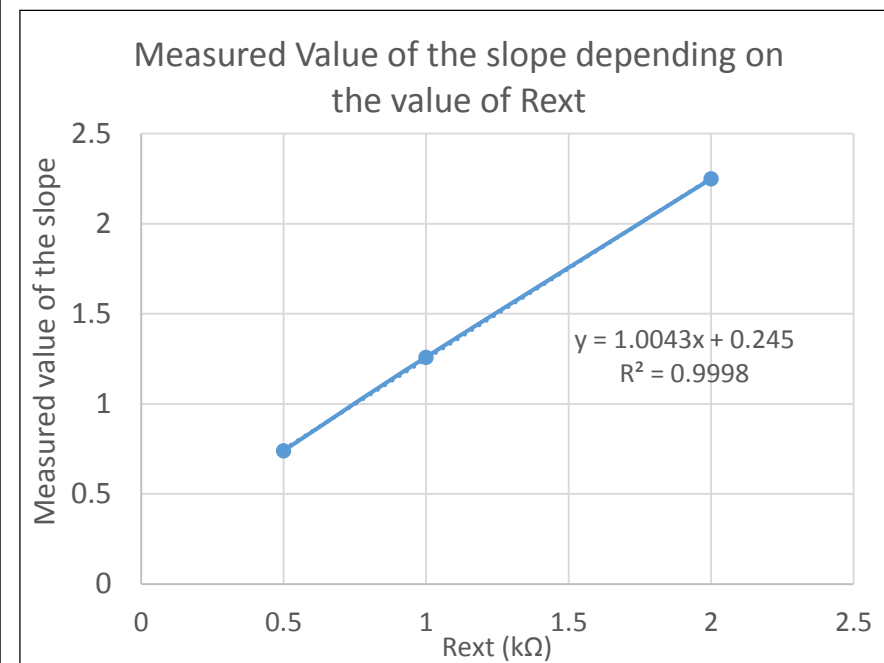
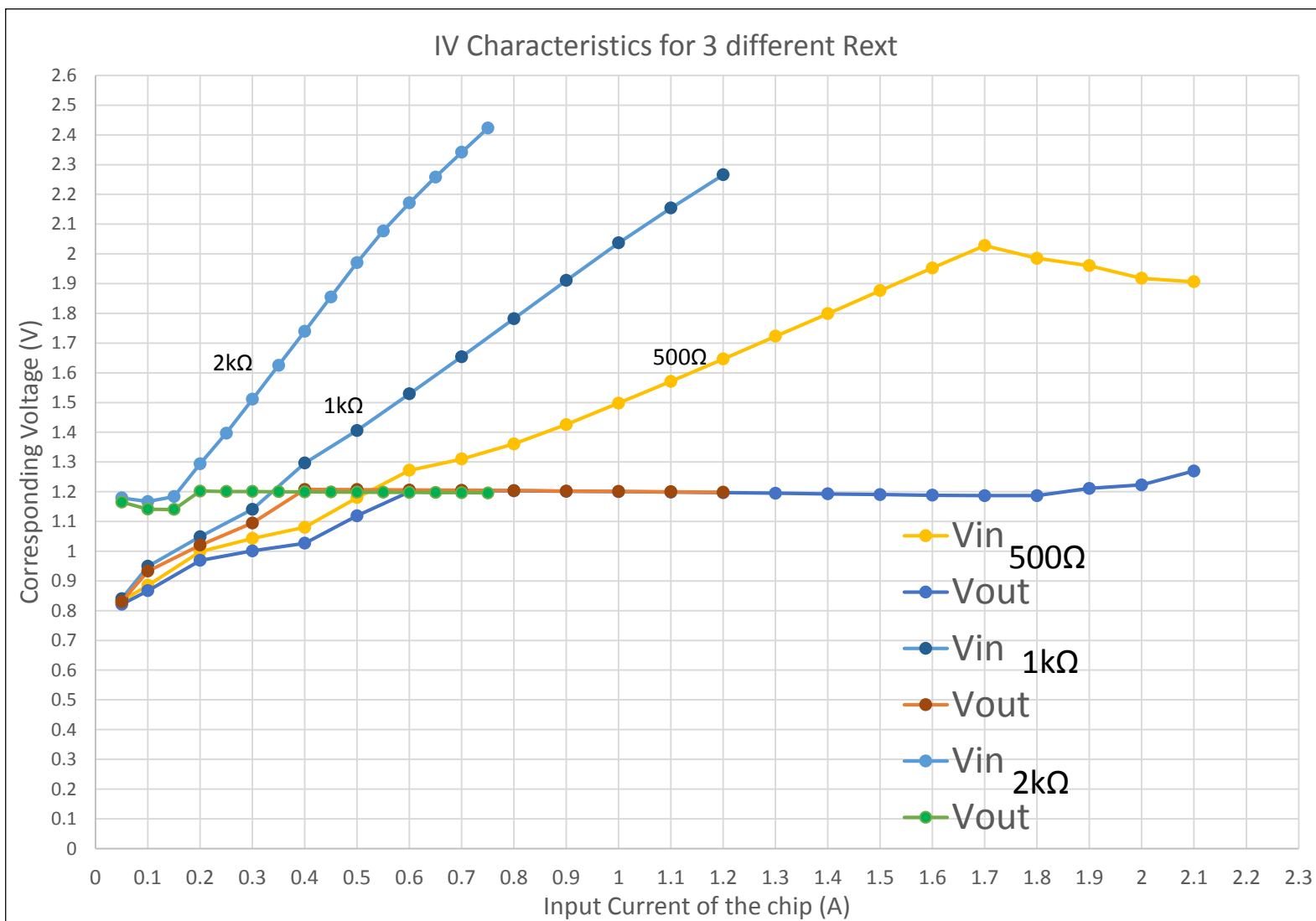


SLDO PCB Layout

# Serial Powering – SLDO PCB Tests



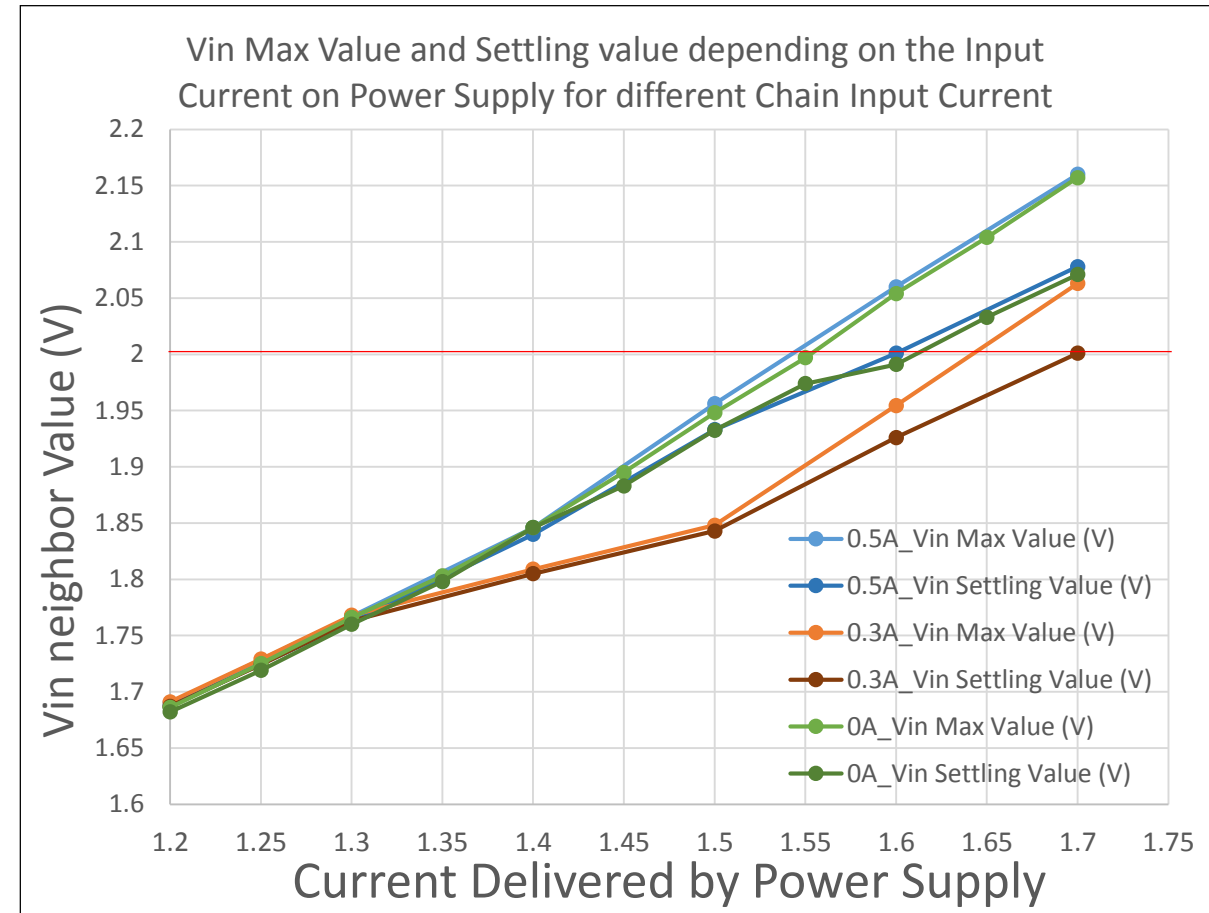
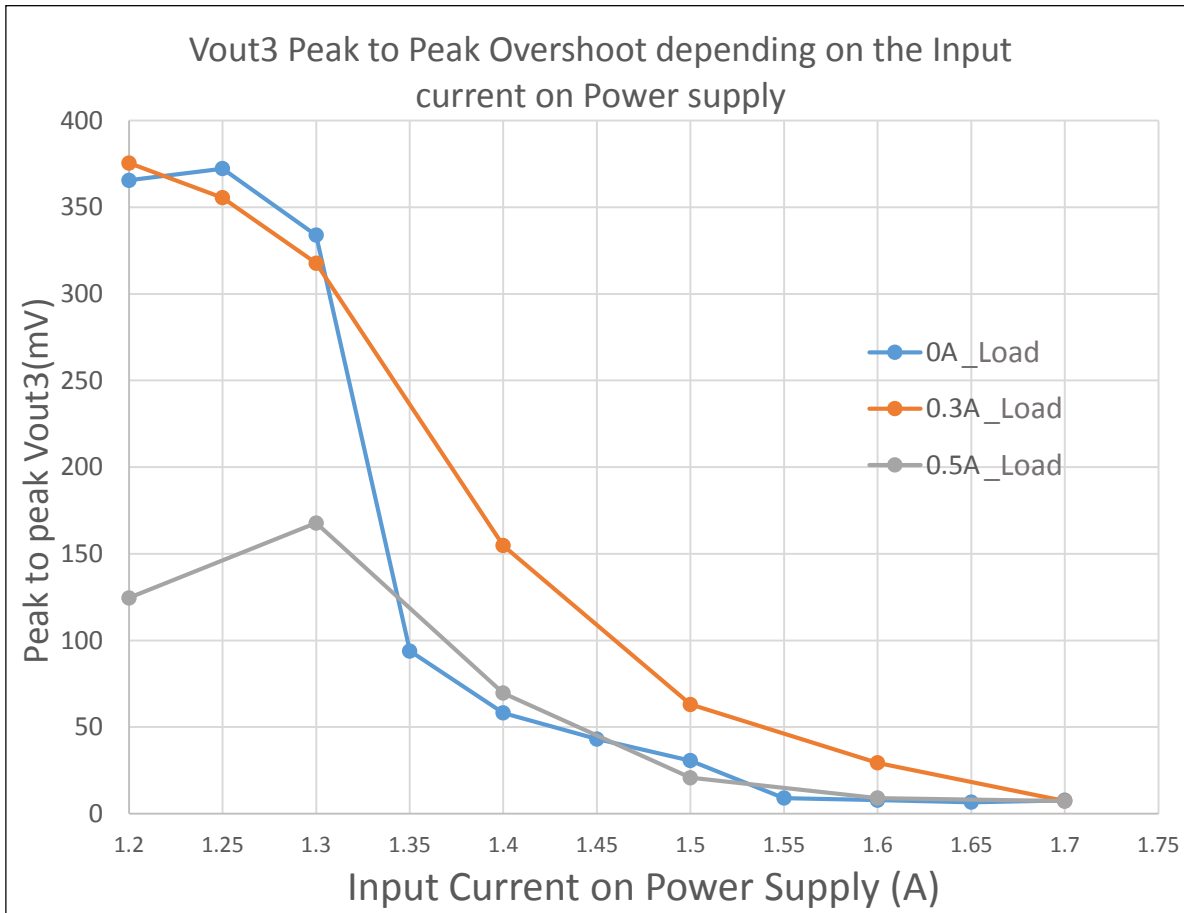
## IV characteristics for different Rext



The behavior of the SLDO is approximately linear when changing Rext.

# Failure Scenarios

## Load on every PCB in the chain



- The SLDO is more stable during Open Circuit failure scenario with a static load of about 0.5A for low currents

- This has to be taken in consideration for the Power Supply design, the choice of compliance depends strongly on the power supply.