Electronics design for HEP experiments and accelerator technology at WUT

R.S.Romaniuk, et al.

Outline

- WUT in numbers and HEP/Acc at WUT
- Electronics for HEP and Accelerators

- Examples (ISE-PERG): CMS-RPC-MT, JET-EFDA-GEM det, Astro-GRB, LHC-SMP
- Examples: (prof.J.Dobrowolski, ISE-Microwaves): DESY, FLASH, XFEL
- Examples (prof.K.Zaremba, WUT): COMPASS, C2GS, T2K
- Examples (prof.M.Lipiński, AGH): fiberoptic virtual atomic clock
- Examples: ph.d students at CERN – TOTEM, White Rabbit, LHC Interlocks, Beam diagnostics, Alba,

WUT in numbers

- Education specialties – 30
- Faculties – 20
- Students – nearly 36000
- Academic staff – 2500 (500 prof.)
- Total staff – 5000

- Faculty of E&IT is ~15% of WUT

„Nuclear” sciences at WUT

- Electrical Engineering
- High Power and Nuclear Engineering
- Electronics Engineering
- IT and Computer Science
- Material Engineering
- Mechanical Engineering and Machine Constr.
- Physics
- Chemistry
- Around 150+ people, 15 groups, plus Ph.D. students, international cooperation, no large local Accelerator infrastructure

Electronic systems in HEP experiments

Basic tasks of electronic systems:

- **Measurements:**
  Reception and conditioning (amplification, filtering, shaping) of analog signals from detector; ADC process to obtain digital representation of measured value

- **Processing:**
  Realization of fast digital processes to obtain interesting physical values: detector signal analysis to extract particle paths

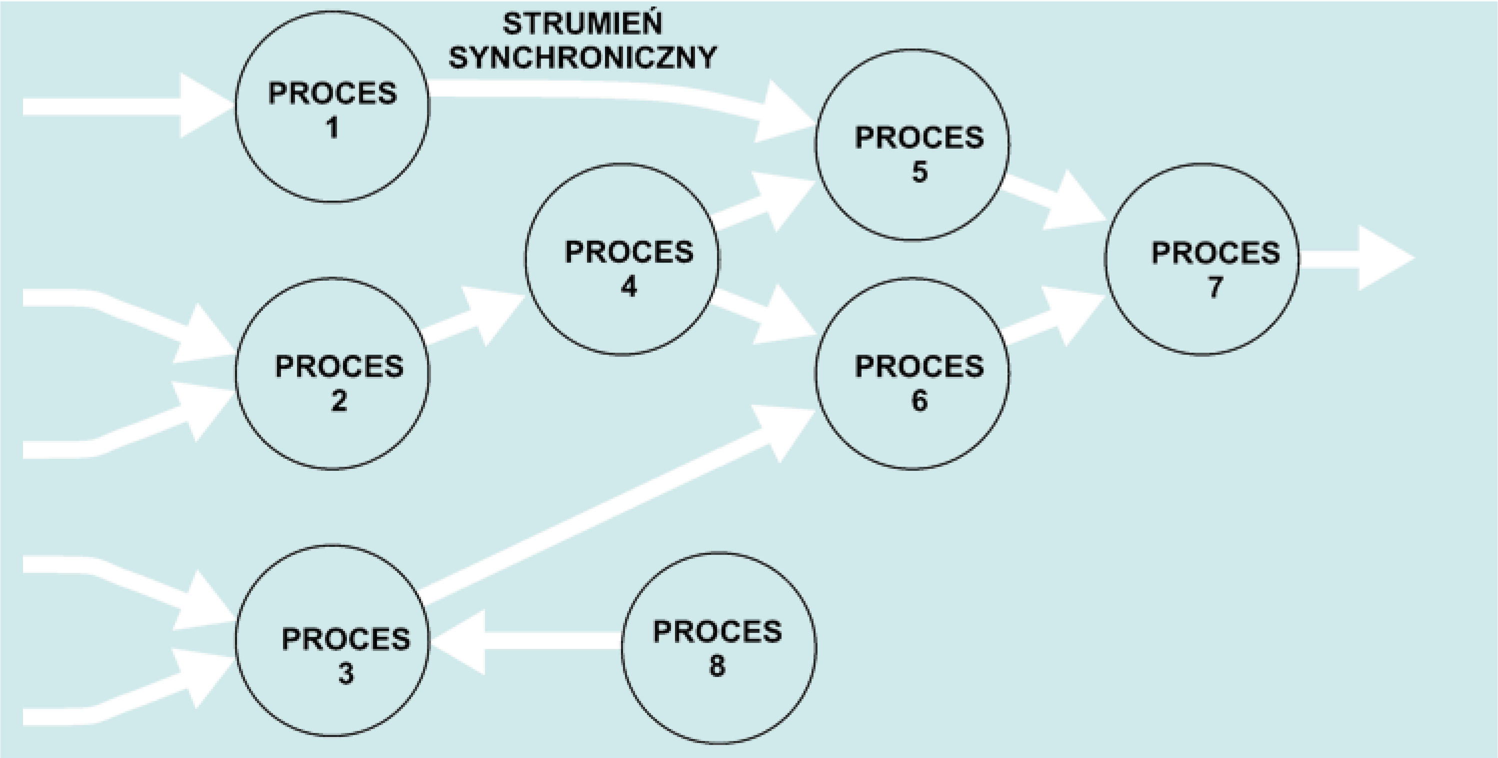
- **Data acquisition:**
  Building of collision images database from the data chosen by local or global trigger

Electonic systems in HEP experiments

Basic features of electronic systems:

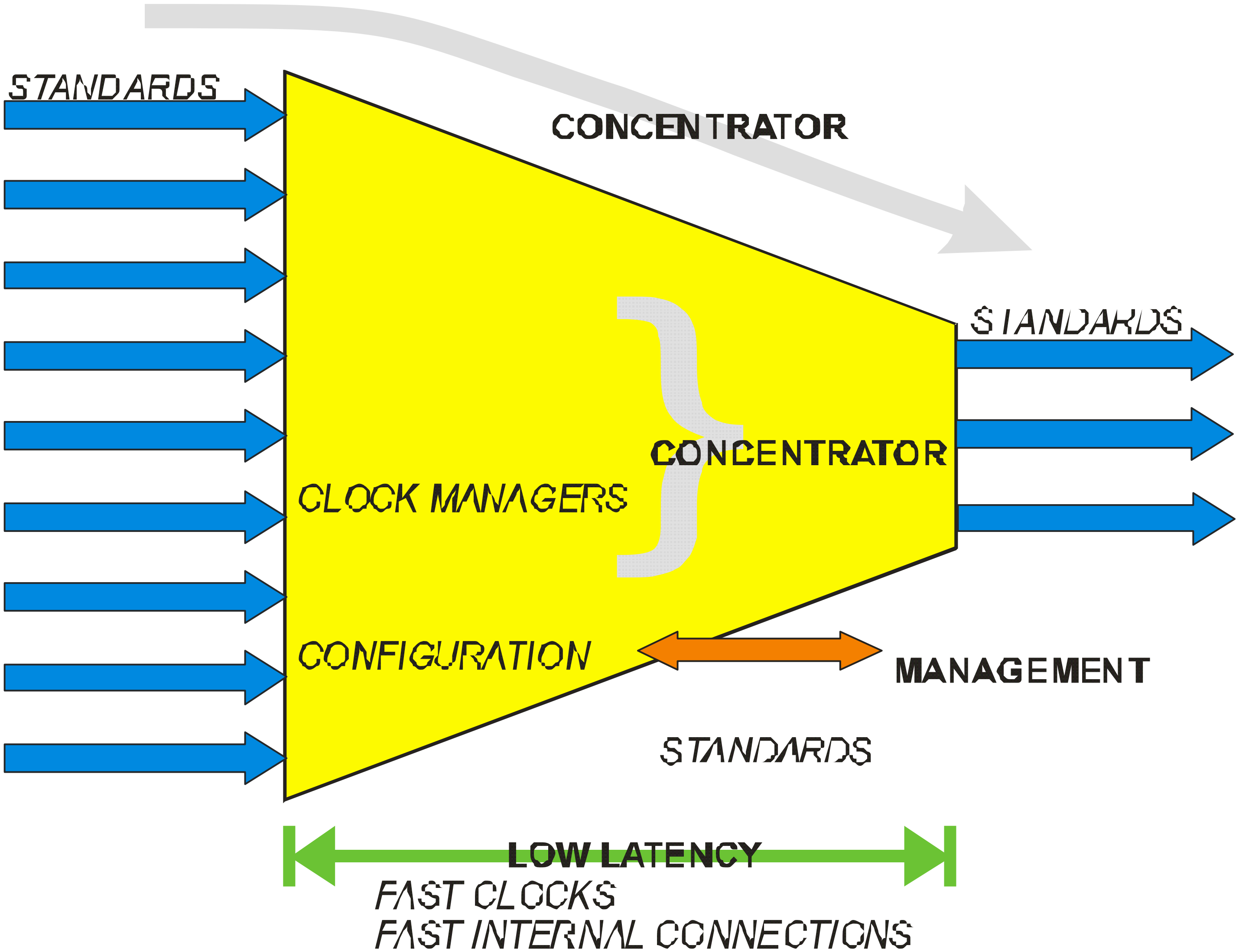
- BIG RATE stems from the collision frequency and the need to analyse each recorded particle bunch collision independently
- MULTI CHANNEL required by the space resolution of the detector, 100 mega channels
- SYNCHRONOUS relevant to the successive collisions, time correlation is maintained on all levels of signal processing in all channels, all detectors, and all global systems of the experiment
- DISTRIBUTED stems from large dimensions of detectors, confined room on detectors, large distances between electronics modules
- PIPELINED large rate, synchronous, data processing in series by successive functional blocks, increase in system throughput

TRIDAQ System Model



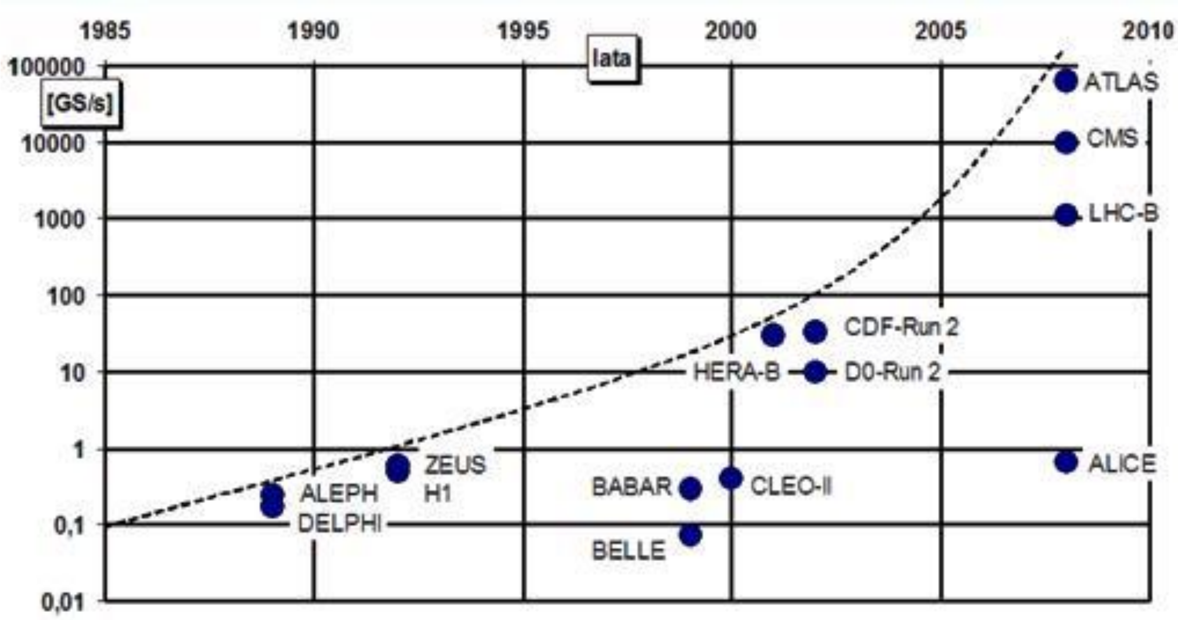
- TRIDAQ System is modelled as a distributed network of disspated pipeline processes
- Network of processes builds a full functional layer of the system, and realizes particular taks or group of tasks for the experiment
- Network node is a functional unit and is not identical with the division of the system to physical electronic modules

Network Node: example of fpga solution



Hardware concentrator

Increase in number of measurements in HEP experiments



Reasons: increase of energy and luminosity; decrease of active cross-section

Increase during the last two decades

First Level Trigger rate: **one thousand** times

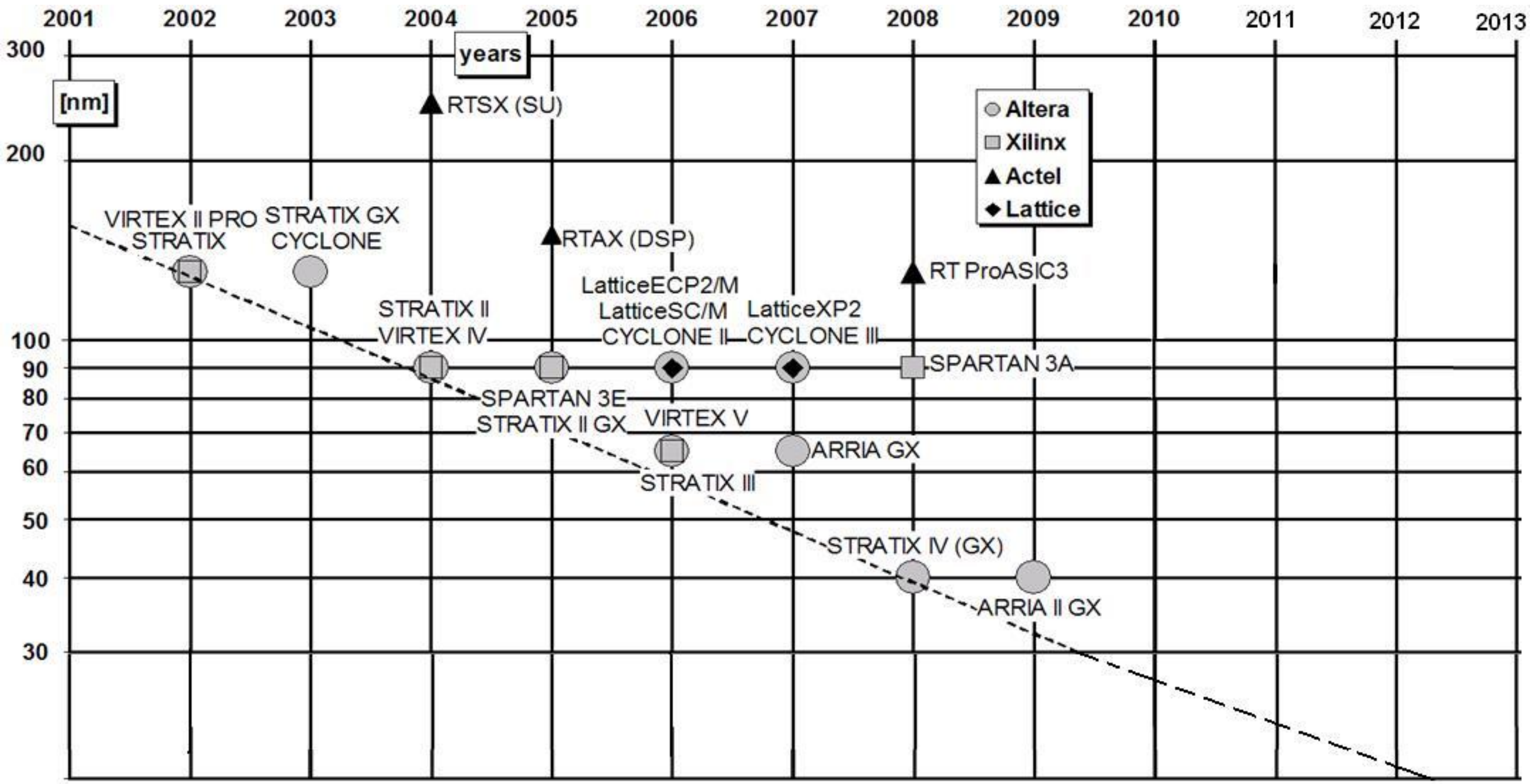
Number of measurement channels: **three hundred** times

Size of registered events: **fifty** times

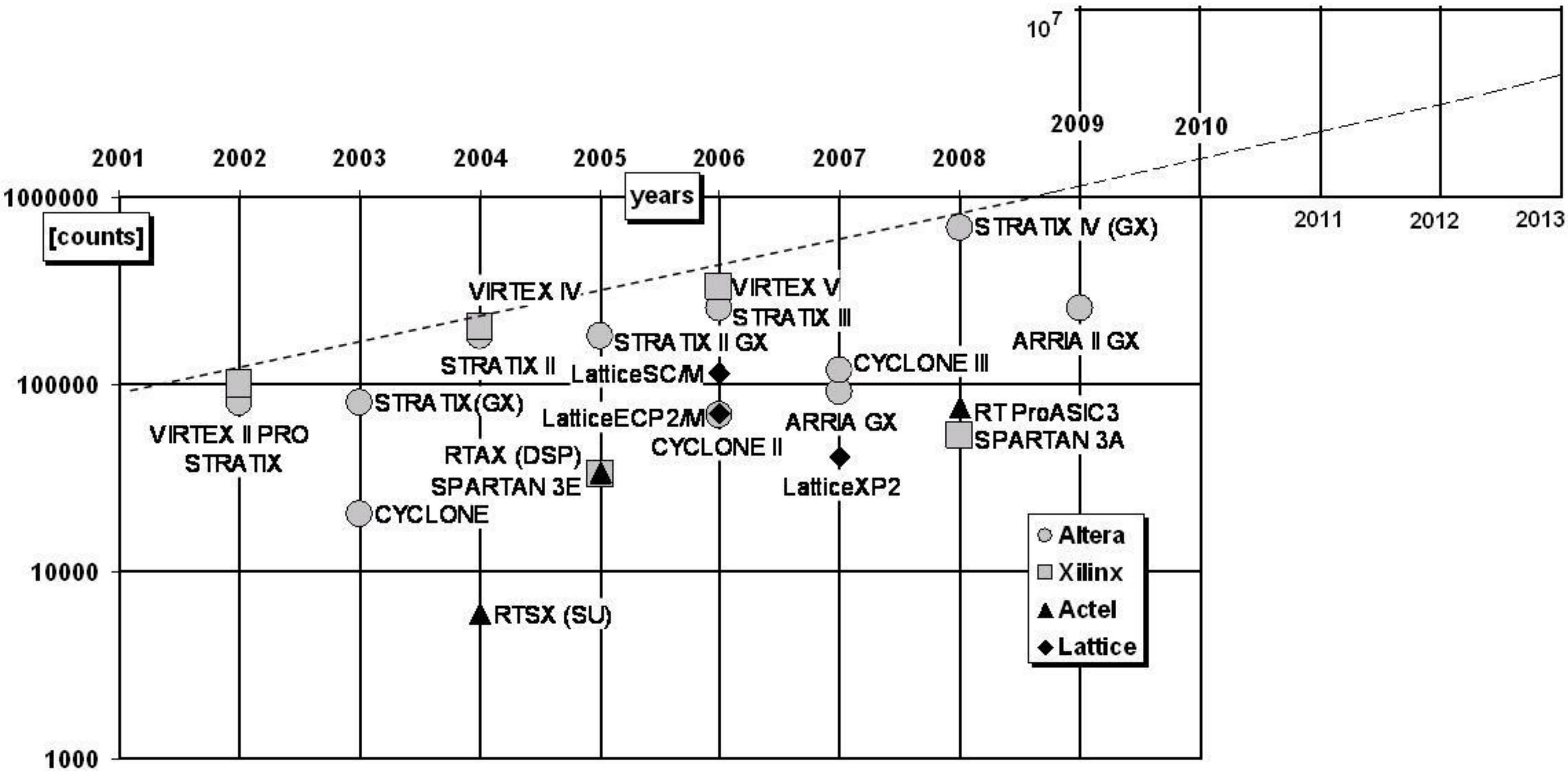
Number of measurements in time unit: **one hundred thousand** times

Rate of experimental data acquisition: **one thousand** times

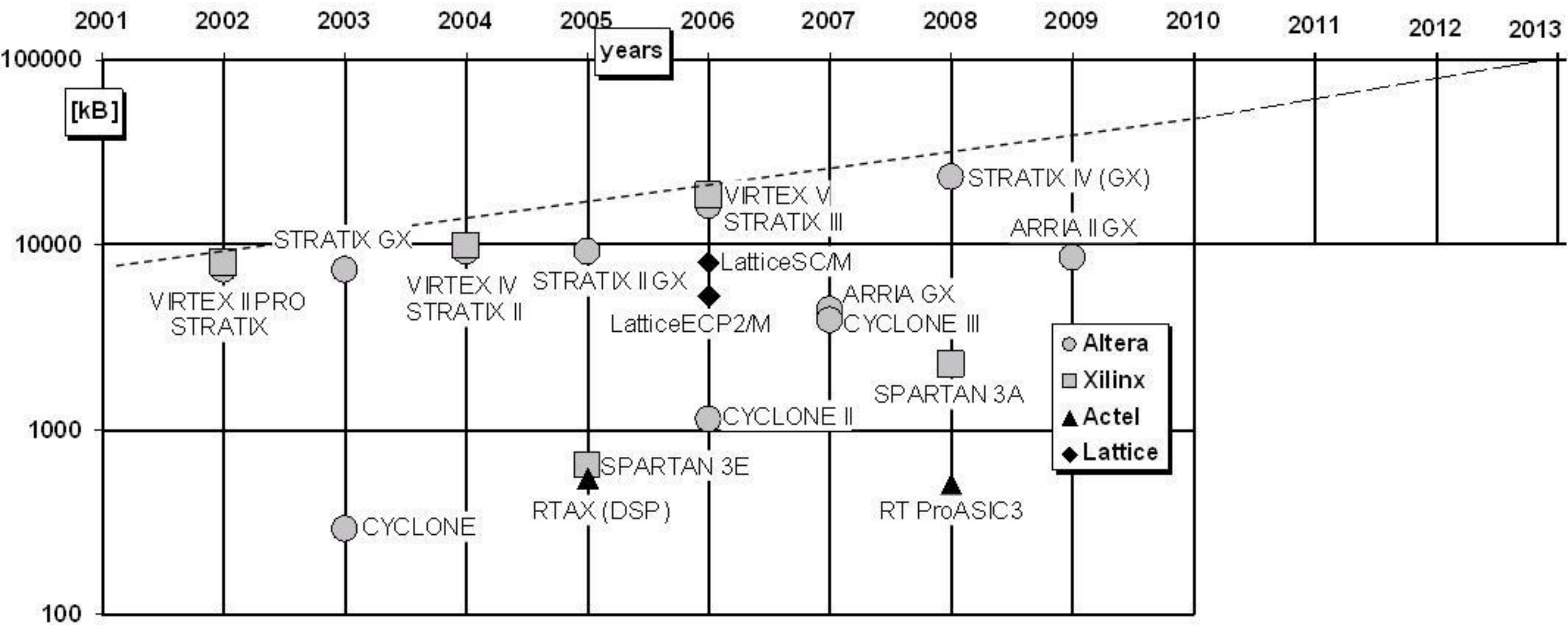
fpga circuit development: basic dimension



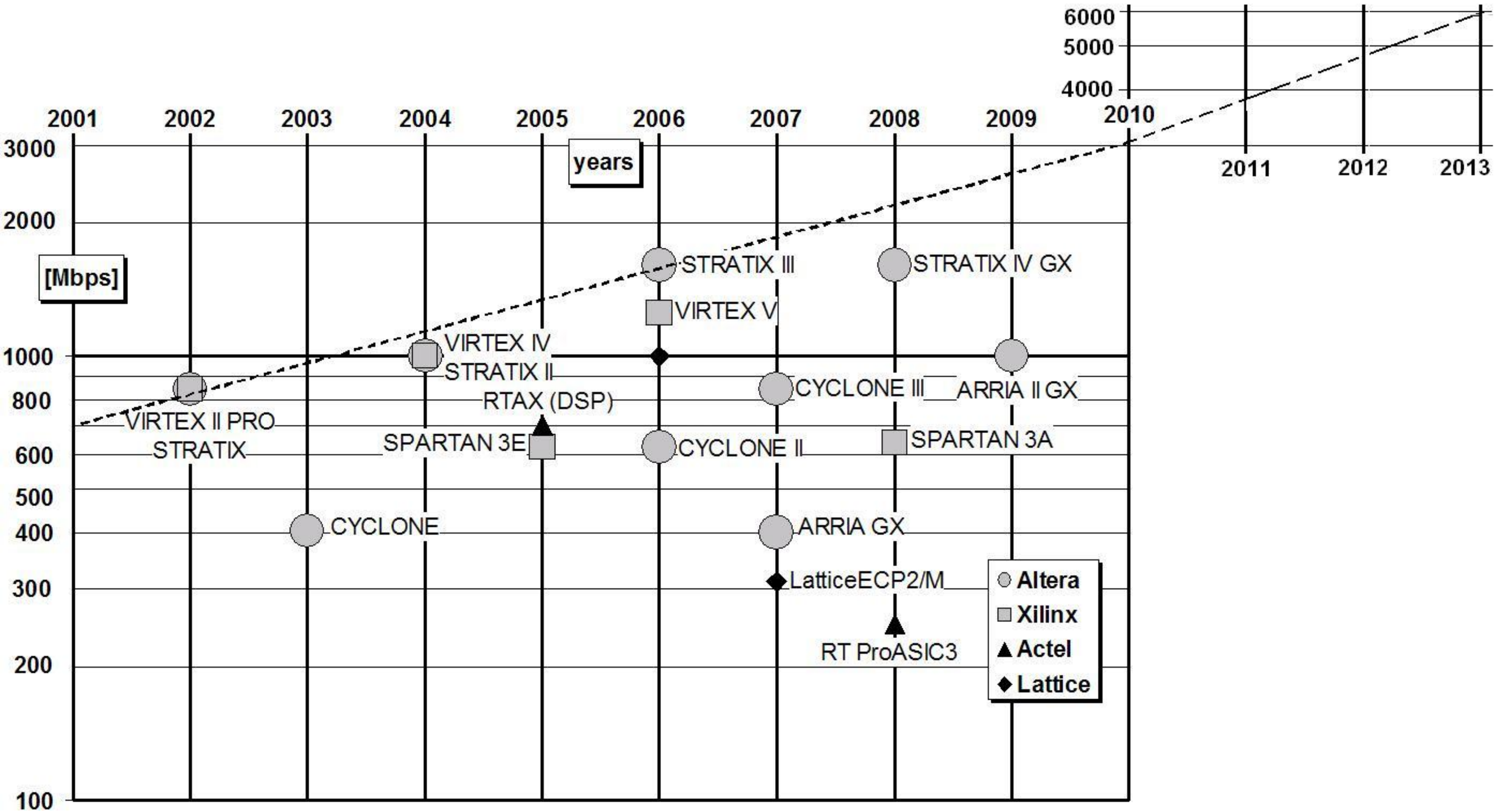
fpga development: LCELL number



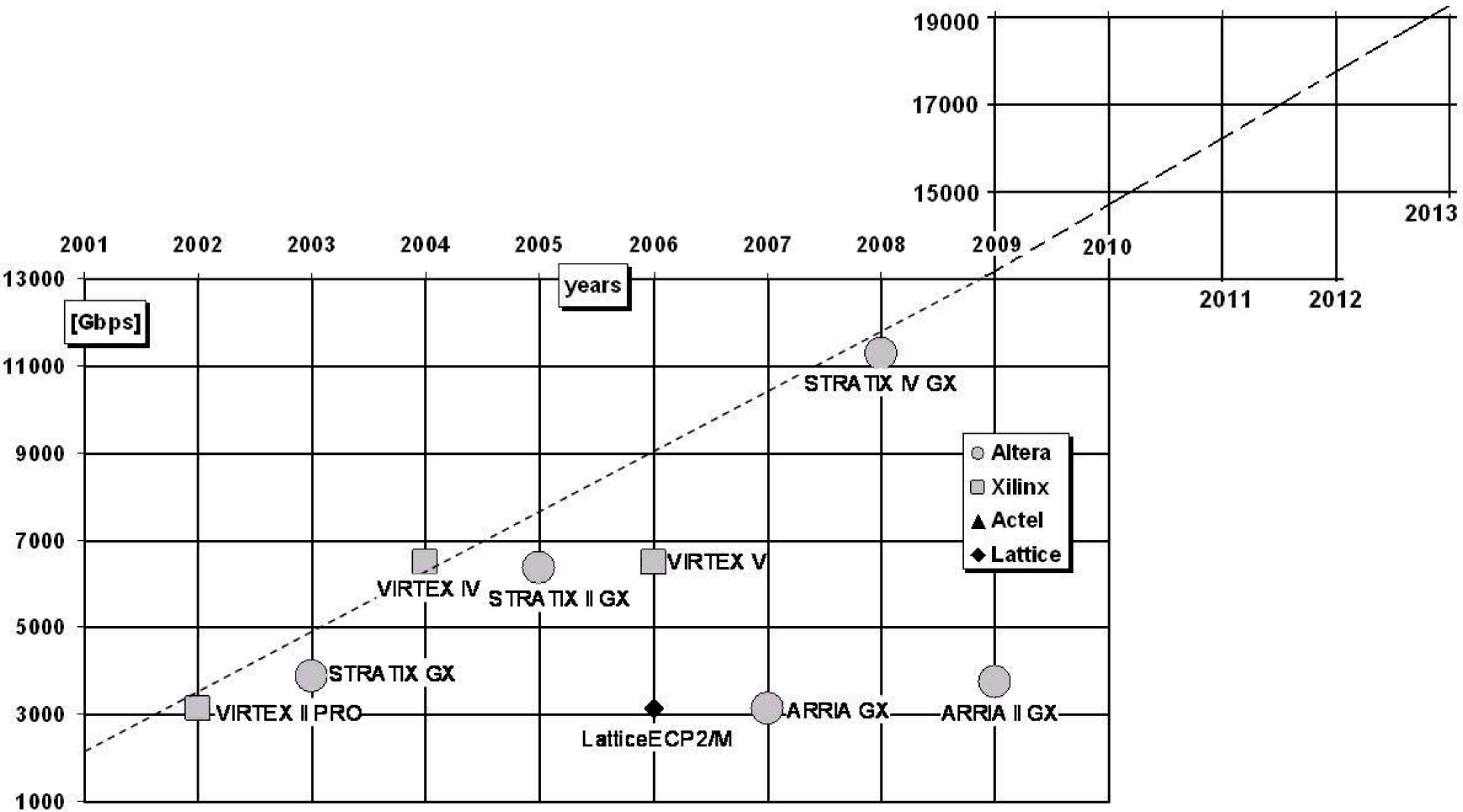
fpga development: SRAM capacity



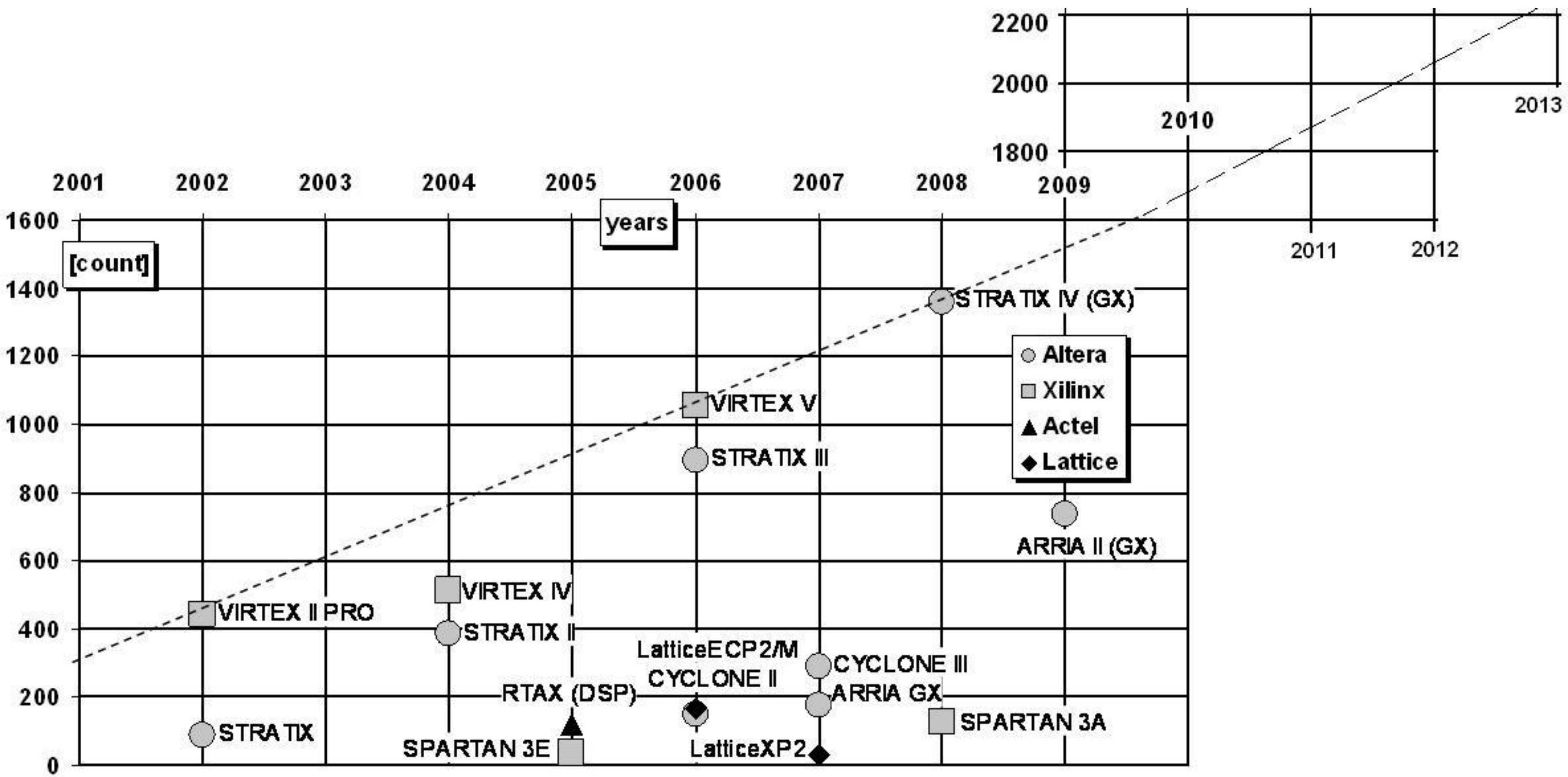
fpga development: I/O rate - LVDS



fpga development: I/O rate – serdes



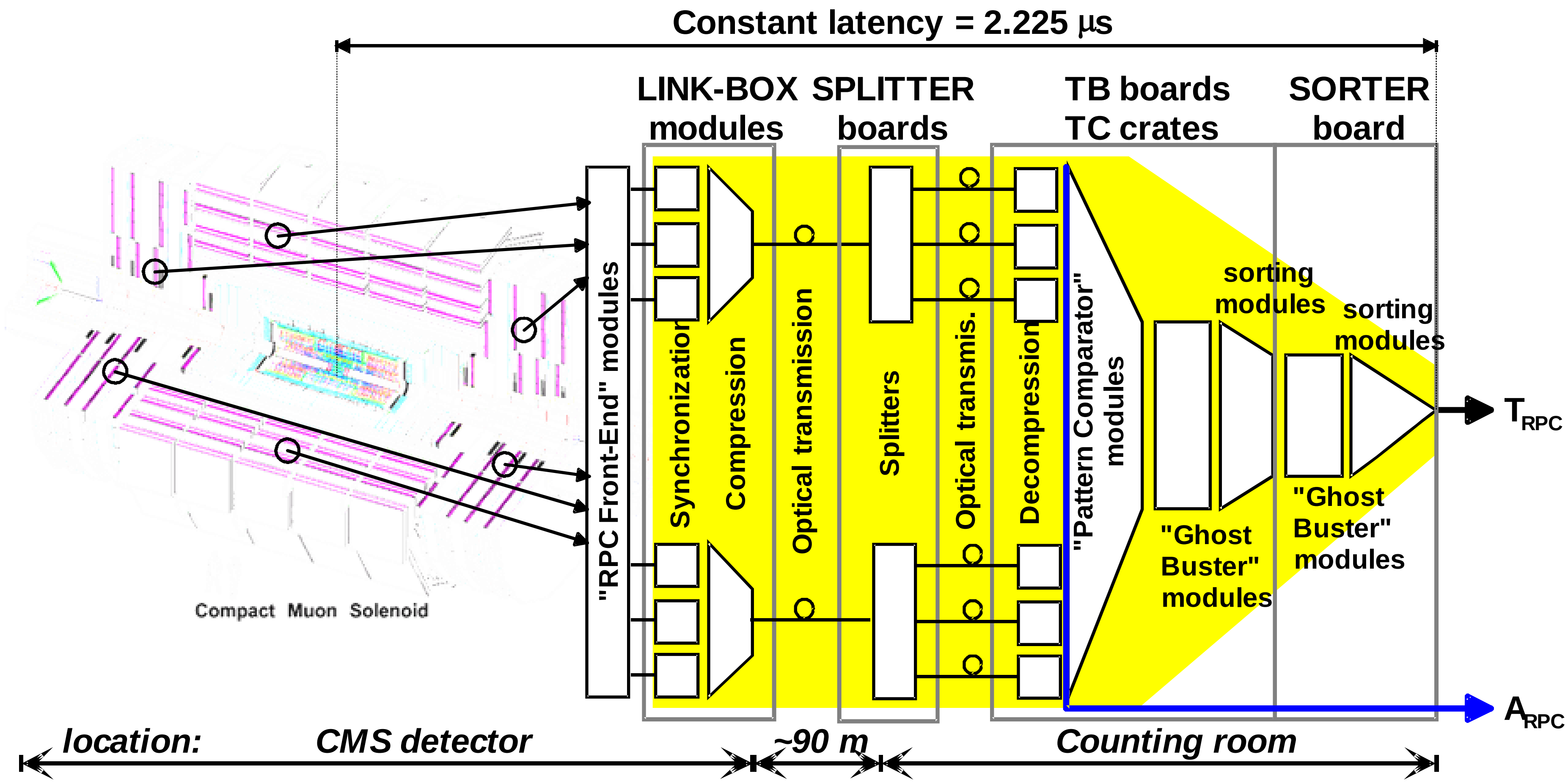
fpga development: multiplying units 18x18



fpga examples: xilinx

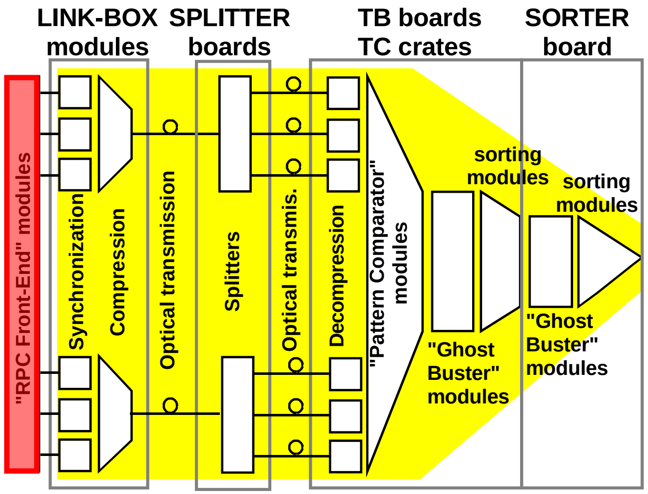
Features	Artix-7	Kintex-7	Virtex-7	Spartan-6	Virtex-6
Logic Cells	352,000	480,000	2,000,000	150,000	760,000
BlockRAM	19Mb	34Mb	68Mb	4.8Mb	38Mb
DSP Slices	1,040	1,920	3,600	180	2,016
DSP Performance (symmetric FIR)	1,248GMACS	2,845GMACS	5,335GMACS	140GMACS	2,419GMACS
Transceiver Count	16	32	96	8	72
Transceiver Speed	6.6Gb/s	12.5Gb/s	28.05Gb/s	3.2Gb/s	11.18Gb/s
Total Transceiver Bandwidth (full duplex)	211Gb/s	800Gb/s	2,784Gb/s	50Gb/s	536Gb/s
Memory Interface (DDR3)	1,066Mb/s	1,866Mb/s	1,866Mb/s	800Mb/s	1,066Mb/s
PCI Express® Interface	Gen2x4	Gen2x8	Gen3x8	Gen1x1	Gen2x8
Agile Mixed Signal (AMS)/XADC	Yes	Yes	Yes		Yes
Configuration AES	Yes	Yes	Yes	Yes	Yes
I/O Pins	600	500	1,200	576	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.5V, 1.8V, 2.5V
EasyPath Cost Reduction Solution	-	Yes	Yes	-	Yes

RPC Muon Trigger System overview

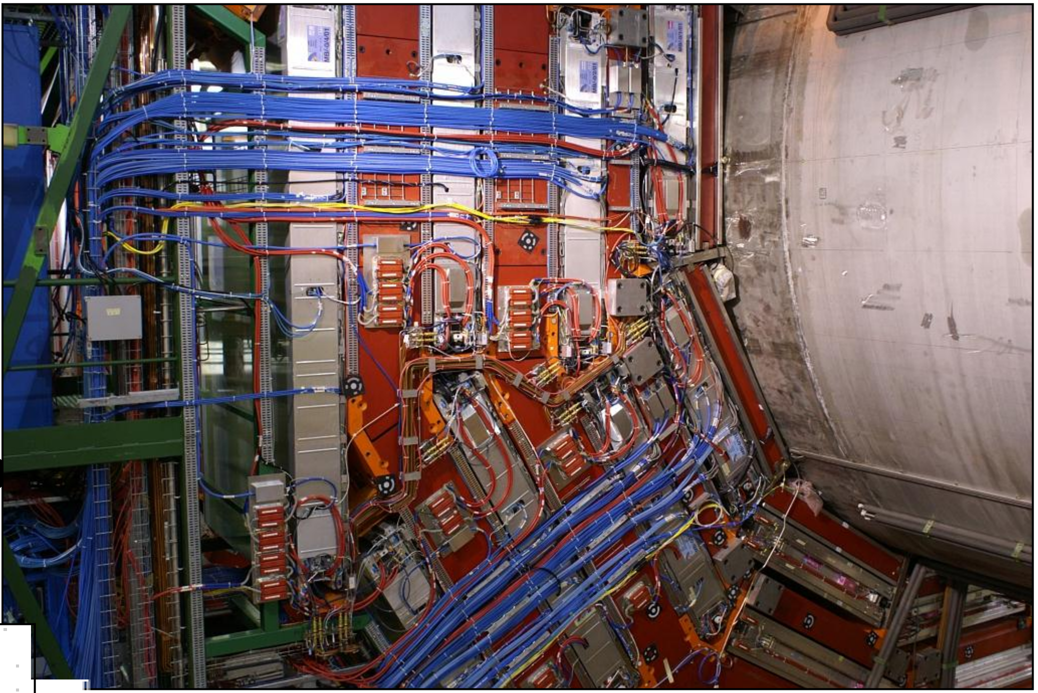


General functional and hardware system structure

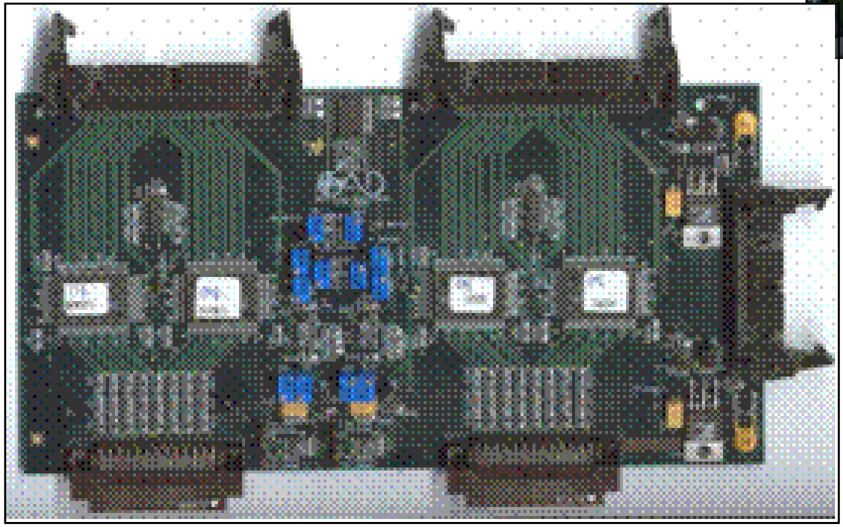
RPC Muon Trigger System overview



- **Input signals from RPC– 200000**
- **Front-End boards – 7200**

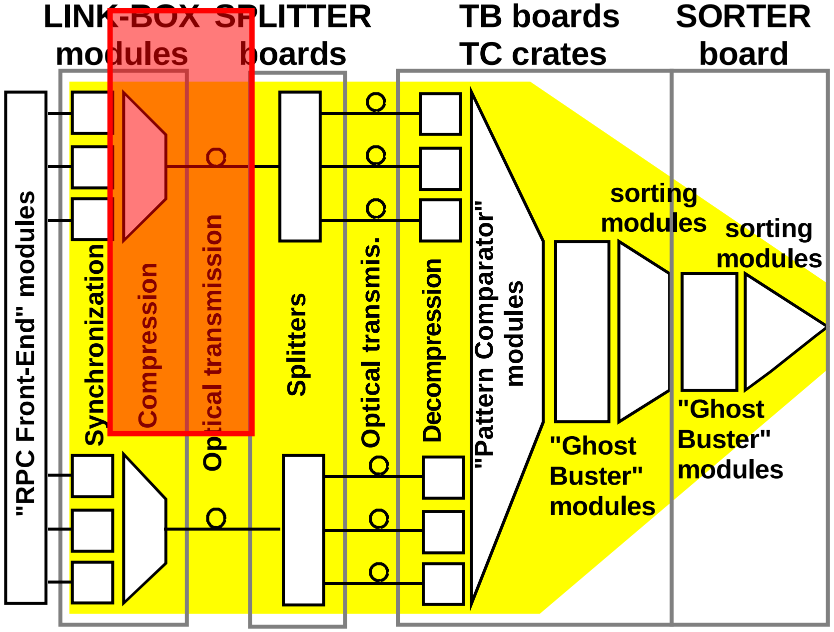


Inner part of CMS detector

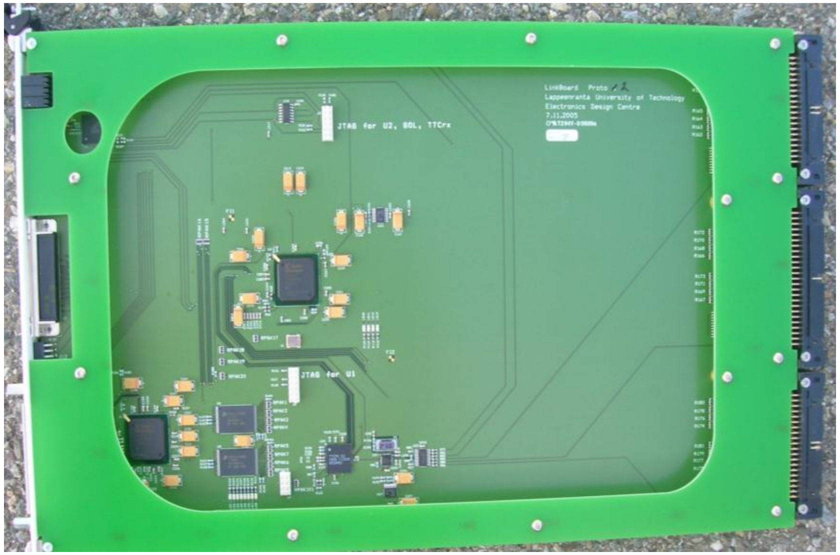


Front-end board

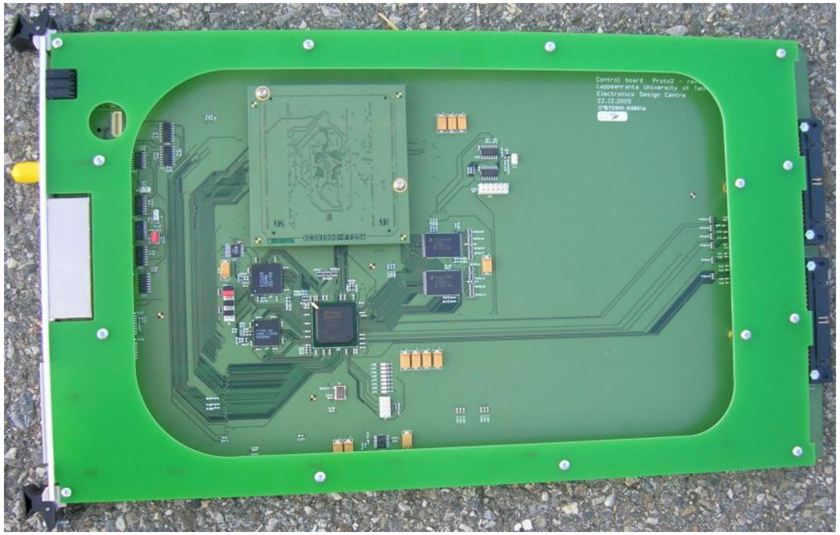
RPC Muon Trigger System overview



- Input signals from RPC – 200000
- Front-End boards – 7200
- Link Boxes – 96
  - Link Boards – 1200
  - Control Boards - 96
- Fibre Links – 444

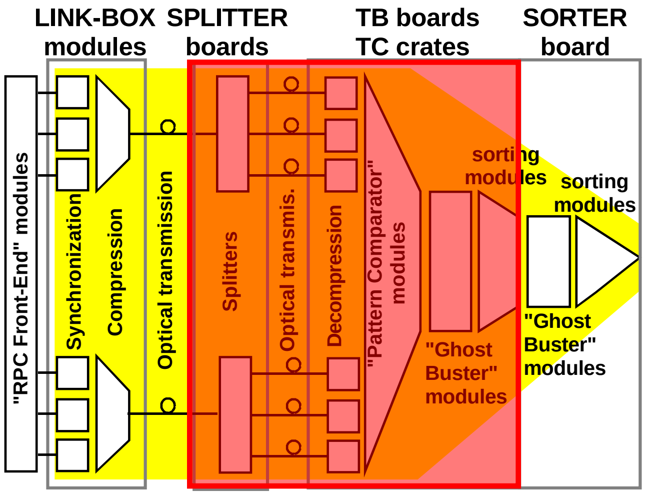


Link Board

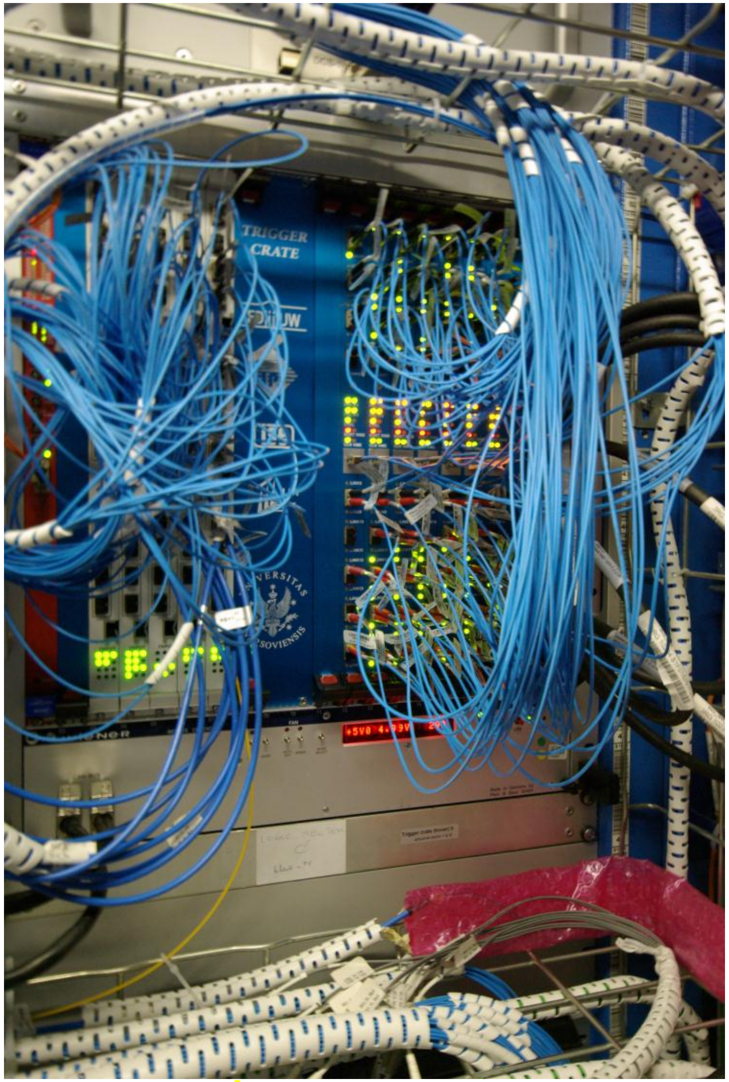


Control board (W.Zabolotny)

RPC Muon Trigger System overview

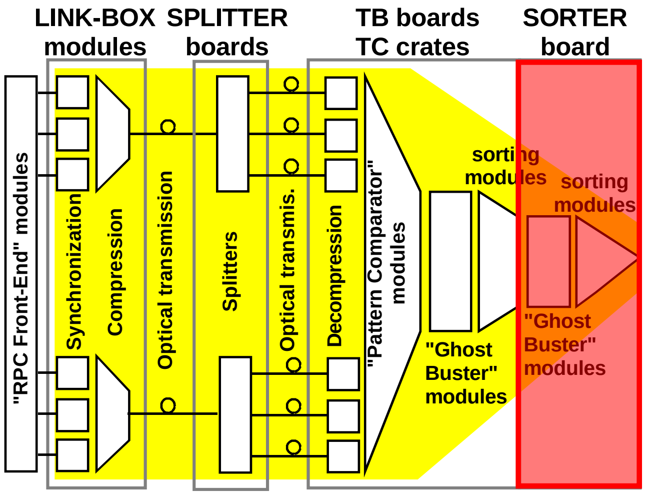


- Input signals from RPC – 200000
- Front-End boards – 7200
- Link Box – 96
  - Link Boards – 1200
  - Control Boards - 96
- Fibre Links – 444
- Splitter boards – 111
- Trigger Cassettes – 12
  - Trigger Boards – 86

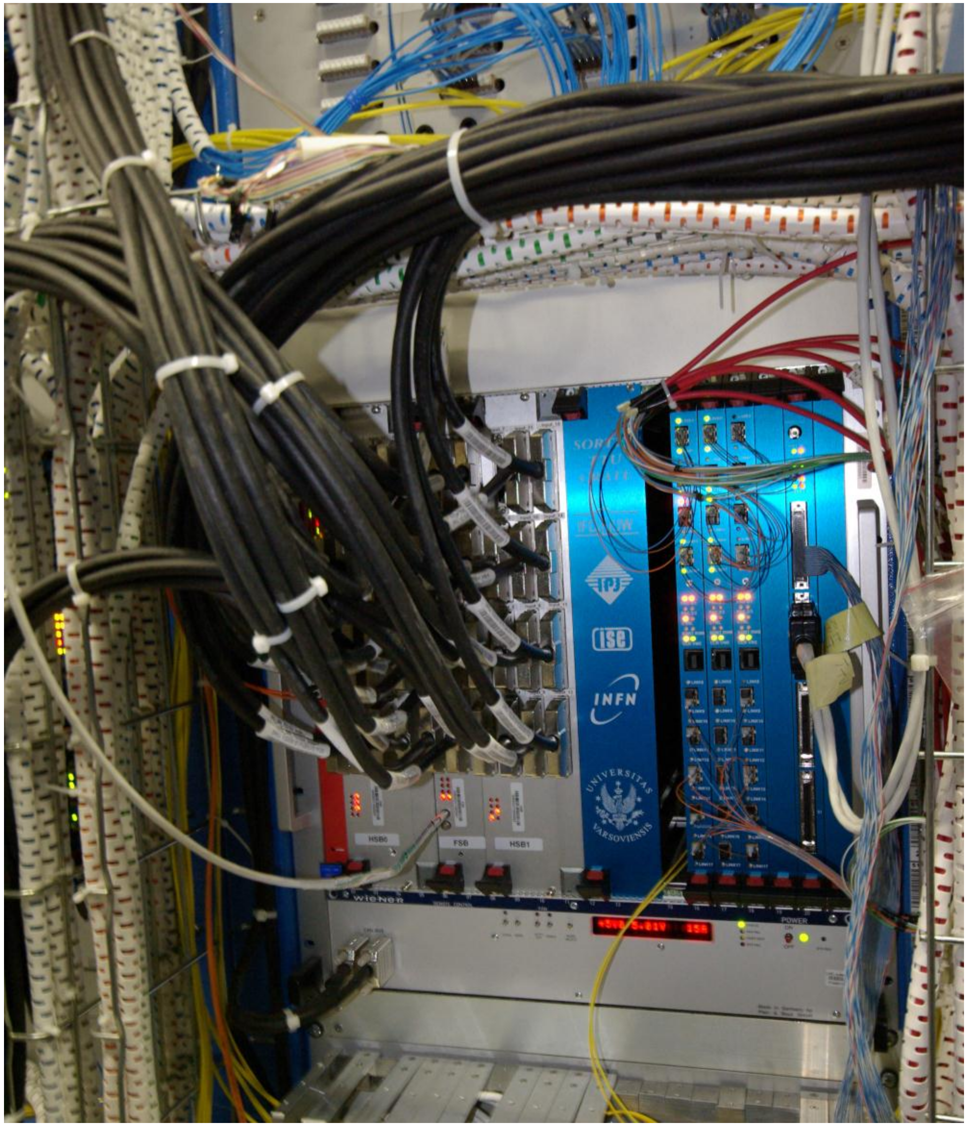


Trigger casette

RPC Muon Trigger System overview

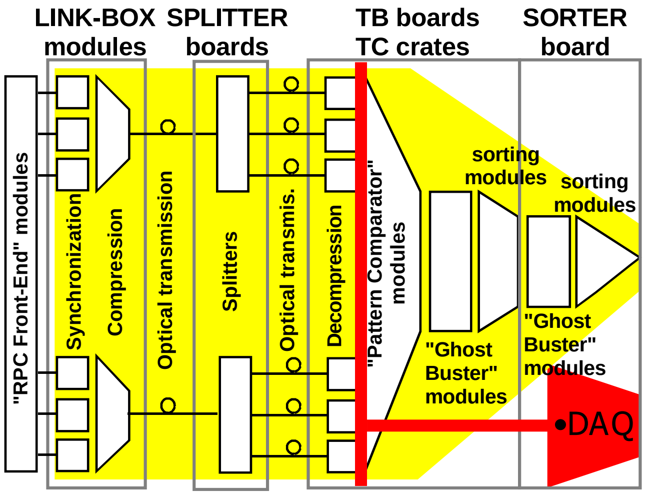


- Input signals from RPC – 200000
- Front-End boards – 7200
- Link Box – 96
  - Link Boards – 1200
  - Control Boards - 96
- Fibre Links – 444
- Splitter boards – 111
- Trigger Cassettes – 12
  - Trigger Boards – 86
- Sorting Cassette – 1
  - Sorting Boards – 3
- Output signals - 80

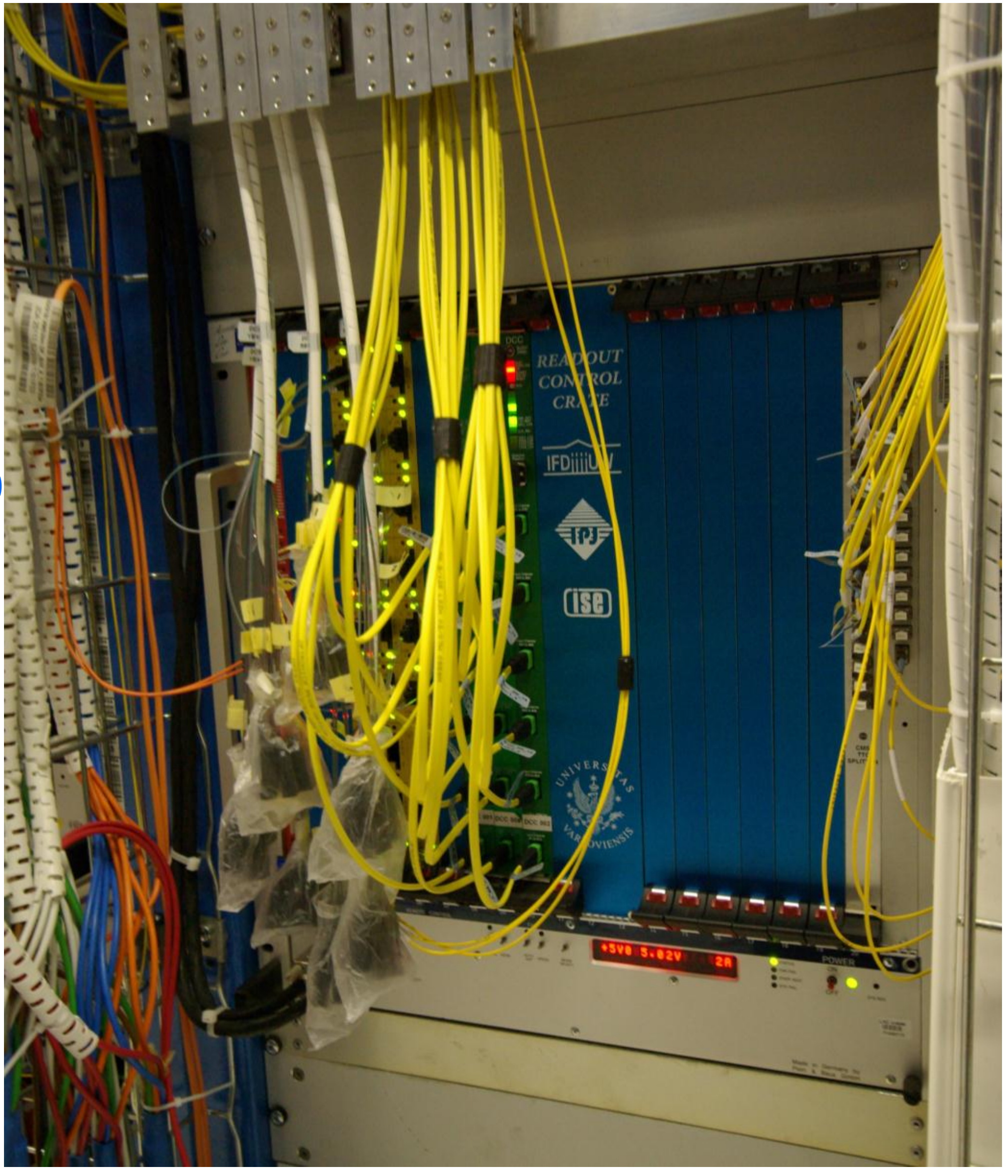


Sorter cassette

RPC Muon Trigger System overview

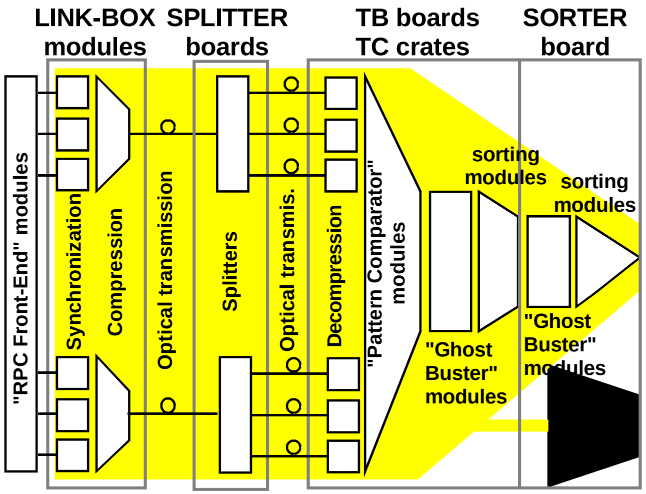


- Input signals from RPC – 200000
- Front-End boards – 7200
- Link Box – 96
  - Link Boards – 1200
  - Control Boards - 96
- Fibre Links – 444
- Splitter boards – 111
- Trigger Cassettes – 12
  - Trigger Boards – 86
- Sorting Cassette – 1
  - Sorting Boards – 3
- Output signals - 80
- Readout Cassete - 1
  - DAQ boars - 4

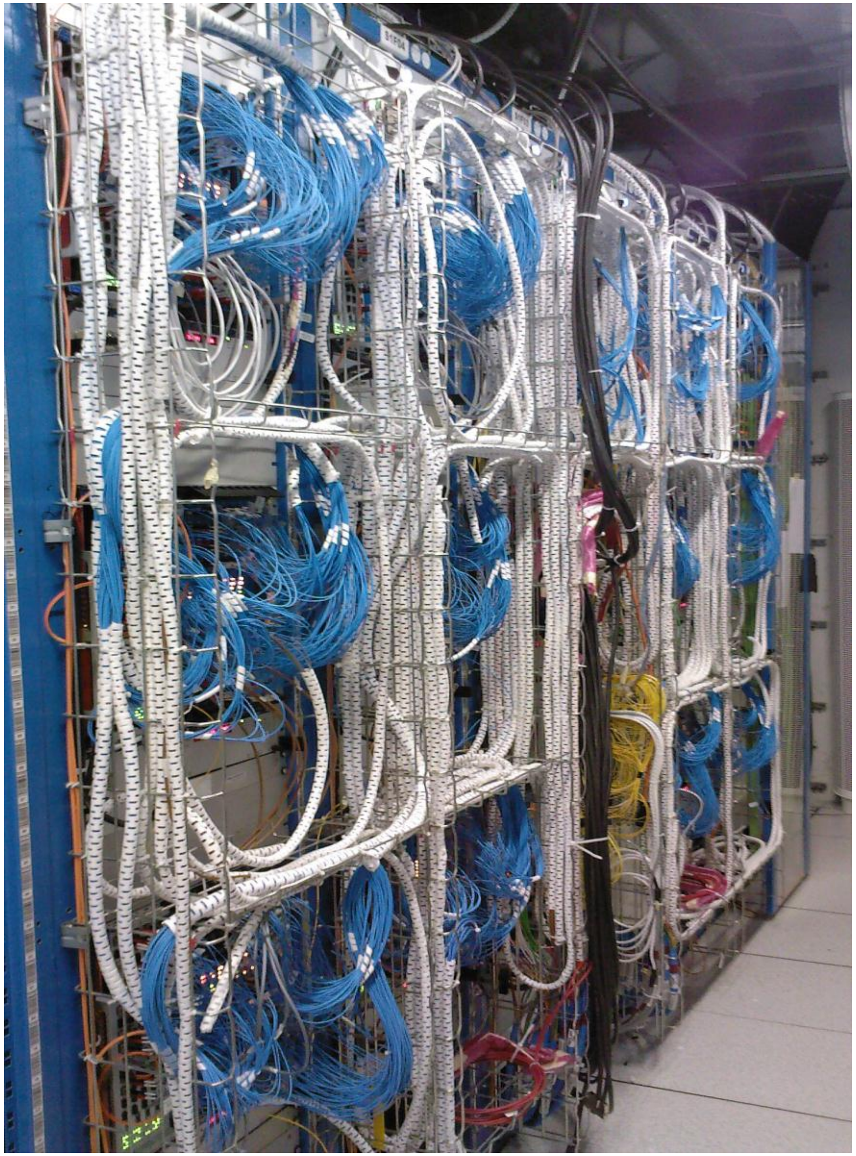


Readout cassette (W Zabolotny)

RPC Muon Trigger System overview

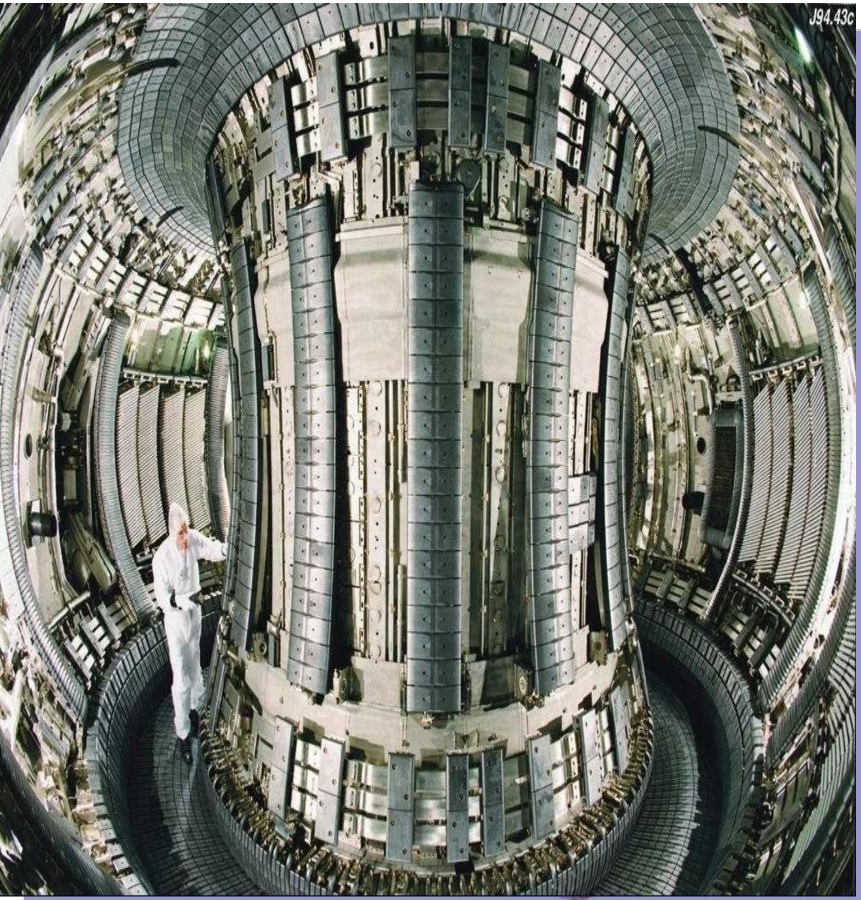


• Input signals from RPC		–
200000 FPGAs		
• Front-End boards	– 7200	
• Link Box	– 96	
– Link Boards	– 1200	2400
– Control Boards	- 96	288
• Fibre Links	– 444	
• Splitter boards	– 111	
• Trigger Cassettes	– 12	
– Trigger Boards	– 86	1232
• Sorting Cassette	– 1	
– Sorting Boards	– 3	6
• Output signals	- 80	
• Readout Cassete	- 1	
– DAQ boars	- 4	24



RPC Trigger crates

Joint European Torus (JET)



1973 – building decision
1983 – first experiments

Basic parmeters:

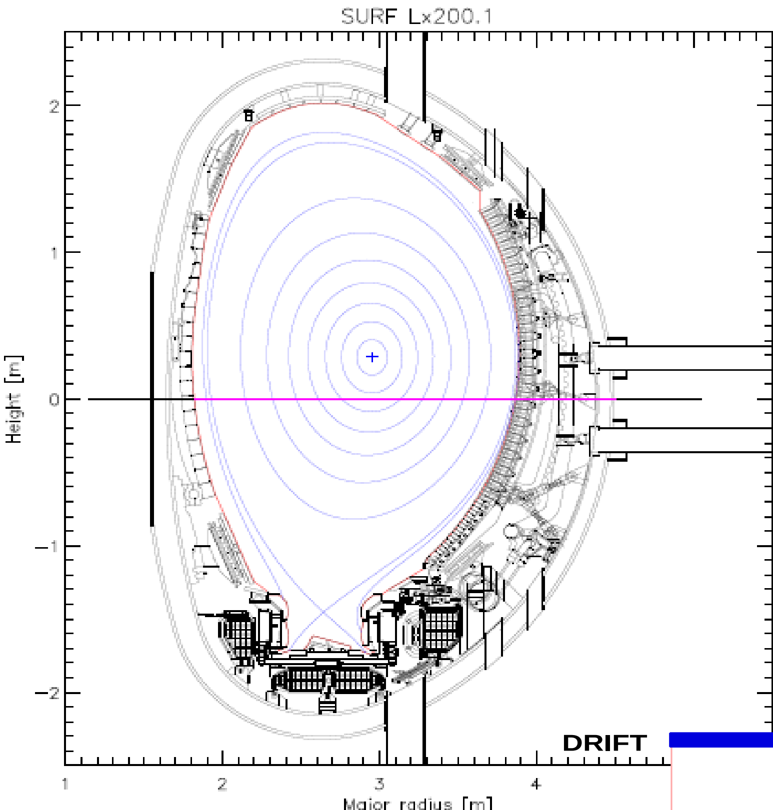
- Torus radius:…..3.1 m
- Chamber:…H=3.96 m x S=2.4 m
- Plasma volume:…80 m^3
- Plasma current:….up to 5 MA
- Magnetic field: up to 4 T

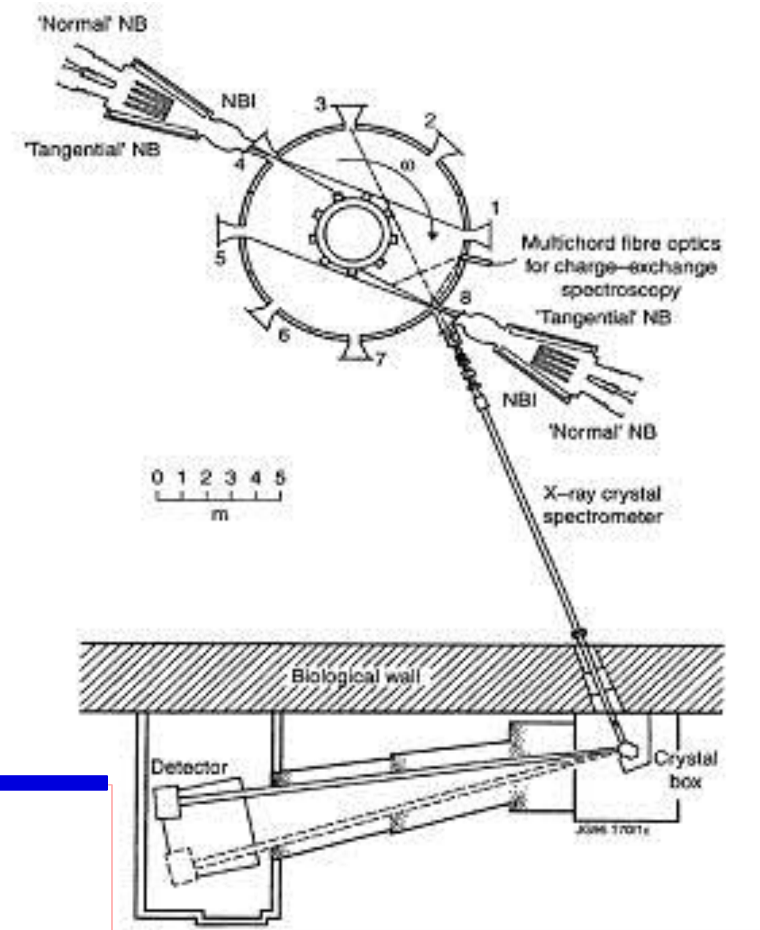
JET achievements:

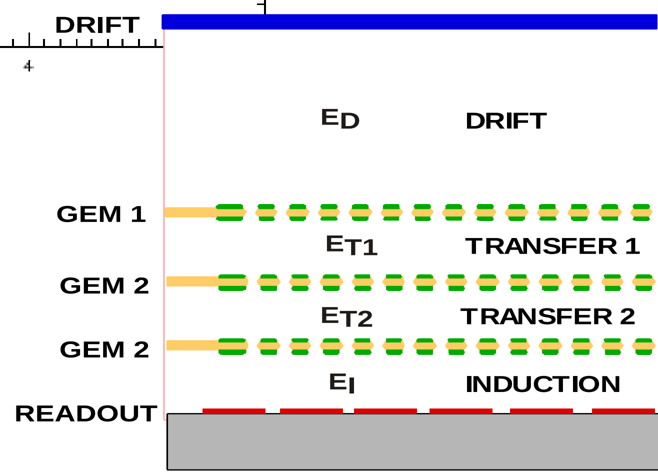
- 1991: controlled D+T fusion, ~2MW 1s
- 1997: fusion power 16MW at 75% efficiency

EFDA – European Fusion Development Agreement

JET plasma diagnostics

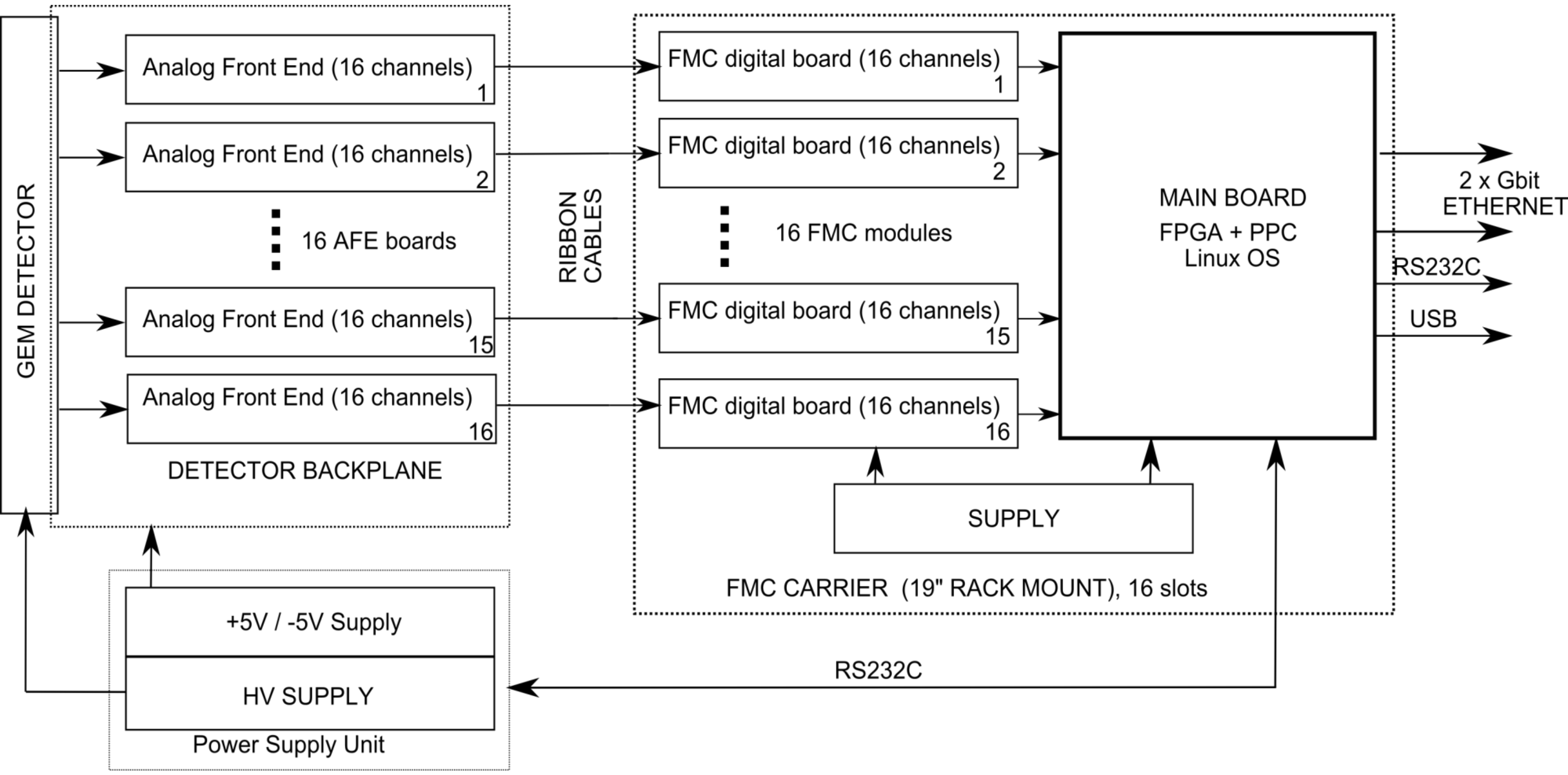






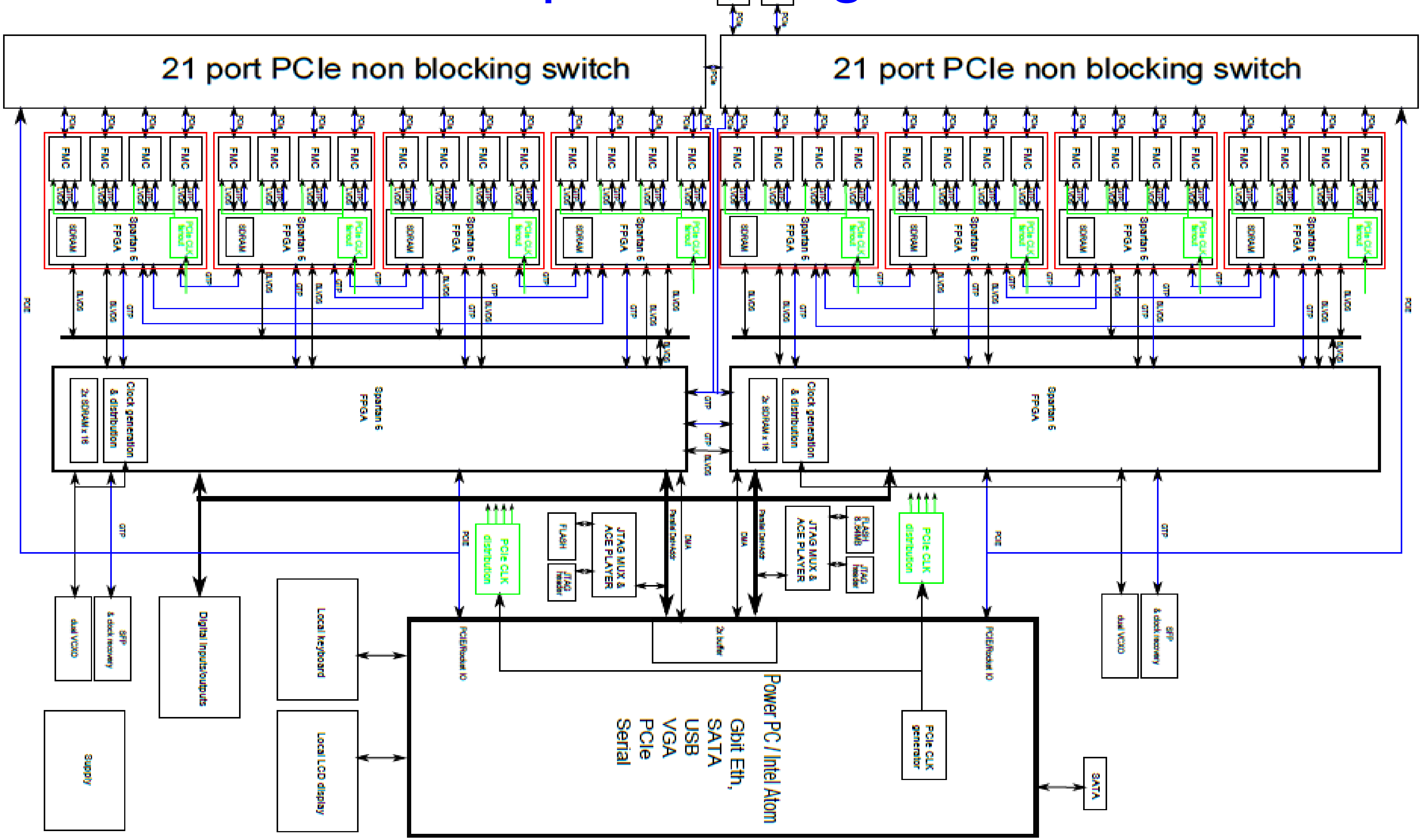
GEM detector – Gas Electron Multiplier

GEM electronics overview



256 (512) channels x 100MHz x 10bit = 256 (512) Gbit/s data stream for complete system.
This stream needs to be analysed in real time.

FMC-based processing electronics



Innovative FMC-based modular structure
Very low latency, fast parallel connection
Central CPU for algorithms and system control

Extensible architecture (i.e. DSP, processing, communication modules) Automatic, self-testing and real-time diagnostic system

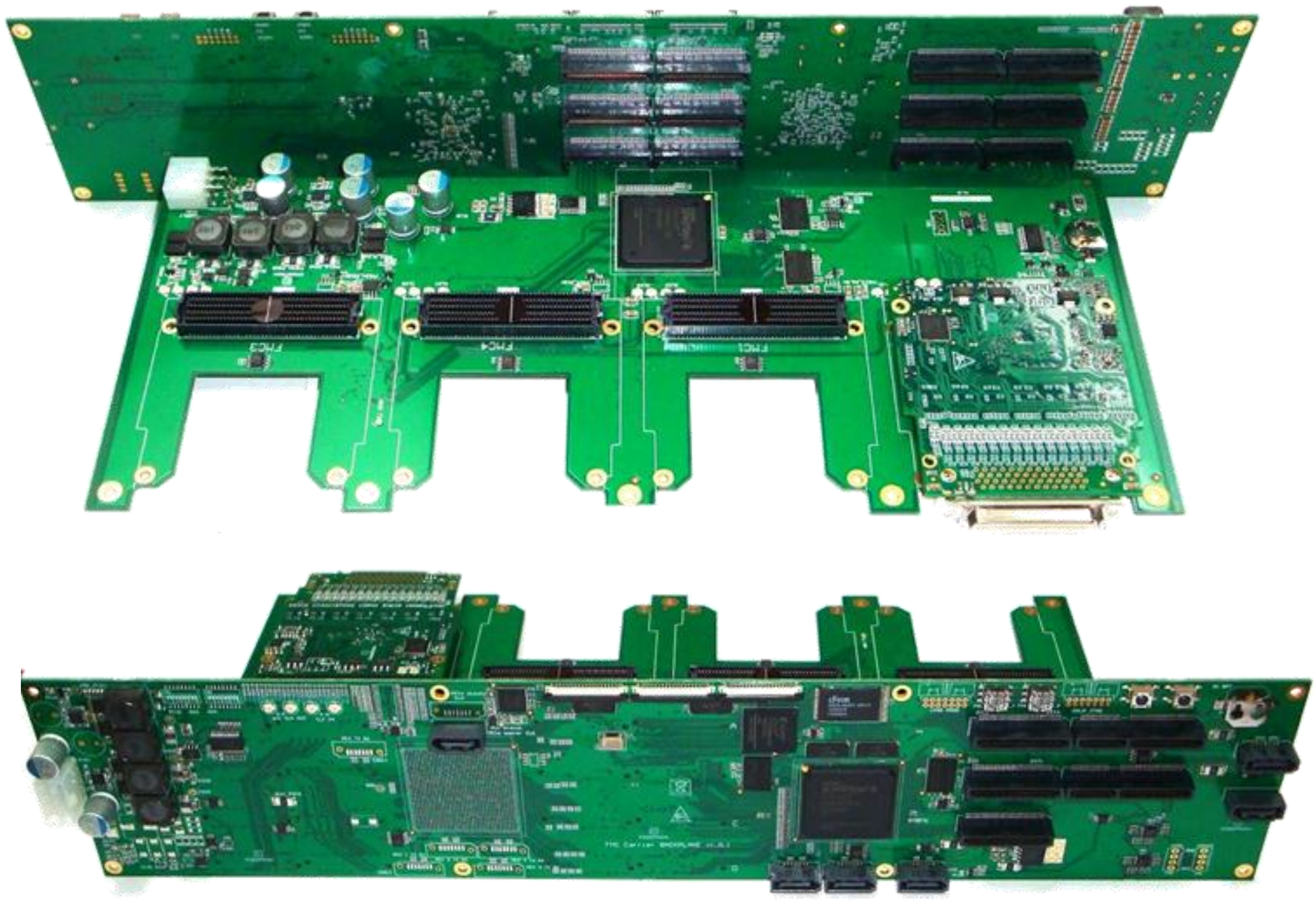
final digital crate – FMC carrier

Front view

final digital crate – FMC carrier

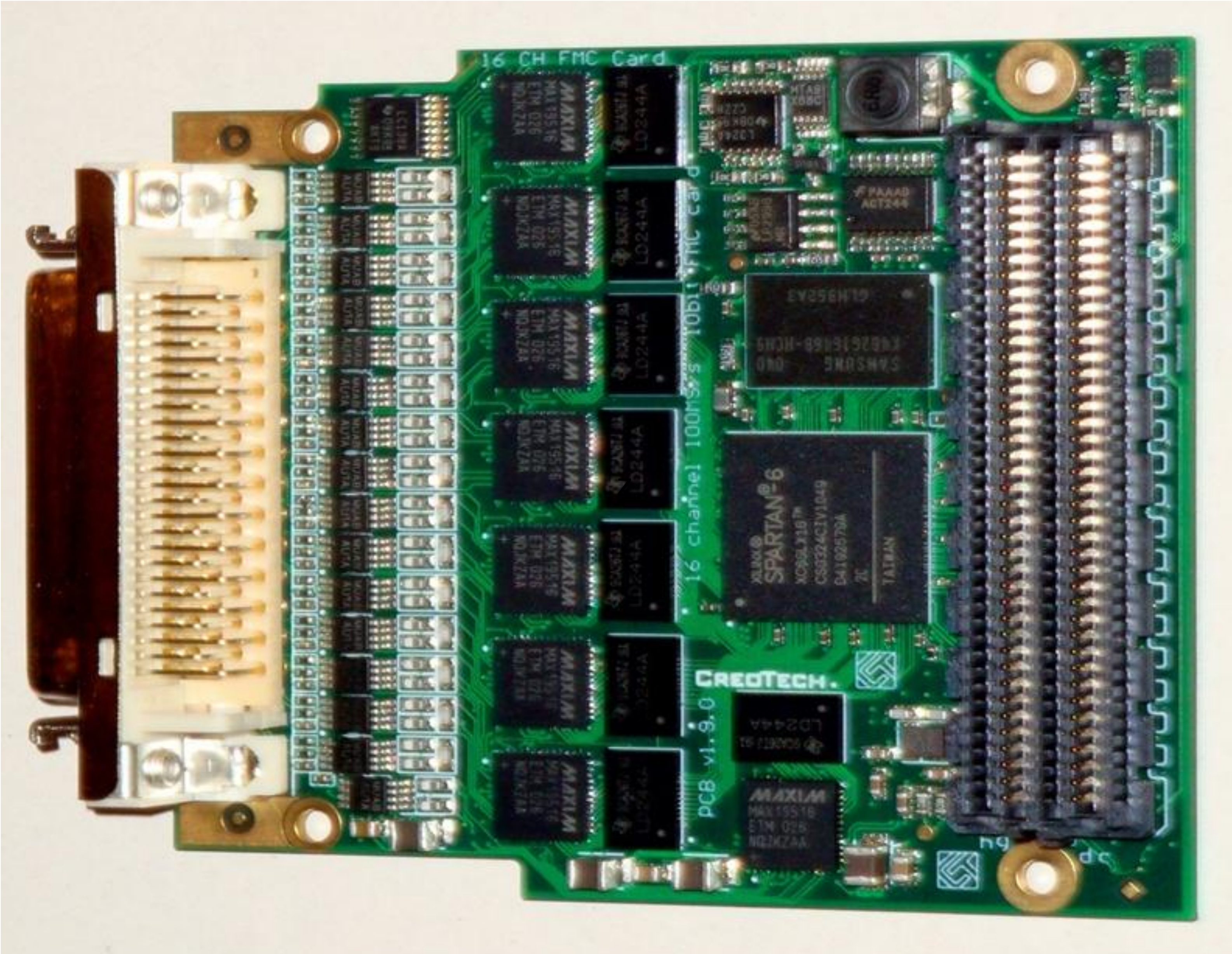
Details of the construction

final digital crate – FMC carrier



Details of the construction

FMC module final design



Gamma Ray Bursts (GRB)

Originate from point sources in the sky:

- energy:……….up to 10 mld years of Sun work
- time:…0.01-100 s
- distance:…….up to 13 mld light years
- frequency:……..2-3 times a day
- spectrum of photons: …..from IR to ~GeV

-discovered by US spy satellites Vela in 1967

Causes: hipernova, neutron star merging

π of the Sky – new method of GRB search

Inspiration – the late prof. B. Paczyński (Stanford Uni.)

New measurement strategy:

– continuous wide-field observations

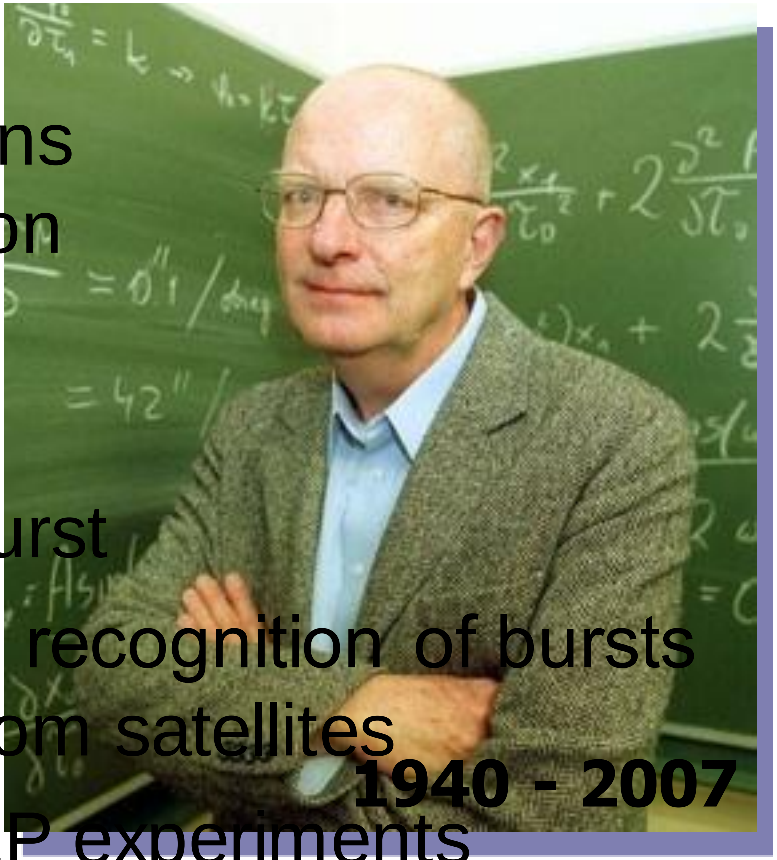
➜ observation of the burst position in negative time

– large time resolution

➜ comparable with time of the burst

– proprietary algorithm of “on-line” recognition of bursts

➜ identification nondependent from satellites



– approach borrowed from the HEP experiments

π of the Sky – detector

– usage of commercial photographic lenses
➜ large field of view, low costs

– sensitive CCD and low-noise analog electronics
➜ long range and large time resolution ~10s

– 2 sets of 16 cameras, monitoring ~2sr
➜ large probability to discover a burst in the field of view
➜ paralakis: removal of satellite background

– dedicated paralactic mount
➜ very fast aiming at the burst, and precise tracking

– reliability and fully robotic and autonomous work
➜ system works non-stop, without human participation

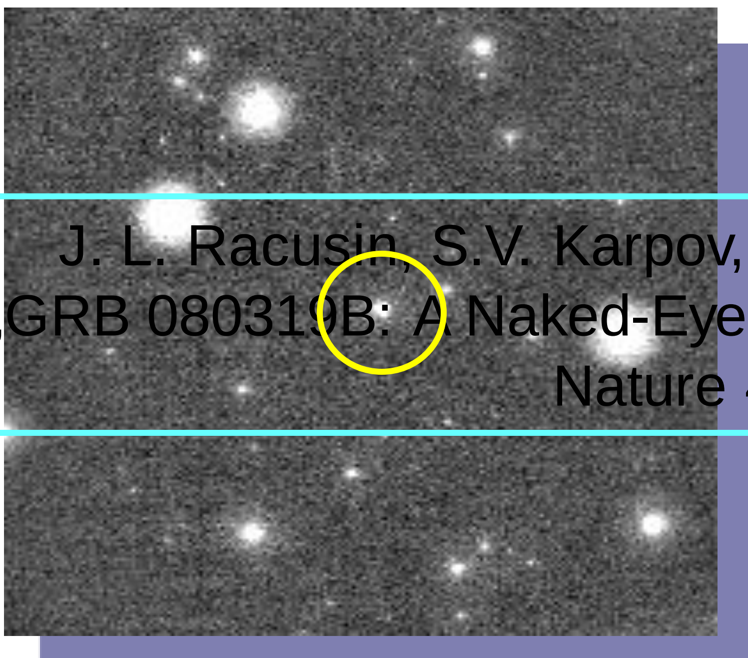
π of the Sky – observatories

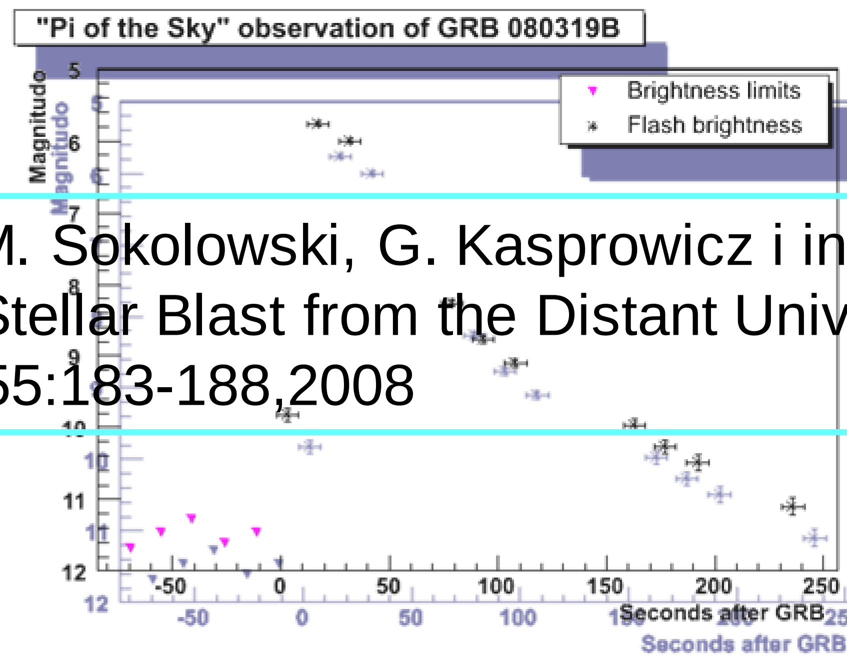
Prototype installed in Las Campanas Observatory, Chile, VI 2004 :

- 2 cameras CCD 2000×2000 pixels
- Cannon lenses f=85mm
- common field of view 20°×20°
- 10 s expositions, magnitudo ~11^m for a single image, and up to 13^m for added 20 images
- fully automatic work and diagnostics
- management over the Internet

π of the Sky – GRB 080319B

- GRB in Wolarz Constellation
- Discovered by Swift satellite at 6:12 UTC, 19.03.2008
- Generated 7,5 mld light years from the Earth
- ~2,5 milion times brighter than supernova
- Burst magnitudo $5{,}8^m$
- Burst time ~ 30 s





J. L. Racusin, S.V. Karpov, M. Sokolowski, G. Kasprowicz i inni:
„GRB 080319B: A Naked-Eye Stellar Blast from the Distant Universe”
Nature 455:183-188,2008

SMP 3v0 - Introduction

Safe Machine Parameters

receives accelerator information

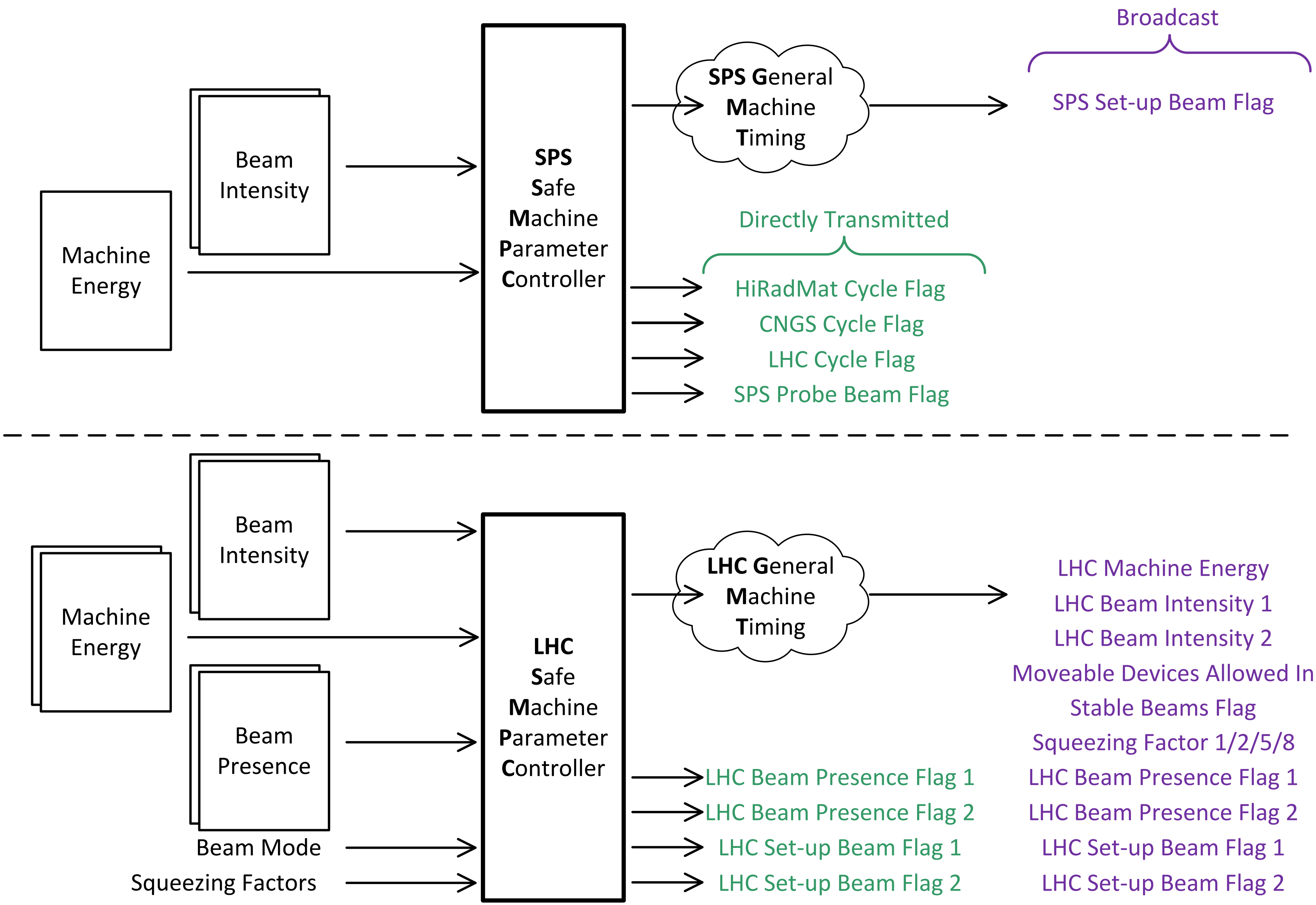
generates flags & values

directly transmitted and / or broadcast

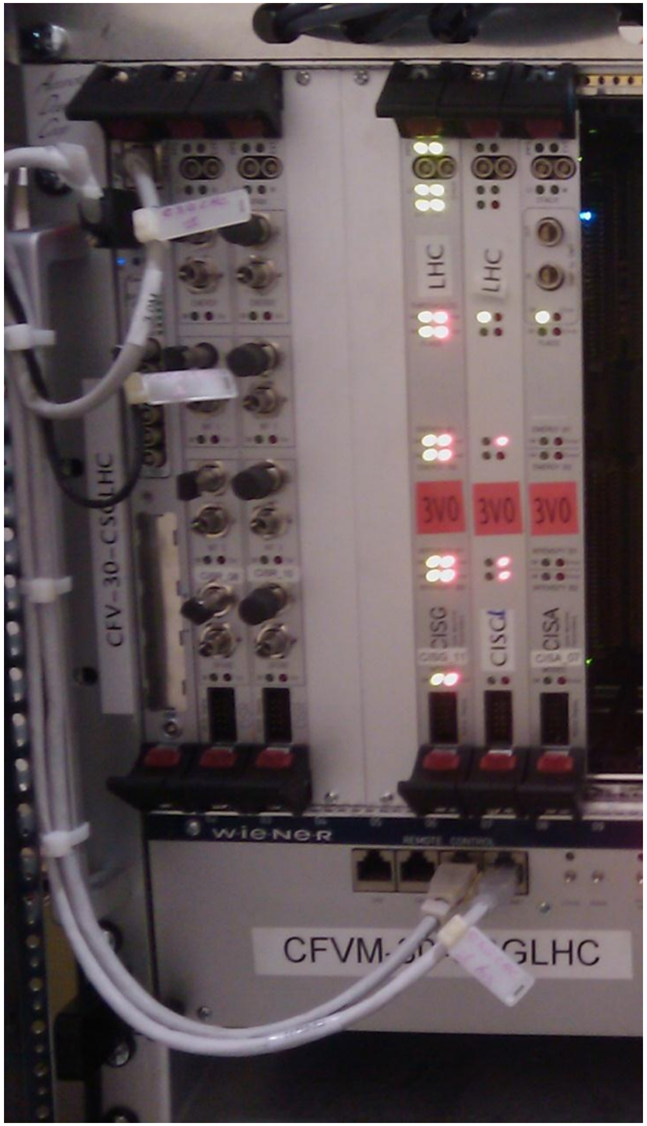
injection procedure
Extraction Interlocks

protection configuration
Beam Interlocks
Collimation
Beam Loss Monitors …

Two Controllers



VME Chassis & Generic Circuit - CISX

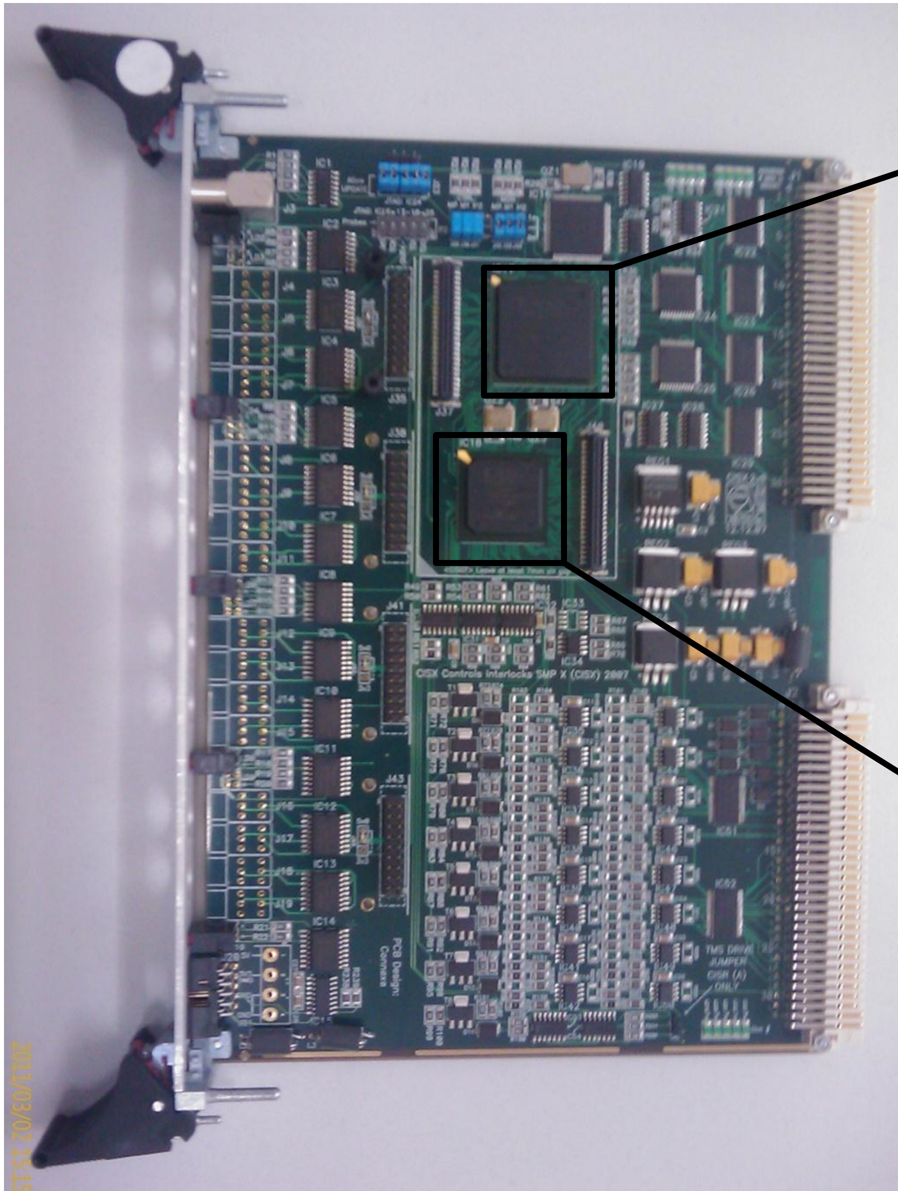


Receiver

Generator LHC
or
Generator SPS

Arbiter

VME Chassis & Generic Circuit - CISX



Monitor FPGA

Receiver – CISR

Generator LHC – CISGL

Generator SPS – CISGS

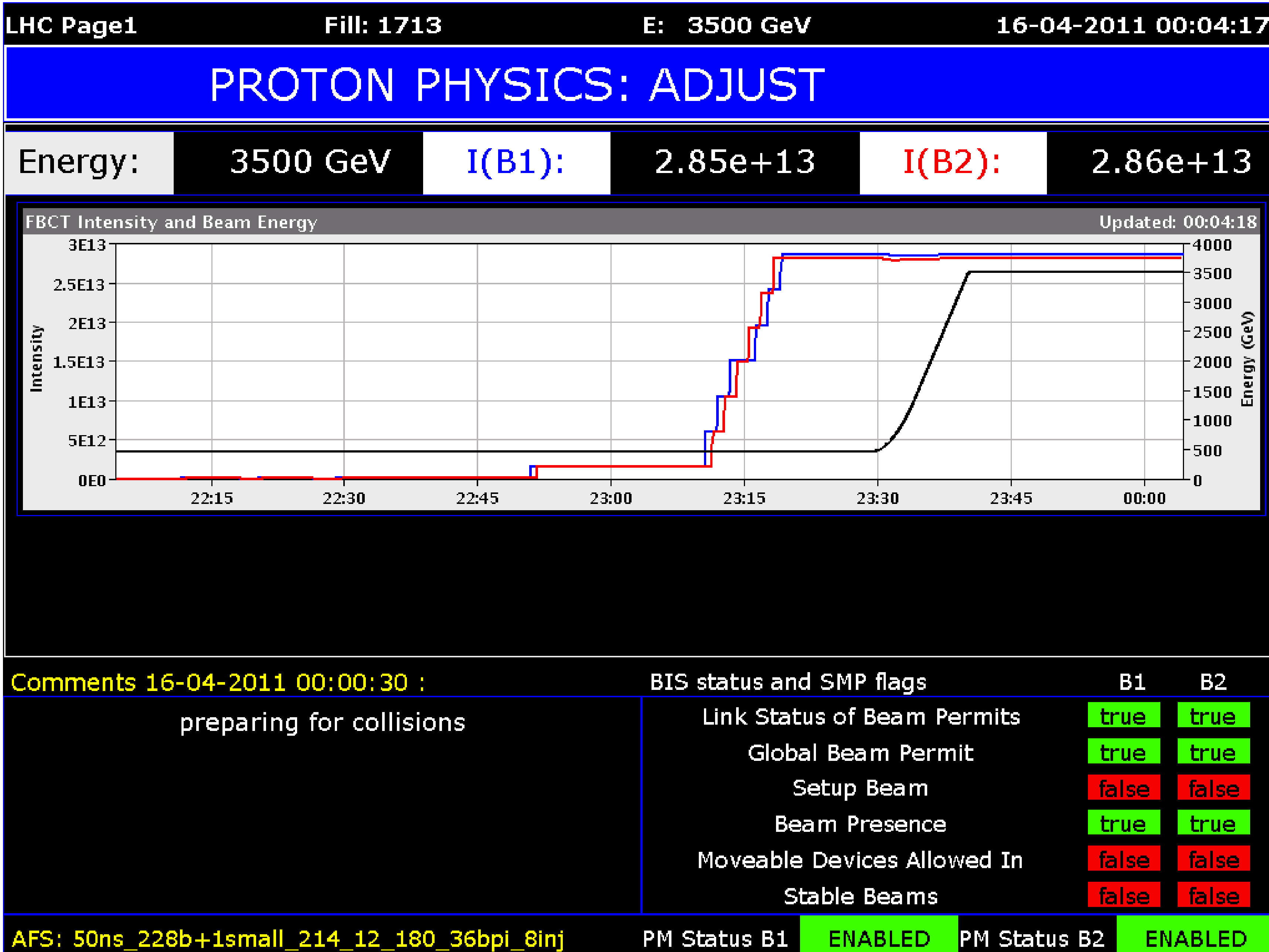
Arbiter – CISA

Control FPGA

VHDL implementation

Safety approach?

LHC page 1



LHC Page1
Fill: 1713
E: 3500 GeV
16-04-2011 00:04:17
PROTON PHYSICS: ADJUST
Energy:
3500 GeV
I(B1):
2.85e+13
I(B2):
2.86e+13
FBCT Intensity and Beam Energy
Updated: 00:04:18
Intensity
Energy (GeV)
3E13
2.5E13
2E13
1.5E13
1E13
5E12
0E0
4000
3500
3000
2500
2000
1500
1000
500
0
22:15
22:30
22:45
23:00
23:15
23:30
23:45
00:00
Comments 16-04-2011 00:00:30 :
preparing for collisions
BIS status and SMP flags
B1
B2
Link Status of Beam Permits true true
Global Beam Permit true true
Setup Beam false false
Beam Presence true true
Moveable Devices Allowed In false false
Stable Beams false false
AFS: 50ns_228b+1small_214_12_180_36bpi_8inj
PM Status B1 ENABLED
PM Status B2 ENABLED

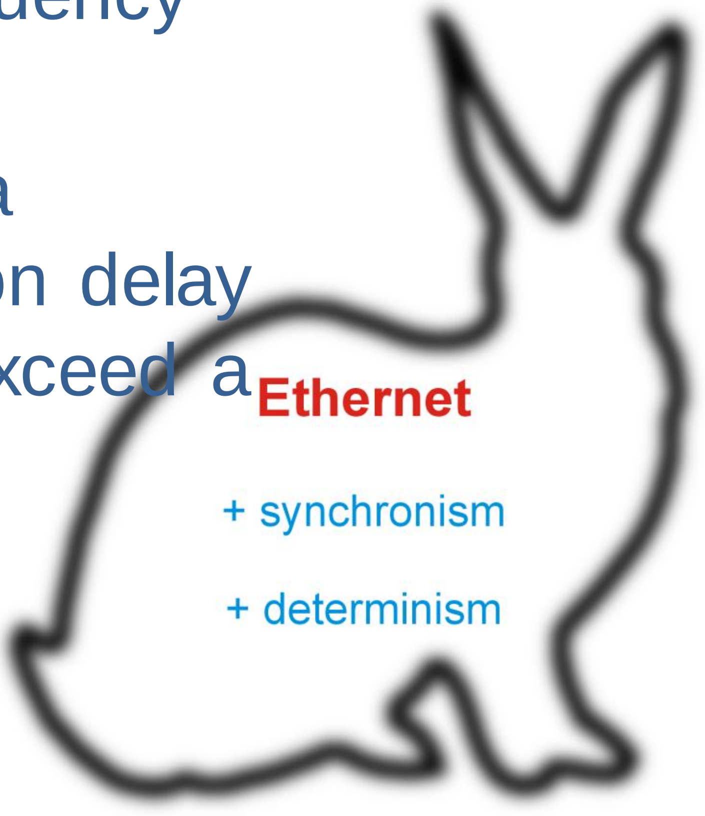
White Rabbit

- Accelerator's control and timing system (CERN, GSI)
- Based on well-known technologies/standards (Ethernet, IEEE1588, SyncE)
- Open Hardware and Open Software, commercially available
- International collaboration
- Main features:
  - Transparent, **high-accuracy** time distribution,
  - Low-latency, **deterministic** data delivery
  - Designed for **high reliability**
  - Plug & Play

What is White Rabbit ?

An **extension** to **Ethernet** which provides:

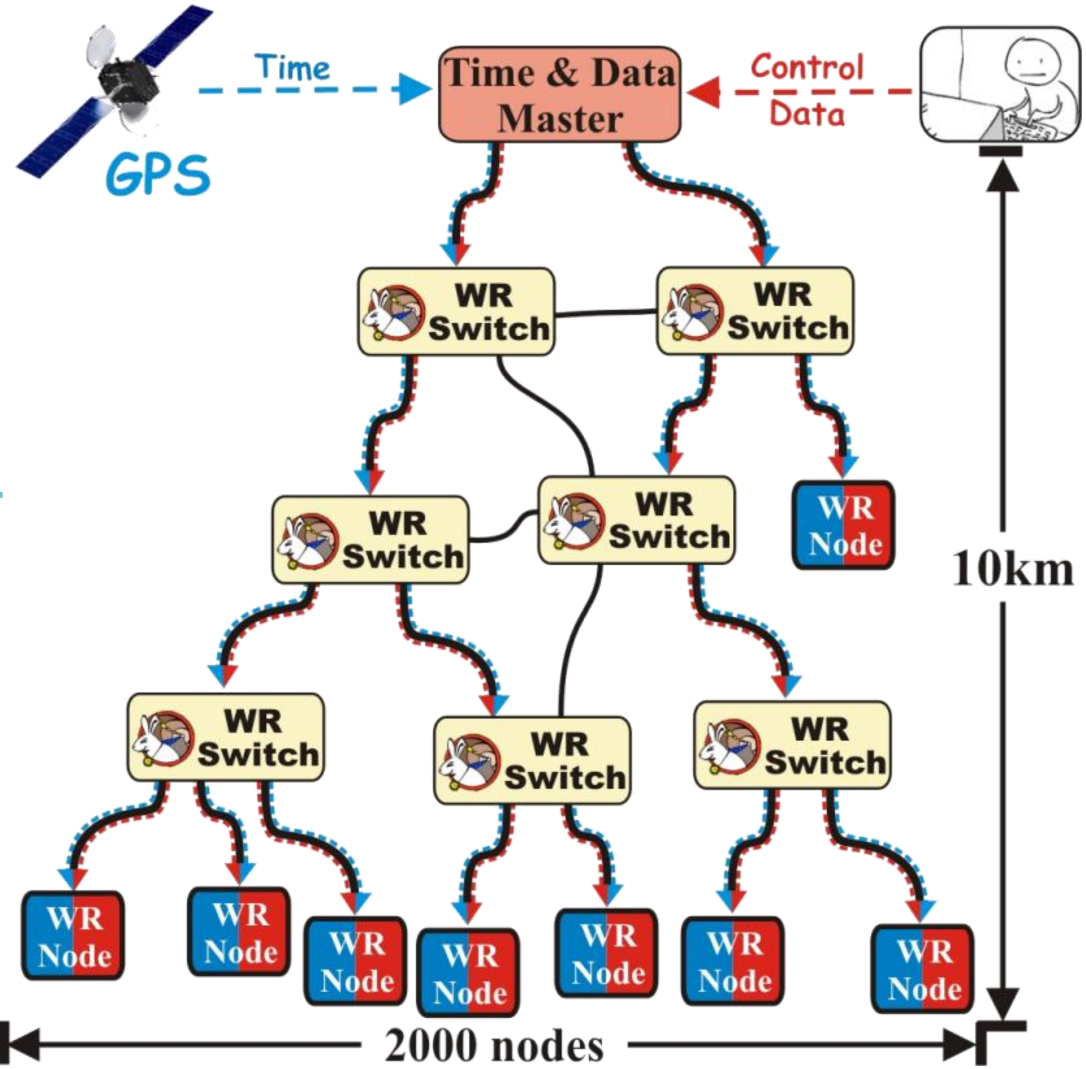
- **Synchronous mode** (SyncE) - common clock for physical layer in entire network, allowing for precise time and frequency transfer.
- **Deterministic routing** latency - a guarantee that packet transmission delay between two stations will never exceed a certain boundary.



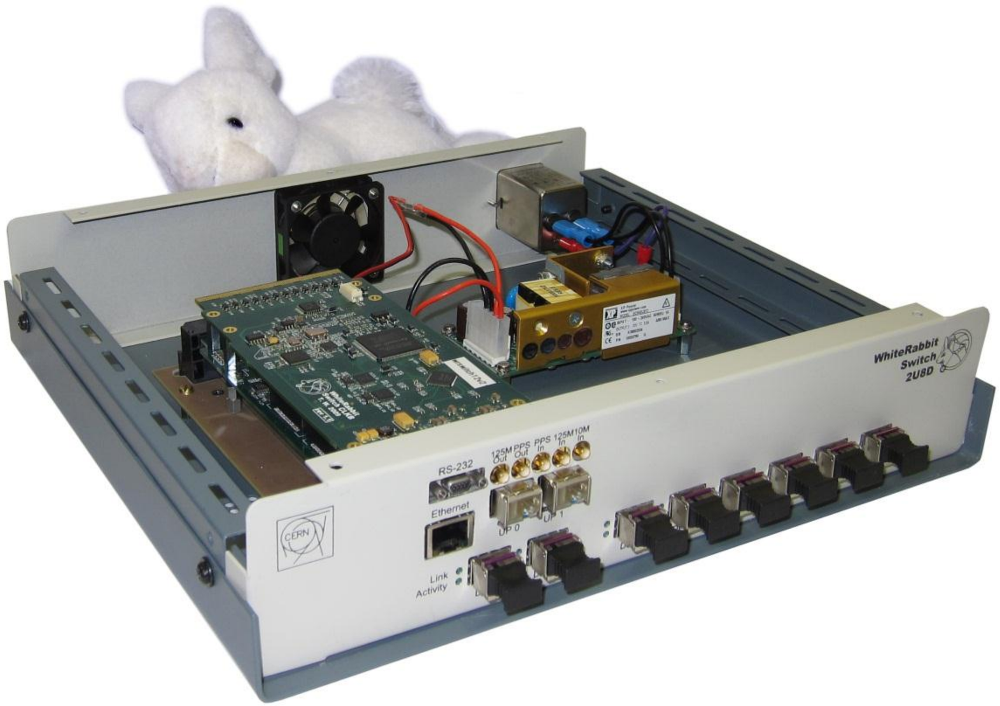
A White Rabbit Network

<u>**Design goals:**</u>

- 1ns synchronization accuracy, 20 ps jitter
- 10 km fiber links
- Up to 2000 nodes



WR Switch



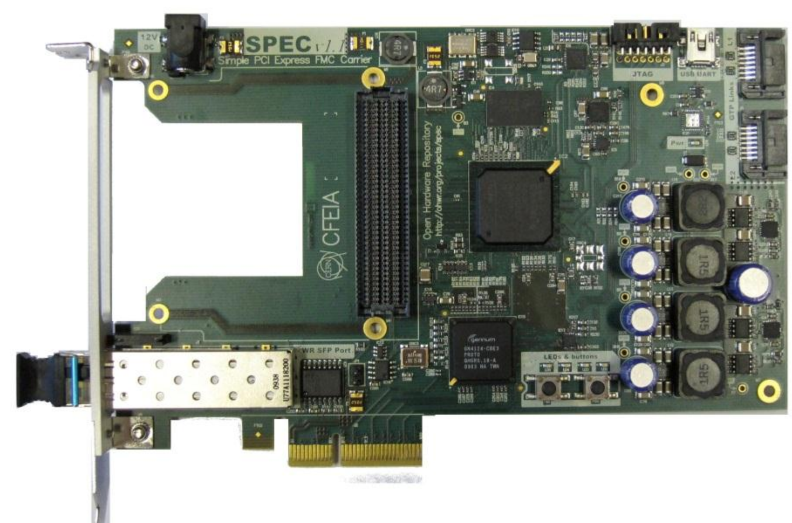
Central element of WR network

- Fully custom design, done from scratch at CERN
- Ten 1000Base-X ports, may drive 10+ km of SM fiber
- 200 ps synchronization accuracy

WR Node

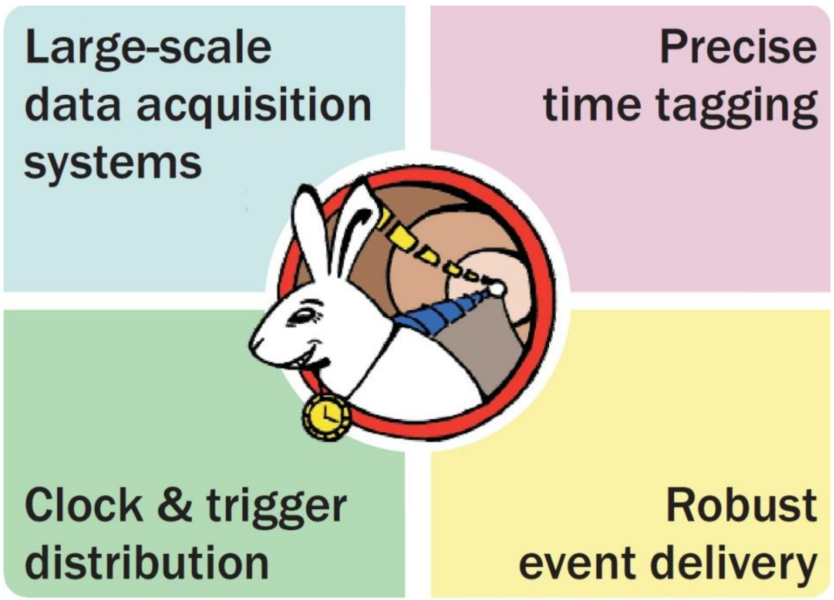
- **IP Core** (HDL) which can be instantiated in any FPGA design
- Provides:
  - **WR synchronization stack** (using an embedded CPU)
  - **Forward Error Correction (FEC)** encoder/decoder
  - Deterministic embedded CPU, timers, counters
- Reference WR Node H/W design:

  Simple PCIe FMC carrier (SPEC)
  - Can host FMCs (FPGA Mezzanine Cards) with ADCs, DACs, TDCs
  - Open Hardware
  - Commercially available



Possible applications

- Accelerator control and timing system (CERN, GSI)
- Distributed Direct Digital Synthesis (TTC, RF, bunch clock)
- Distributed oscilloscope
- Time distribution in Large High Altitude Air Shower Observatory (Tibet, China)



Developments for fs Synchronization

- Master Oscillator System for the FLASH Accelerator

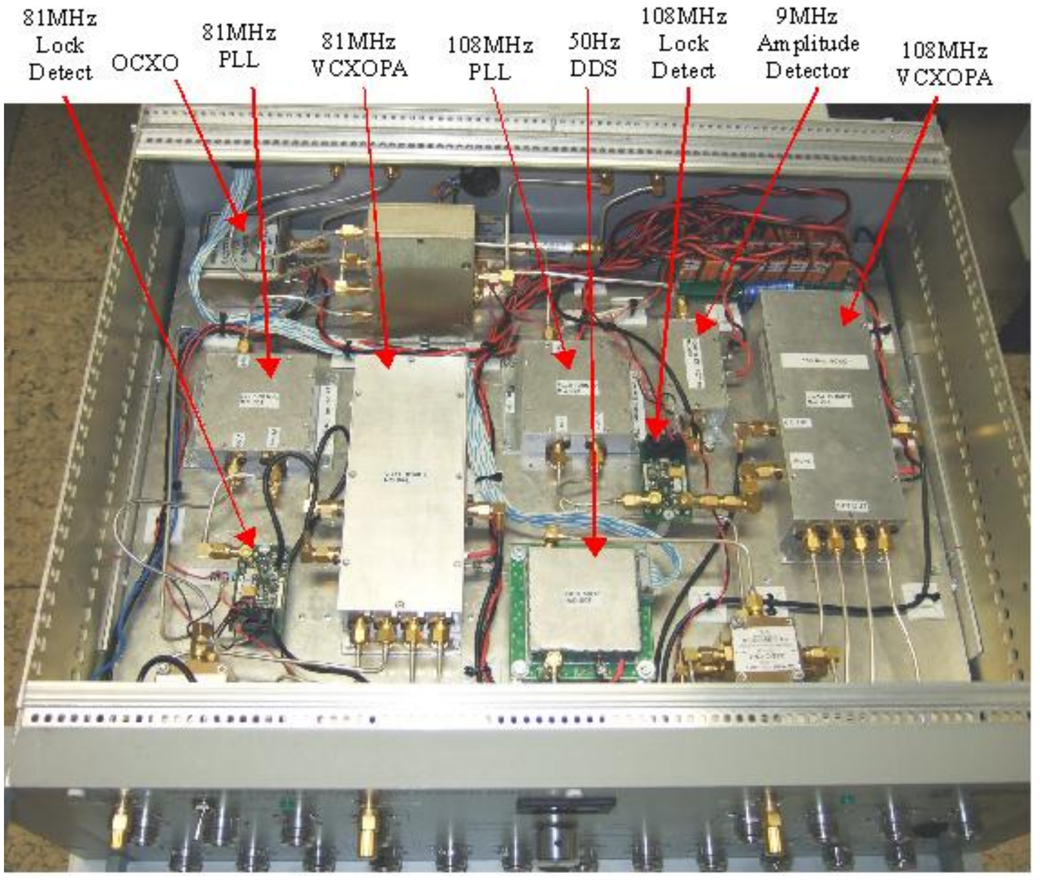
Injector Area

H3 Extension Subdistribution

Team work of DESY and MCID engineers. Many subcomponents of the system were developed in Warsaw

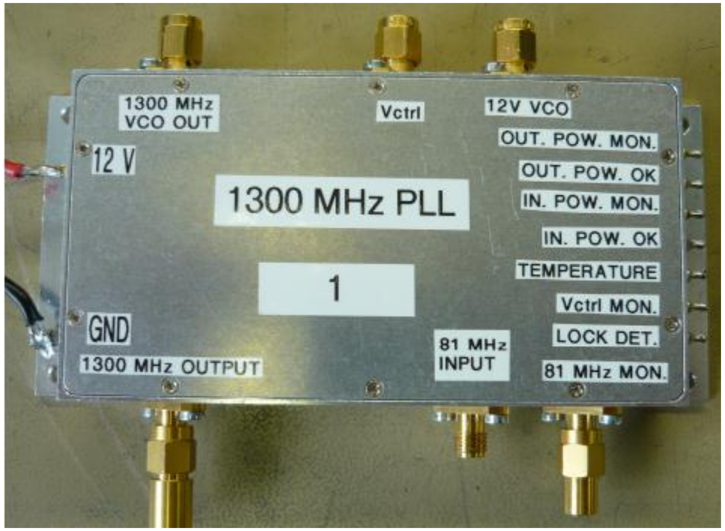
Developments for fs Synchronization

- Main Reference Module for the FLASH Master Oscillator System

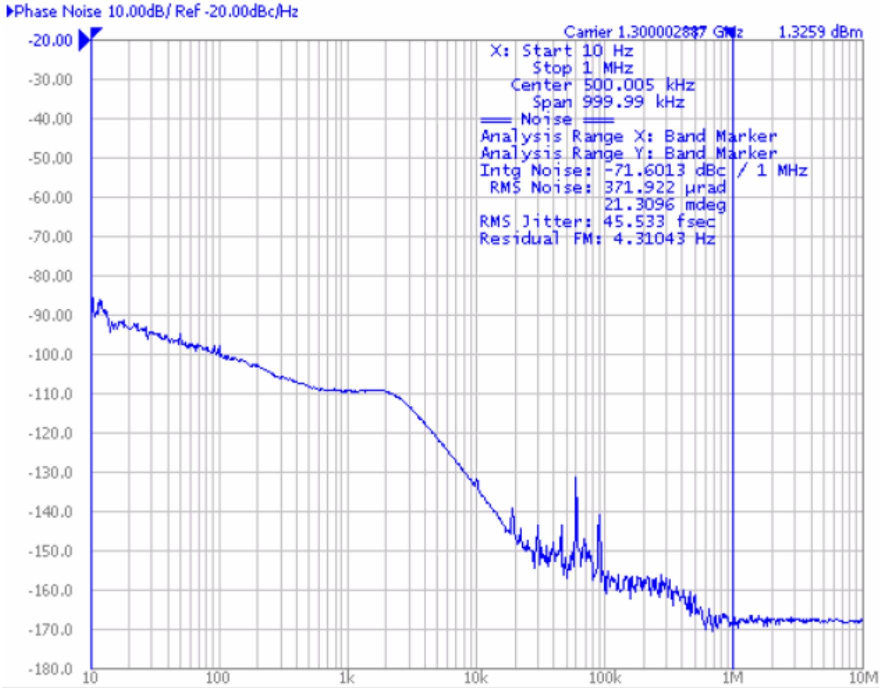


Developments for fs Synchronization

- Extremely Low Phase Noise and Low Drift PLL Module

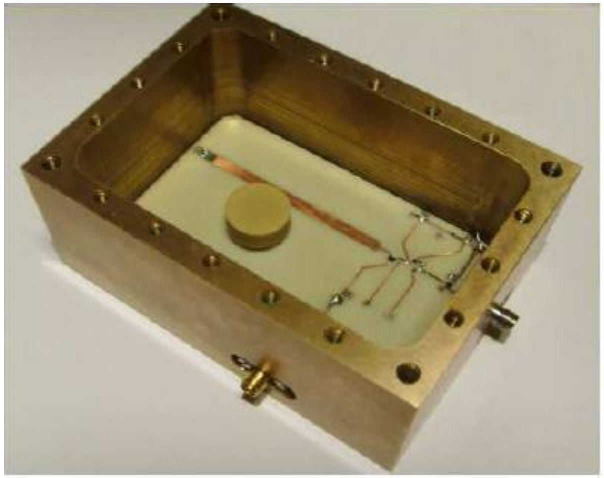


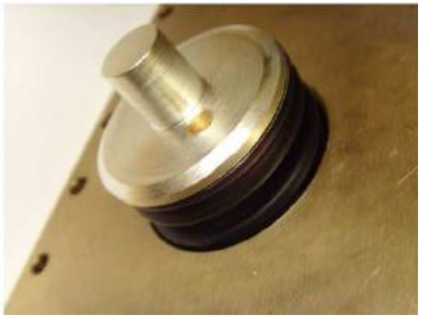
- By Ł. Zembala and H. Weddig
- Designed for use with external VCO
- Includes diagnostic circuits (also for long term drift performance monitoring)
- Phase noise measurement results when locking 1.3 GHz DRO to 81 MHz OCXO below

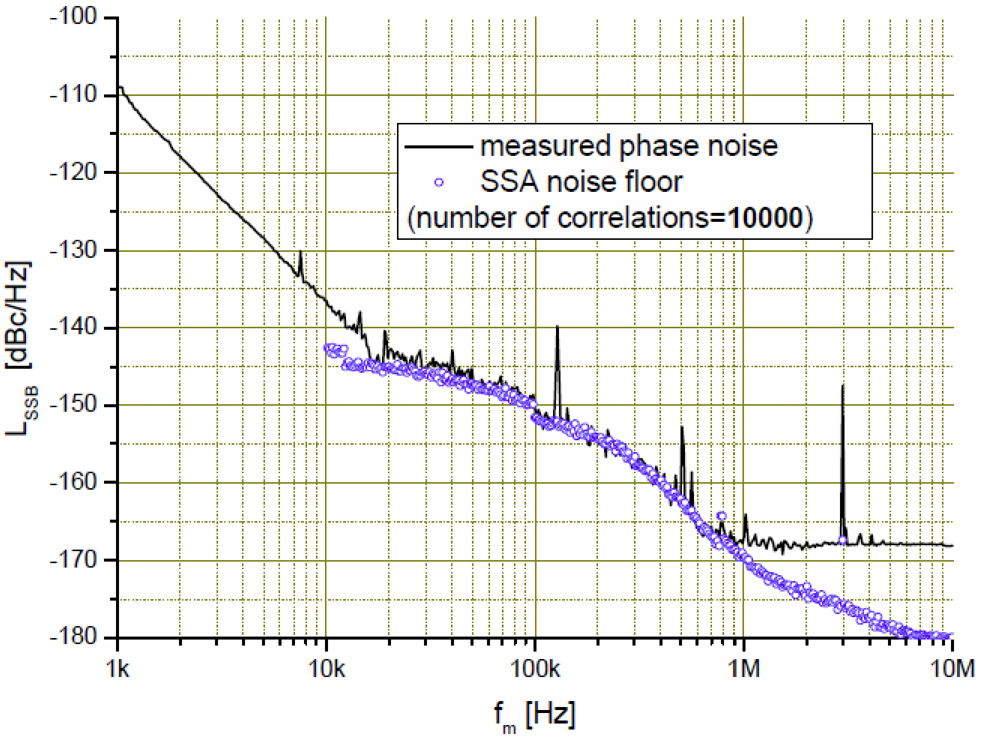


Developments for fs Synchronization

- Extremely Low Phase Noise 2.85 GHz Dielectric Resonator Oscillator
  - By J. Piekarski



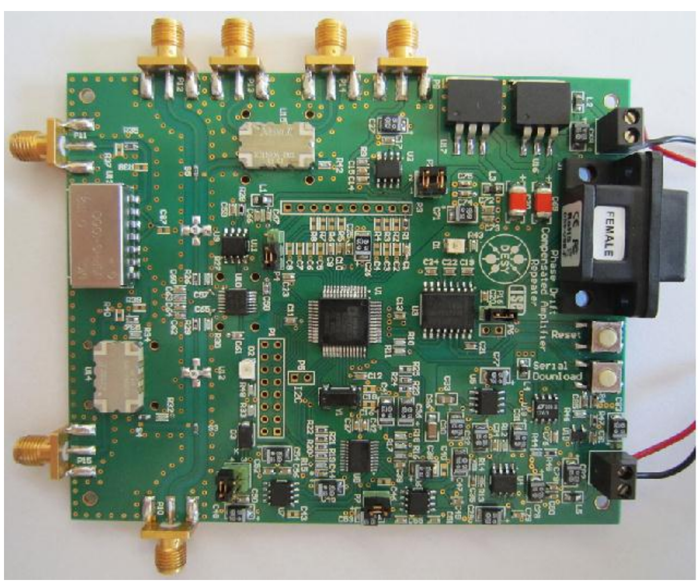


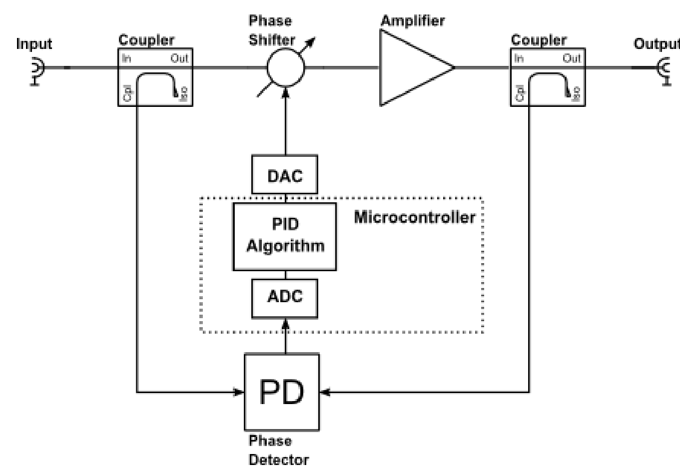


Developments for fs Synchronization

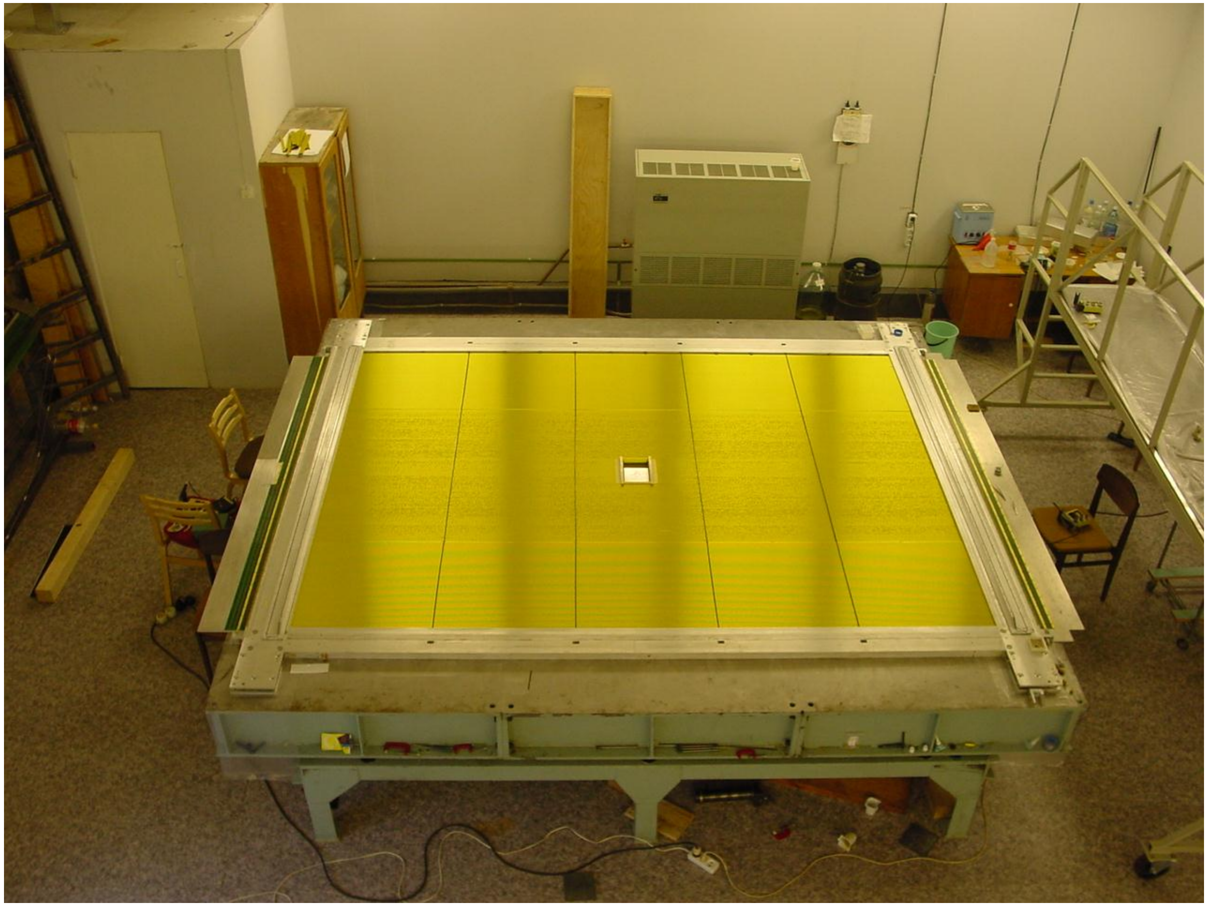
• 1.3 GHz power amplifier drift compensator

- Compensation of phase drifts of high power amplifiers (HPAs)
- Amplifier input and output signals are coupled for measurement by two carefully selected low-phase drift directional couplers
- Phase difference of coupled RF signals is measured by the phase detector
- Measured phase drift of a HPA is compensated by tuning the phase shifter
- Demonstrated drift compensation down to 30 fs/K (p-p)!
- By S. Jabłoński

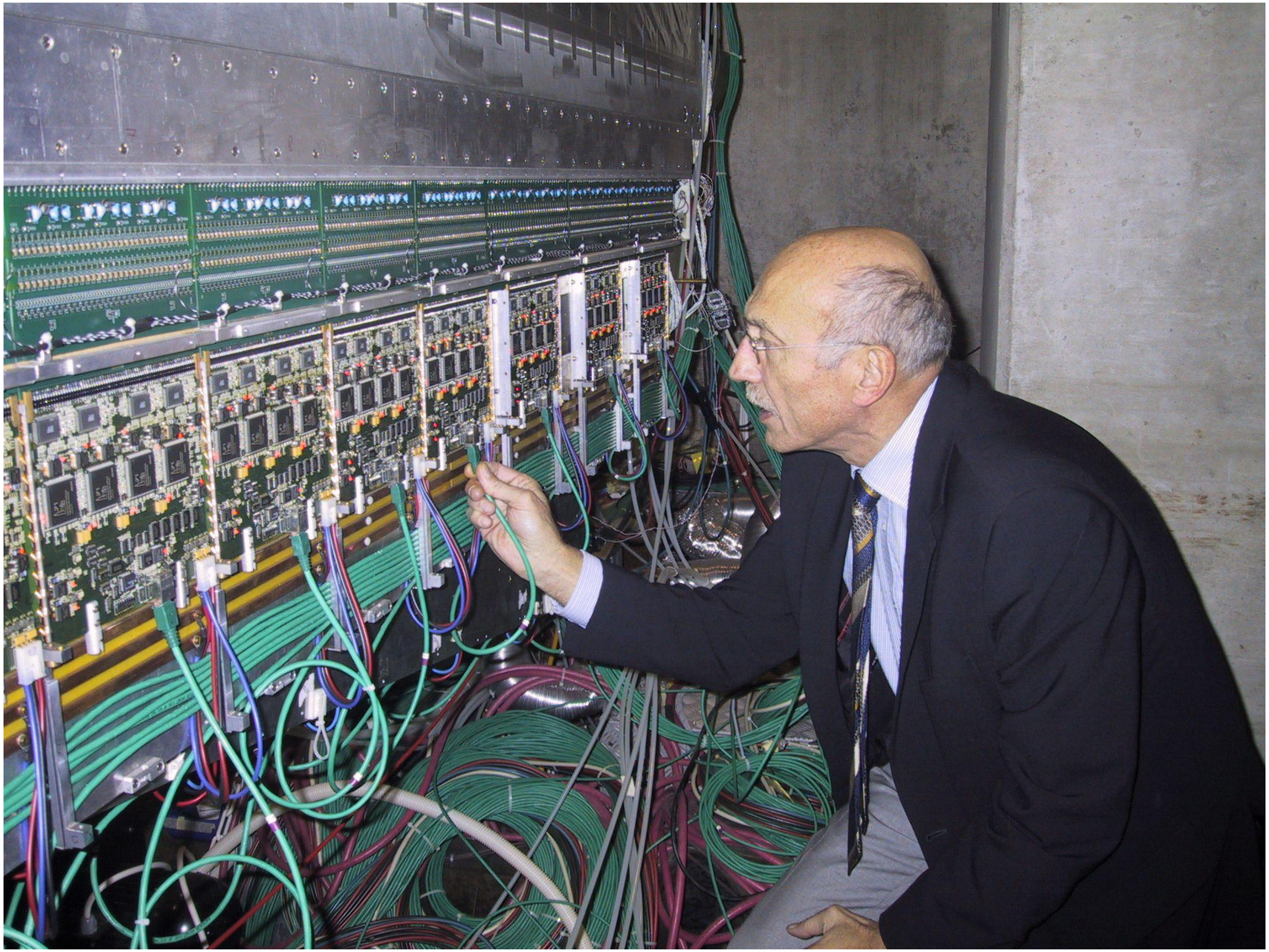




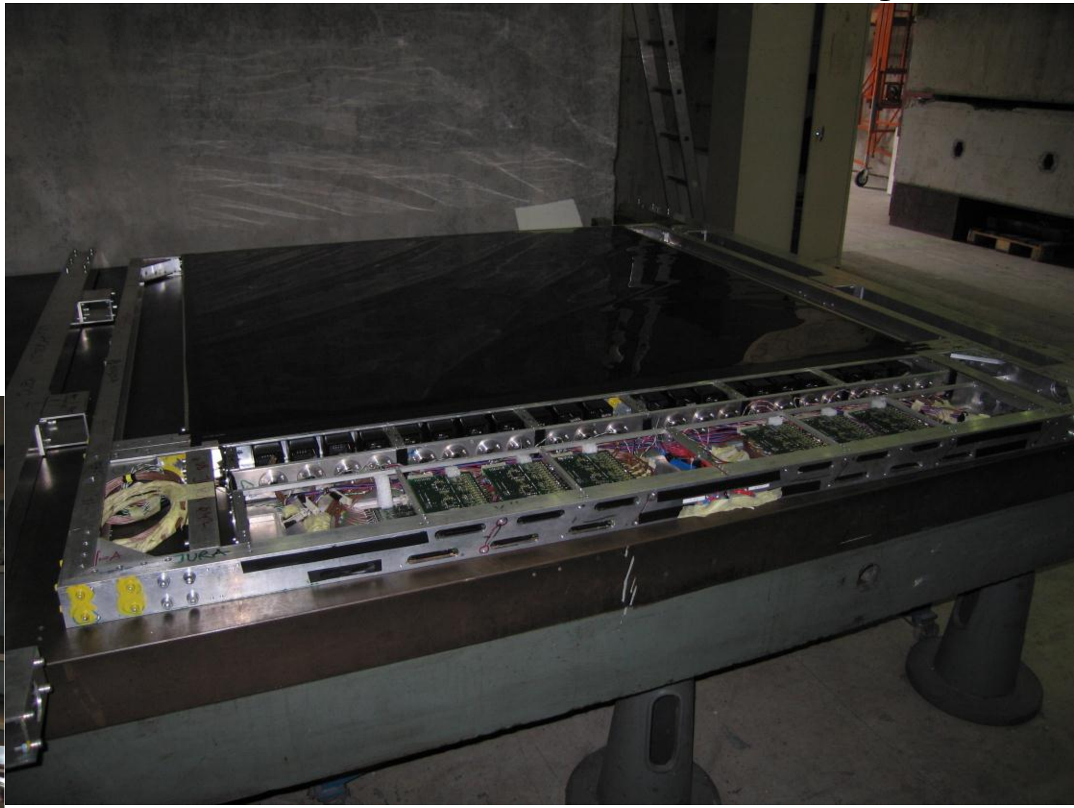
Nuclear and Medical Electronics Department, prof.K.Zaremba, prof.J.Marzec, WUT
CERN COMPASS, Straw tube chamber, JINR-Dubna, gluing of detector plane, cooperation with Freiburg and Munich



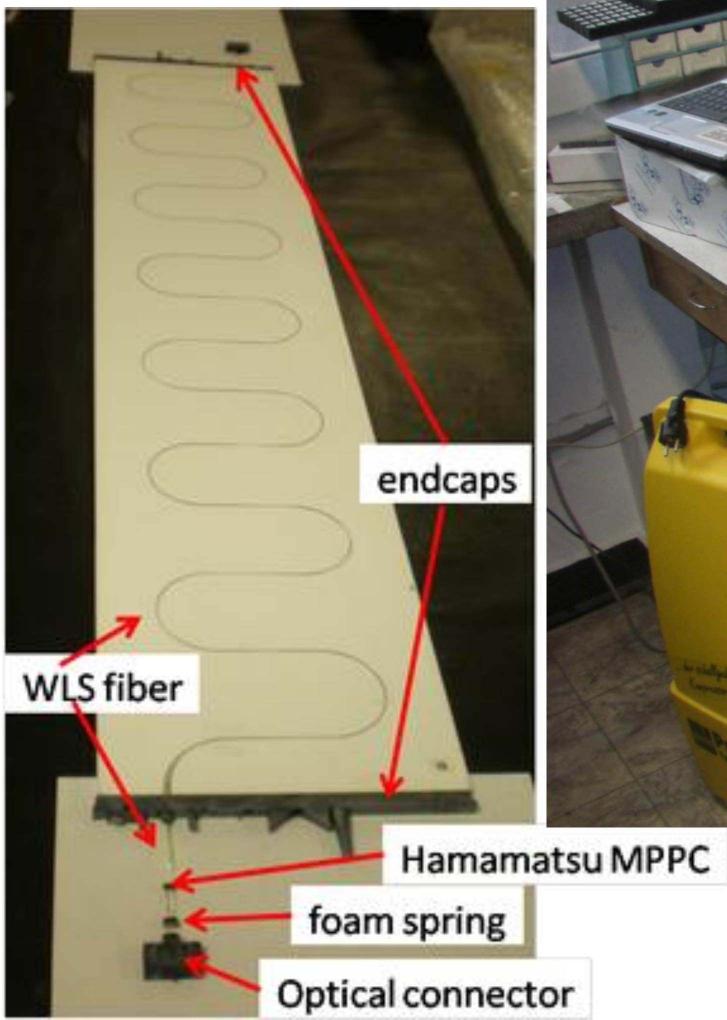
COMPASS, detector front end electronics



COMPASS, Scintillanting Fibers detector, cooperation with NCBJ, detector assembly



T2K, SMRD-Side Muon Range Detector, MPPC-multi-pixel photon counter



SPRD detector, scintillation modules in magnet slots

WUT involvements

- CERN: LHC, CMS, Alice, TOTEM, CERN2GS
- Japan: T2K
- Russia: Dubna JINR
- France: IN2P3, CEA, ITER
- UK: JET
- Italy: INFN
- Germany: DESY, GSI, BESSY
- Spain: Alba
- USA: Fermilab, CEBAF, SLAC
- Chile: ESO, Cherenkov Telescope

Electronics for HEP
and Accelerator Technology

Changes the way

we can do the experiments