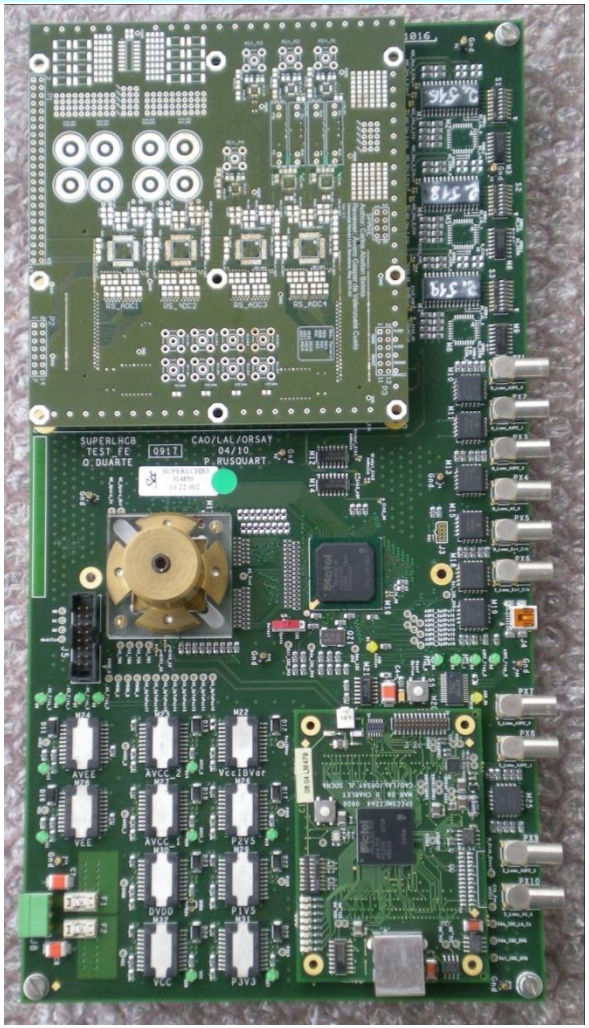
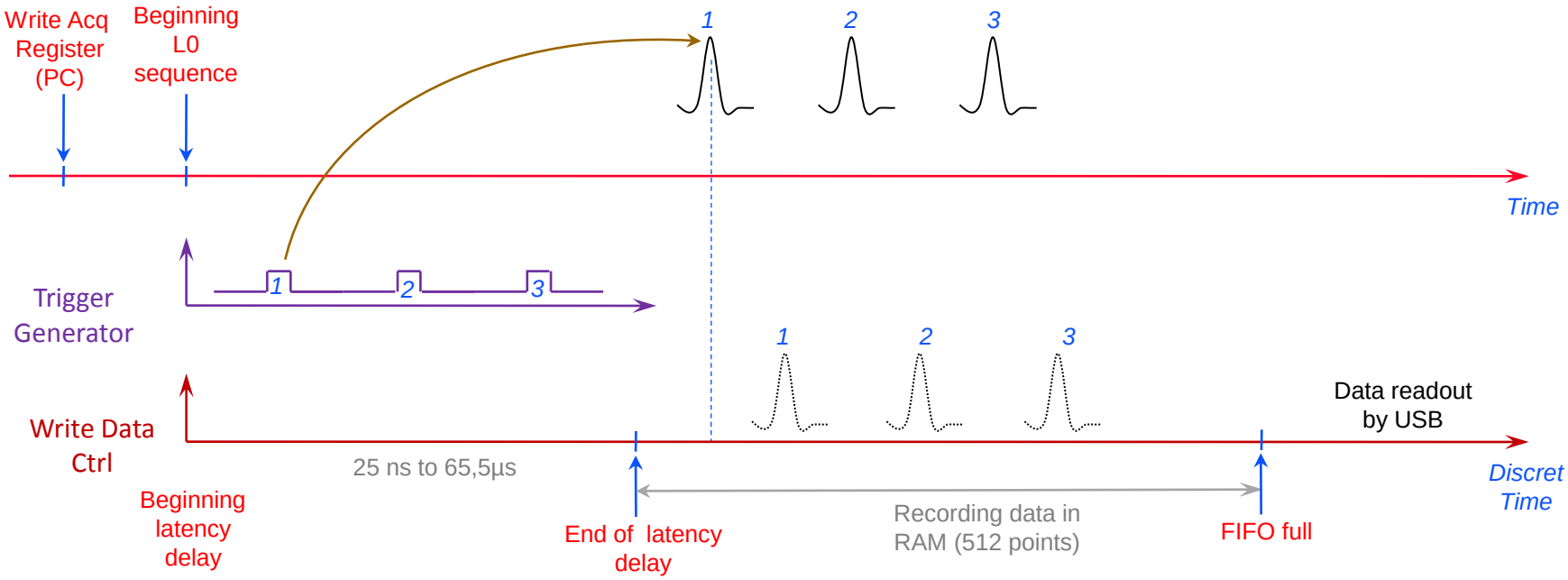
Front-end digital Status

- Acquisition tools to test Analog part.
- Tools to test A3PE FPGA (SSO & SSI)
- Next steps
  - Radiation tests
  - Prototype FEB 8 Channels



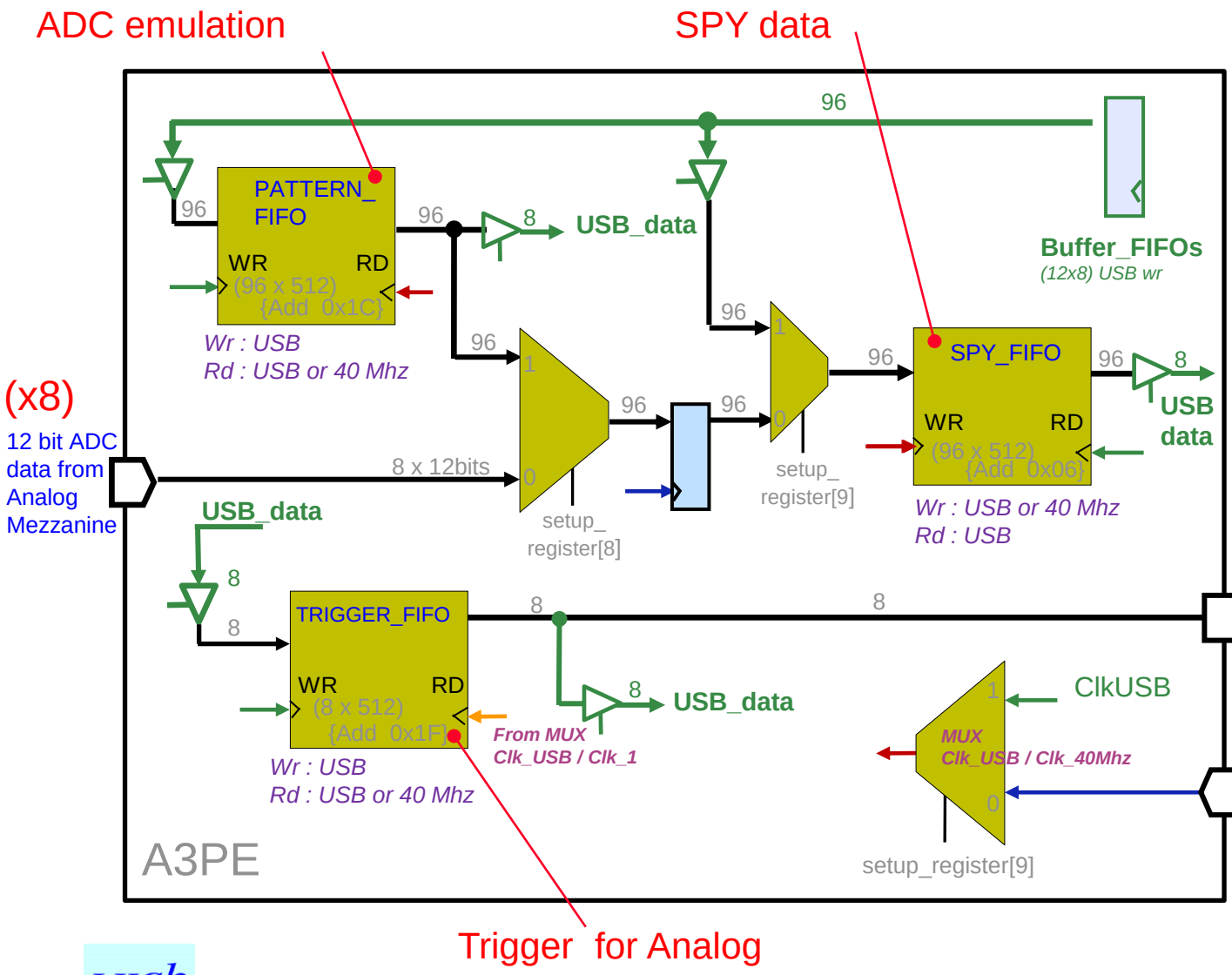
Caceres Thierry
Duarte Olivier

Reminder : Typical acquisition sequence



- **PC write start sequence bit of Acquisition (Acq) Register.**
- **Beginning of L0 sequence.**
- **Each trigger pulse involve pulse shape.**
- **At the end of the latency delay recording 512 points of data (Max).**
- **At the end of the record the system write one “end of acquisition”bit in the Acq_Register .**
- **The PC scrutinize the Acq_Register, when the “end of acquisition” is high the PC download data with the USB interface.**

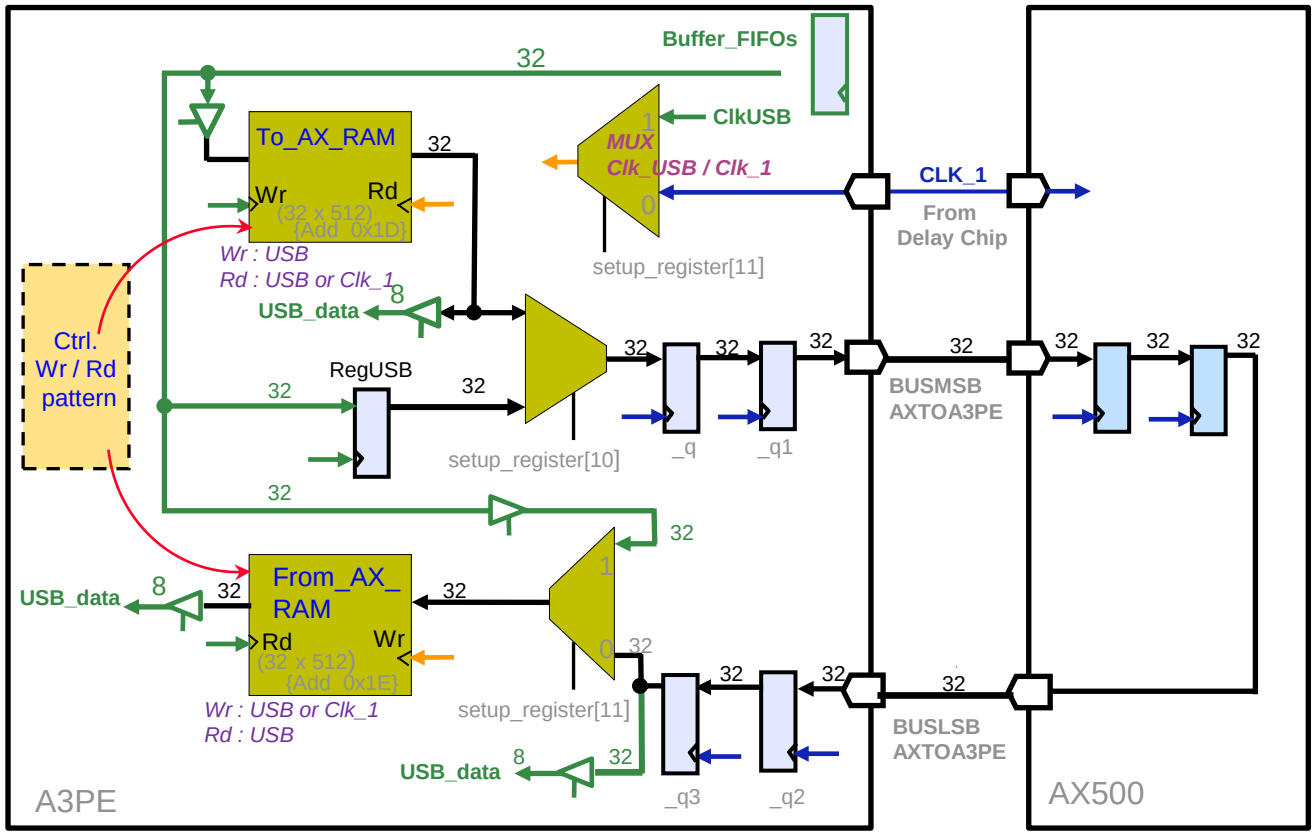
Tools to test Analog part : "Acquisition system"



- **FIFO pattern**
  - Generate digital signals
  - Check FPGA computations
- **SPY FIFO**
  storage of processing results
- **ANALOG PULSE FIFO**
  generate trigger of analog pulses

Tools to test A3PE FPGA (SSO & SSI)

Idea : RAM pattern to test the A3PE IOs functioning by exchanging data between the 2 FPGA (SSO and SSI)

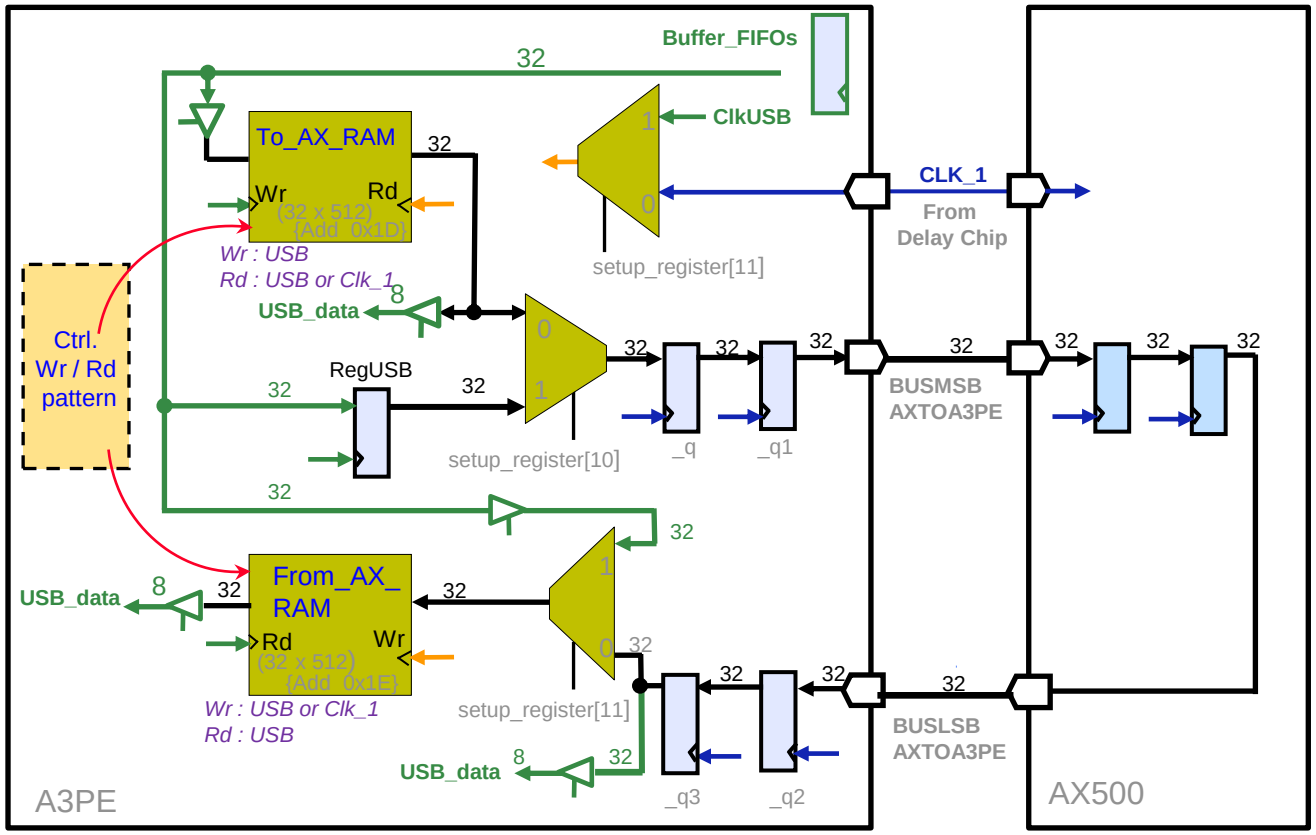


- USB Rd / Wr the RAM (To_AX and From_AX).

Sequence:

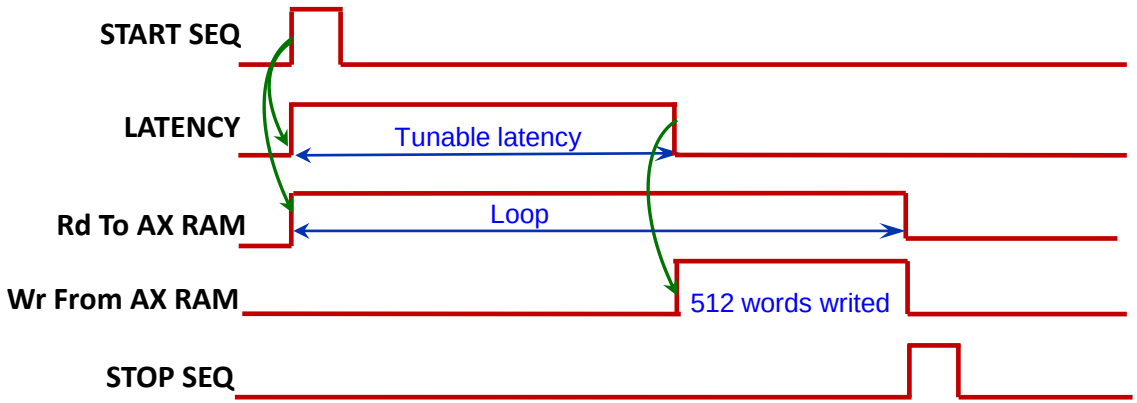
- To_AX _RAM Rd/Wr by USB
- Start commande
- Loop on to AX_RAM until stop command
- Programmable latency to capture data from To_AX_RAM to FROM_AX_RAM

- Start / Stop and latency (implemented !)



Start Stop Latency sequence

START / STOP / LATENCY SEQUENCE

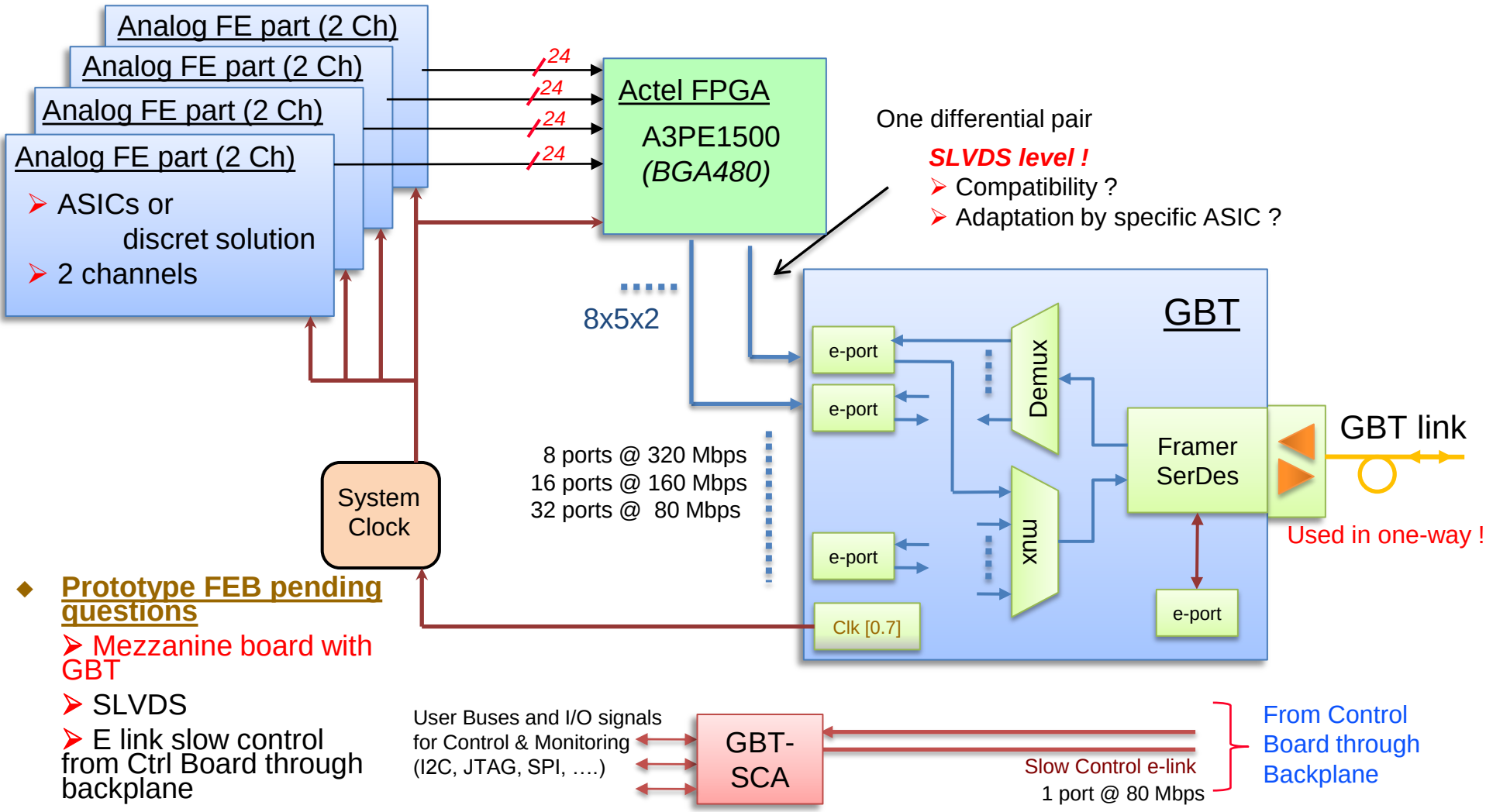


Status:

- Firmware implemented
- Cycle — *Ok*
- Rd / Wr by USB — *Ok*
- Internal loop — *In progress*
- External loop (AX FPGA) — *In progress*
- 3 boards in used

Prototype FEB 8 Channels

Some idea of architecture ….

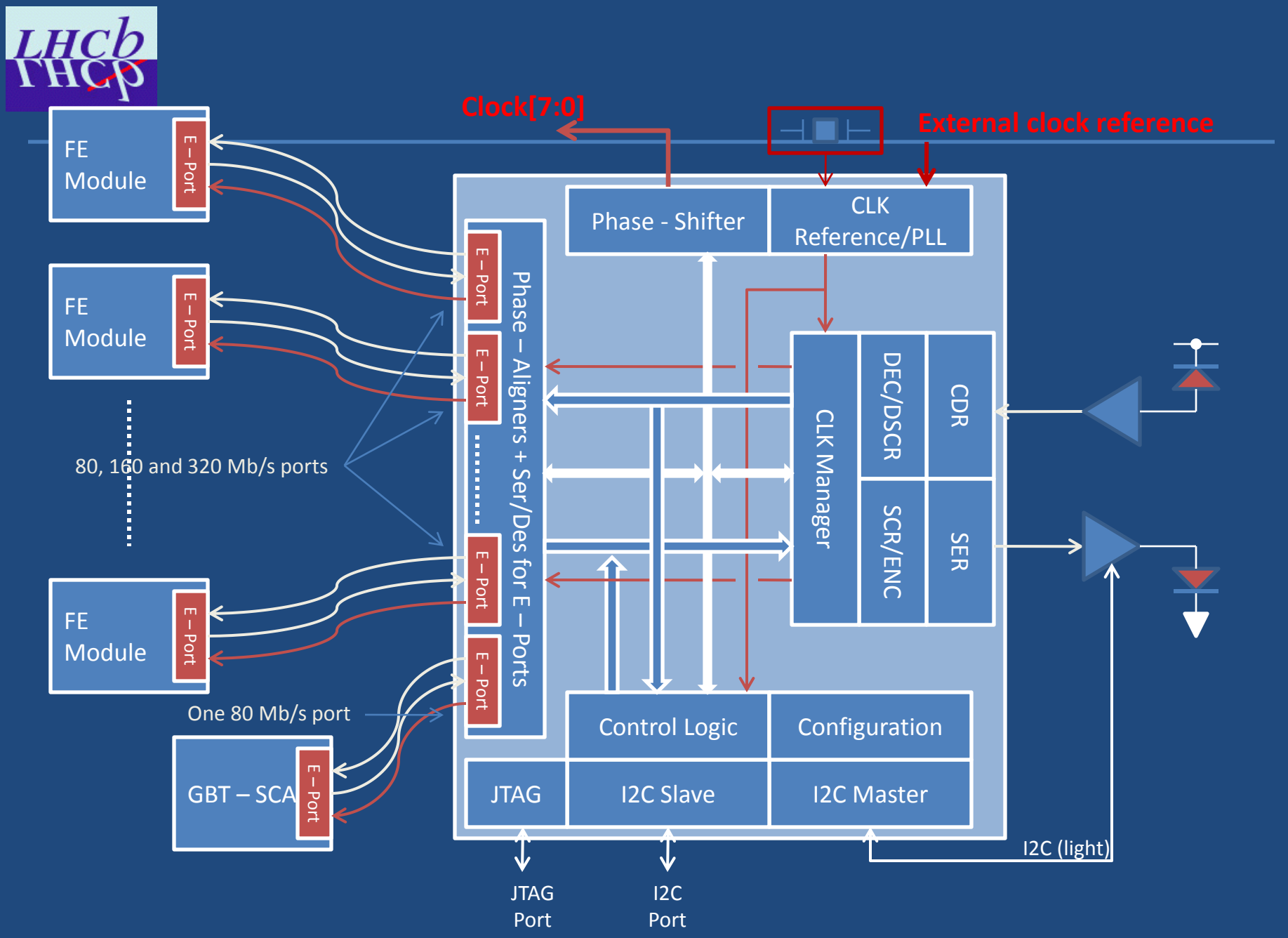


- **Prototype FEB pending questions**
  - Mezzanine board with GBT
  - SLVDS
  - E link slow control from Ctrl Board through backplane

Conclusion

- **Digital electronic is ok, several adjustment have been done .**
- **Last adjustment of the tools to test A3PE FPGA (SSO & SSI).**
- **Radiation tests of components for analog and digital part .**
- **Start thinking about the prototype FEB, we considered a 8 channels prototype FEB for the beginning of 2013 with (mezzanine ?) GBT (availability of the first GBT samples) ?**

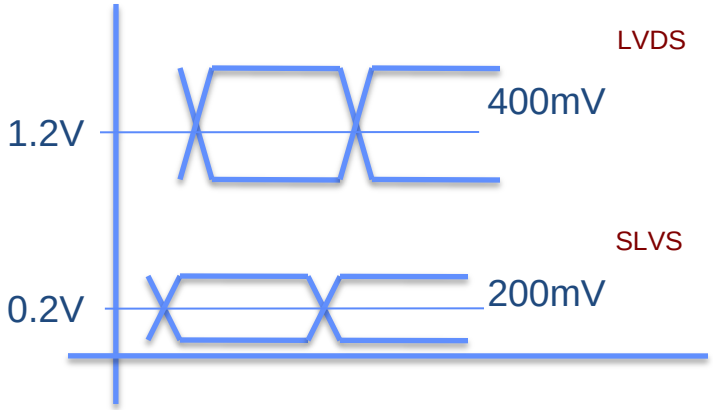
SPARE


Clock[7:0]
External clock reference
FE Module
E – Port
FE Module
E – Port
80, 160 and 320 Mb/s ports
FE Module
E – Port
One 80 Mb/s port
GBT – SCA
E – Port
Phase - Shifter
CLK Reference/PLL
Phase – Aligners + Ser/Des for E – Ports
E – Port
E – Port
E – Port
E – Port
CLK Manager
DEC/DSCR
CDR
SCR/ENC
SER
Control Logic
Configuration
JTAG
I2C Slave
I2C Master
I2C (light)
JTAG Port
I2C Port

Physical Layer (electrical)

Kostas Kloukinas's slide

- **SLVS (Scalable Low Voltage Standard)**
  - **JEDEC standard: JESD8-13**
  - **Differential voltage based signaling protocol.**
    - **Voltage levels compatible with deep submicron processes.**
    - **Typical link length runs of 30cm over PCB at 1Gbps.**
    - **Low Power, Low EMI**
  - **Application in data links for Flat Panel displays in mobile devices.**
    - **Mobile Pixel Link, MPL-2 (National semi.)**



SLVS specifications brief

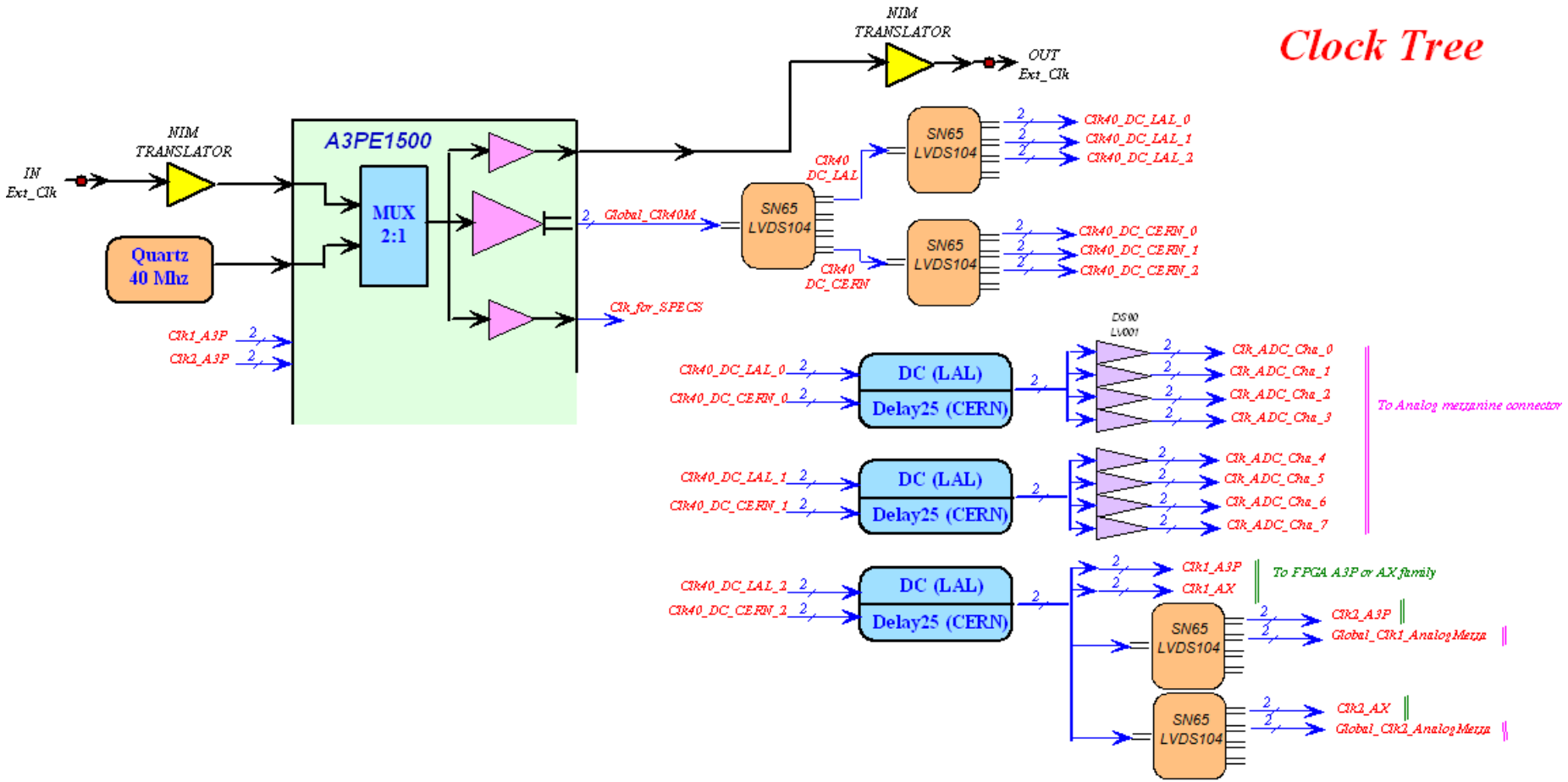
2 mA Differential max

Line impedance: 100 Ohm

Signal: +- 200 mV

Common mode ref voltage: 0.2V

Clock tree


Clock Tree
NIM TRANSLATOR
OUT Ext_Clk
NIM TRANSLATOR
IN Ext_Clk
A3PE1500
MUX 2:1
Quartz 40 Mhz
Clk1_A3P
Clk2_A3P
Global_Clk40M
Clk_for_SPECS
SN65 LVDS104
Clk40 DC_LAL
Clk40 DC_CERN
Clk40_DC_LAL_0
Clk40_DC_LAL_1
Clk40_DC_LAL_2
Clk40_DC_CERN_0
Clk40_DC_CERN_1
Clk40_DC_CERN_2
DC (LAL)
Delay25 (CERN)
DS90 LV001
Clk_ADC_Cha_0
Clk_ADC_Cha_1
Clk_ADC_Cha_2
Clk_ADC_Cha_3
Clk_ADC_Cha_4
Clk_ADC_Cha_5
Clk_ADC_Cha_6
Clk_ADC_Cha_7
To Analog mezzanine connector
Clk1_A3P
Clk1_AX
To FPGA A3P or AX family
Clk2_A3P
Global_Clk1_AnalogMezza
Clk2_AX
Global_Clk2_AnalogMezza
27th November , 2009