



Laboratoire d'Annecy-le-Vieux  
de Physique des Particules

LHCb calorimeter upgrade meeting , June 15<sup>th</sup> 2012

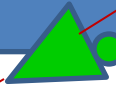
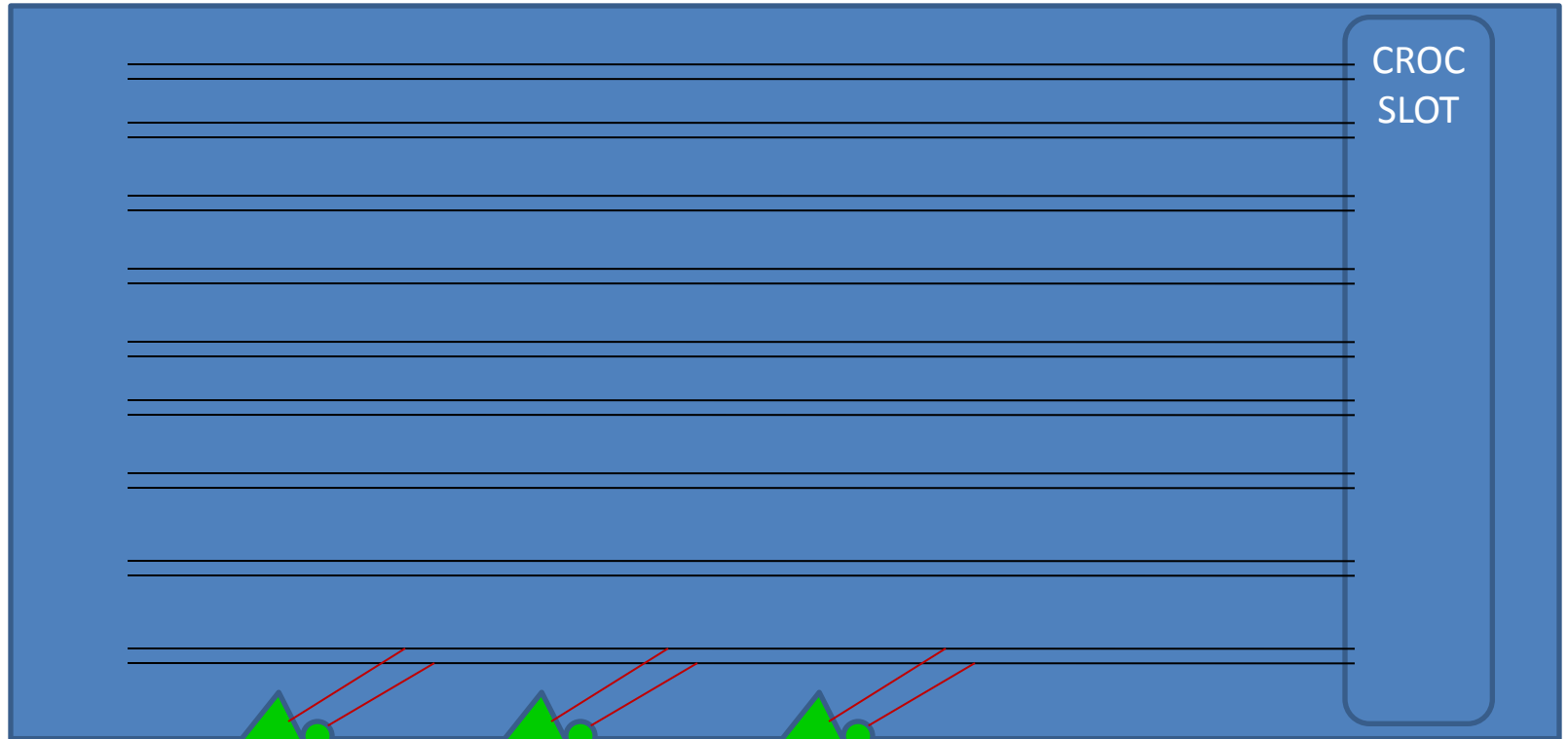
# CONTROL BOARD

## Timing and ECS upgrade for LHCb ECAL Crate

*Cyril Drancourt*

# Current backplane bus

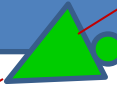
TTC bus: 9 LVDs Line - CROC to all board (FE or TVB) -



FPGA\_Glue  
(FE or TVB)



FPGA\_Glue  
(FE or TVB)



FPGA\_Glue  
(FE or TVB)

# Current backplane bus

TTC bus : 9 LVDS Line - CROC to all board (FE or TVB) -

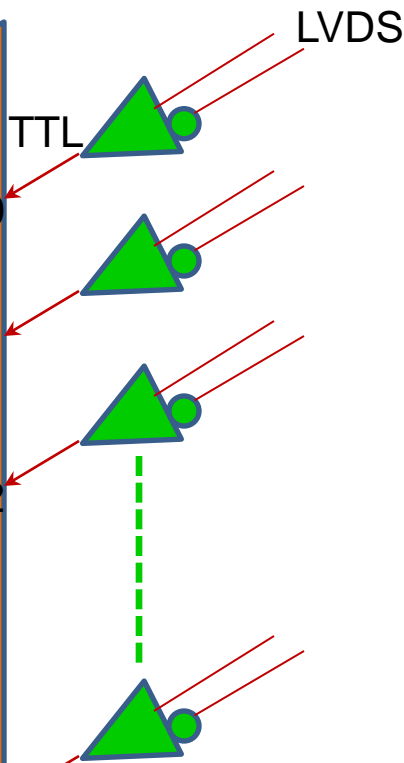
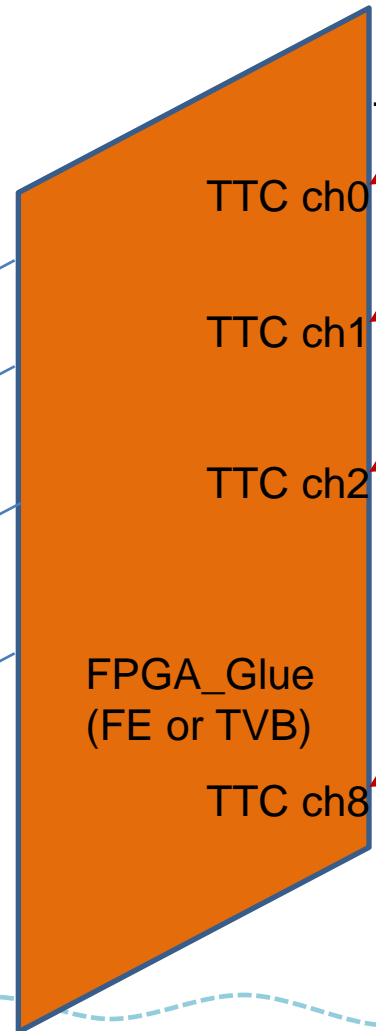
Board Signals

LO\_out  
*(unused in TVB)*

Calib  
*(unused in TVB)*

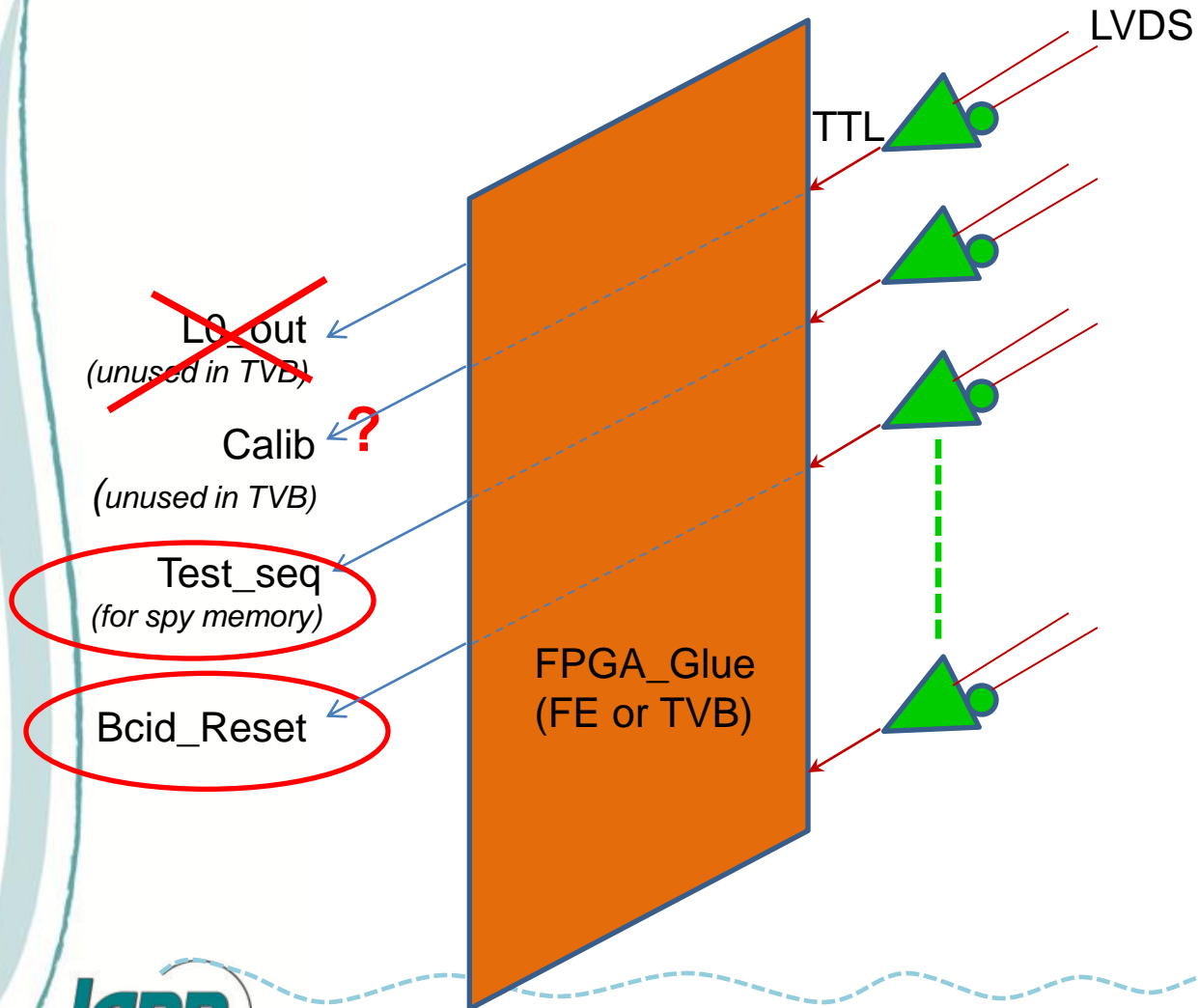
Test\_seq  
*(for spy memory)*

Bcid\_Reset



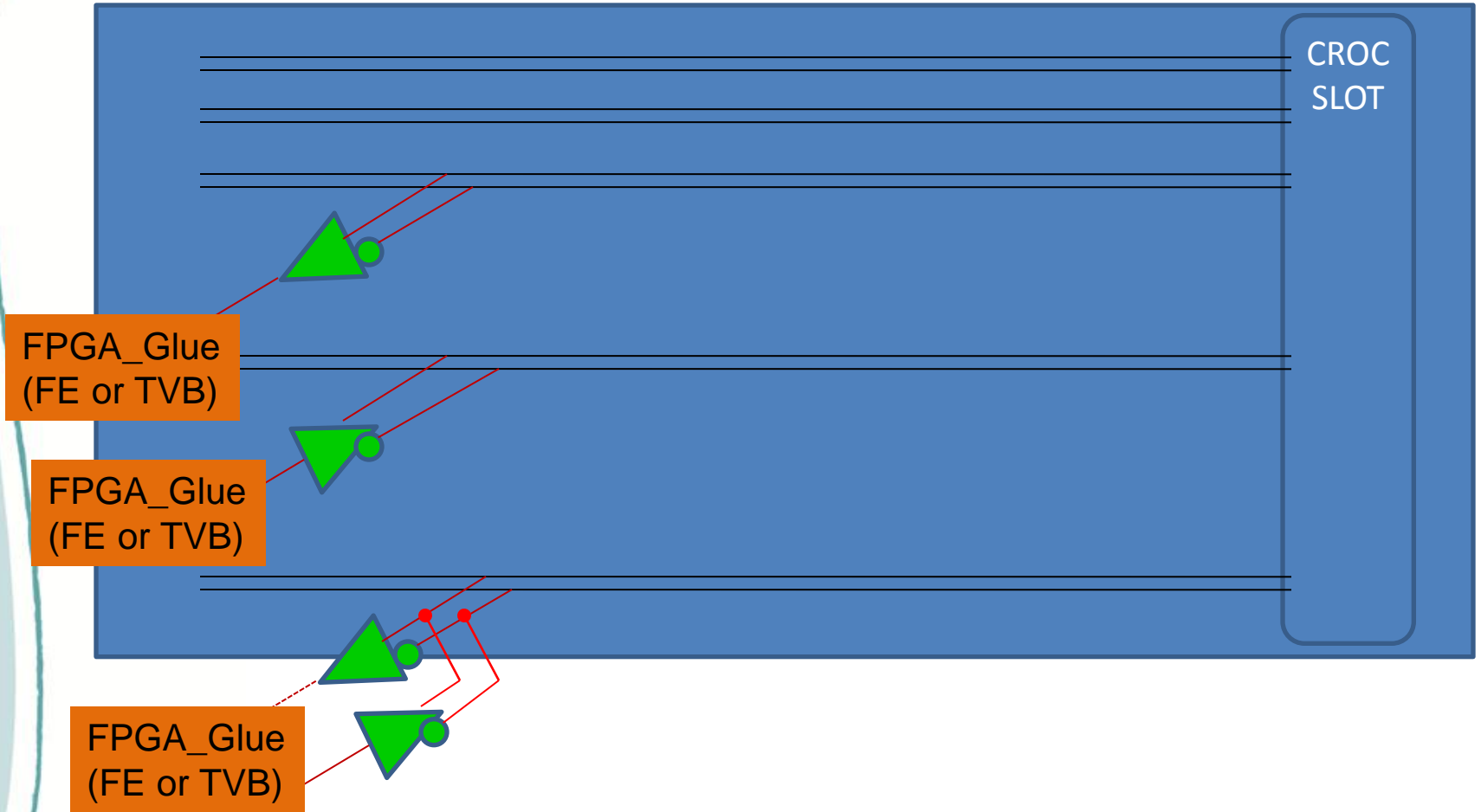
Backplane Bus

# Needs for Upgrade



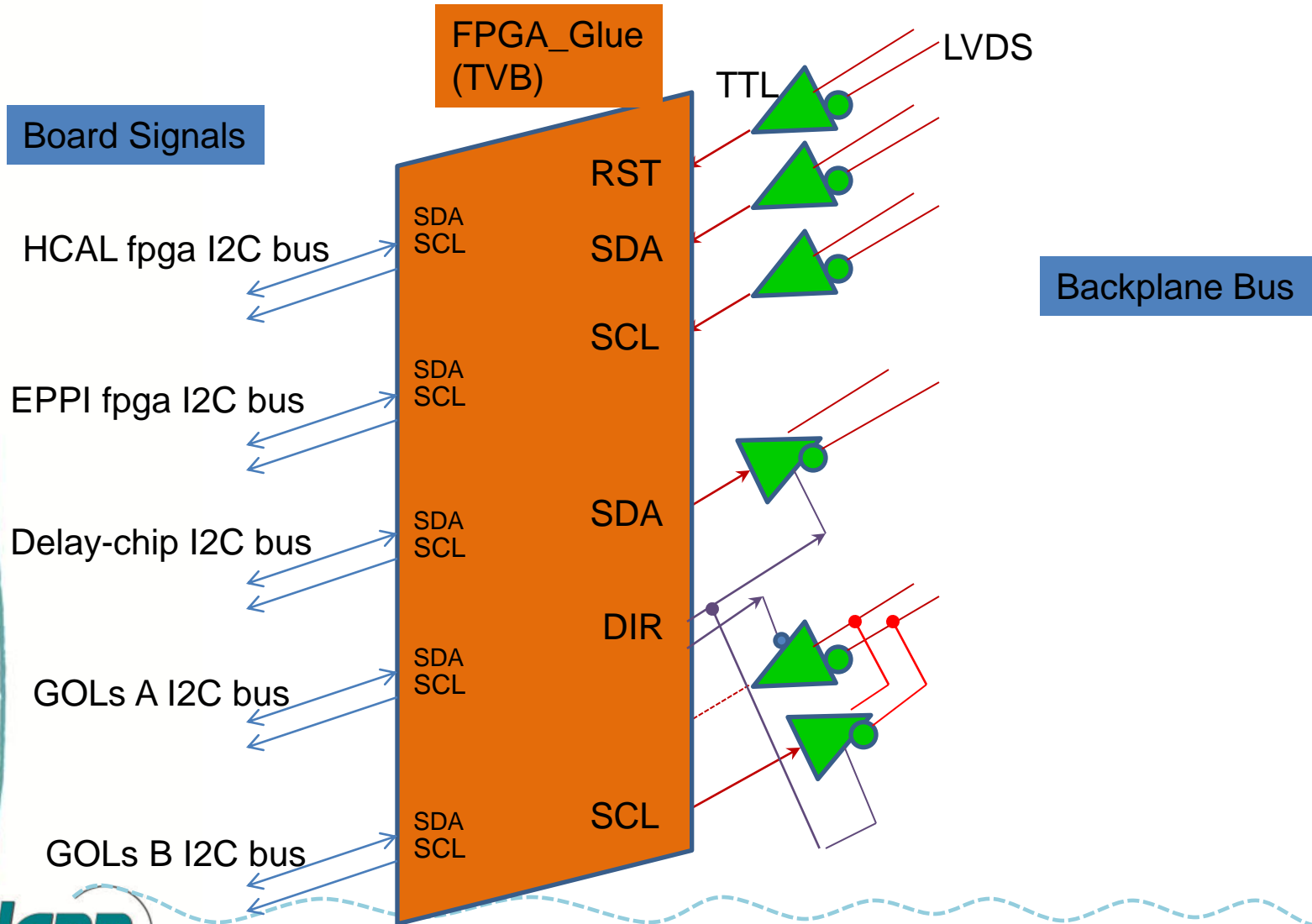
# Current backplane bus

SPECS bus: 5 LVDs Line - 3 CROC-out, 1 CROC-in, 1 CROCinout -

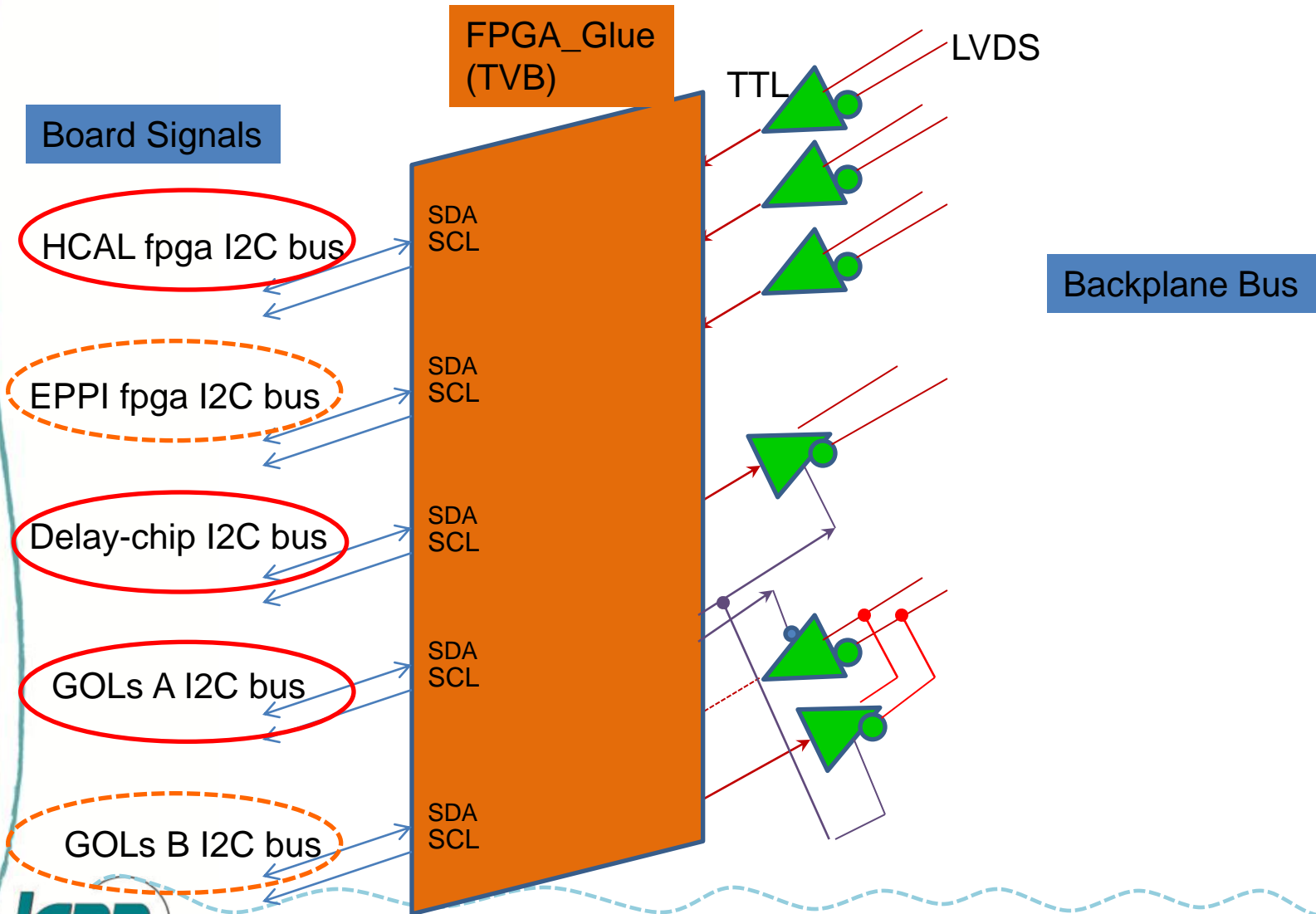


# Current TVB used

**SPECS bus**: 5 LVDs Line - 3 CROC-out, 1 CROC-in, 1 CROCinout -

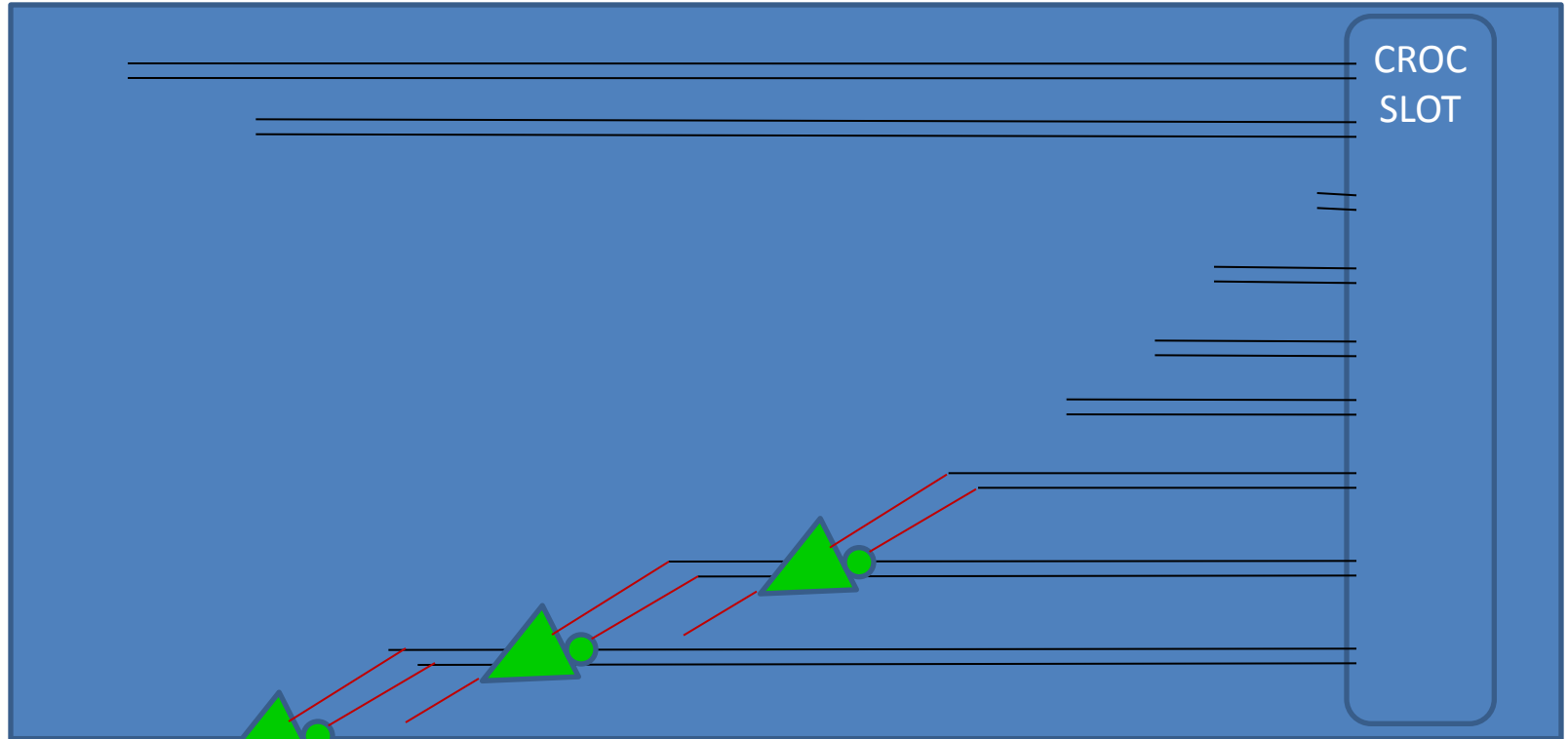


# Needs for Upgrade



# Current backplane clock

1 LVDS Point to Point- CROC to each board (FE or TVB) -



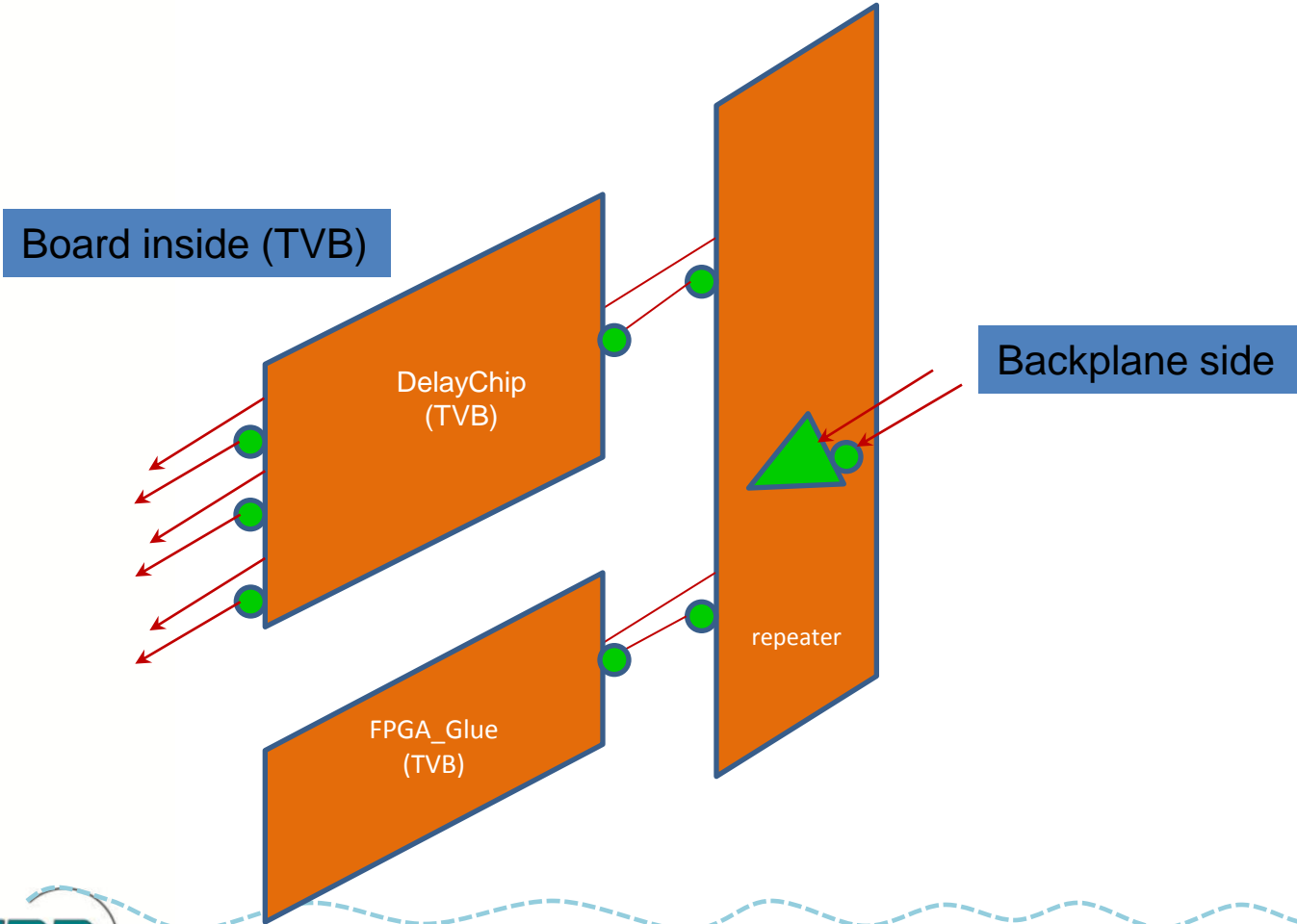
(FE or TVB)



# Current TVB clock

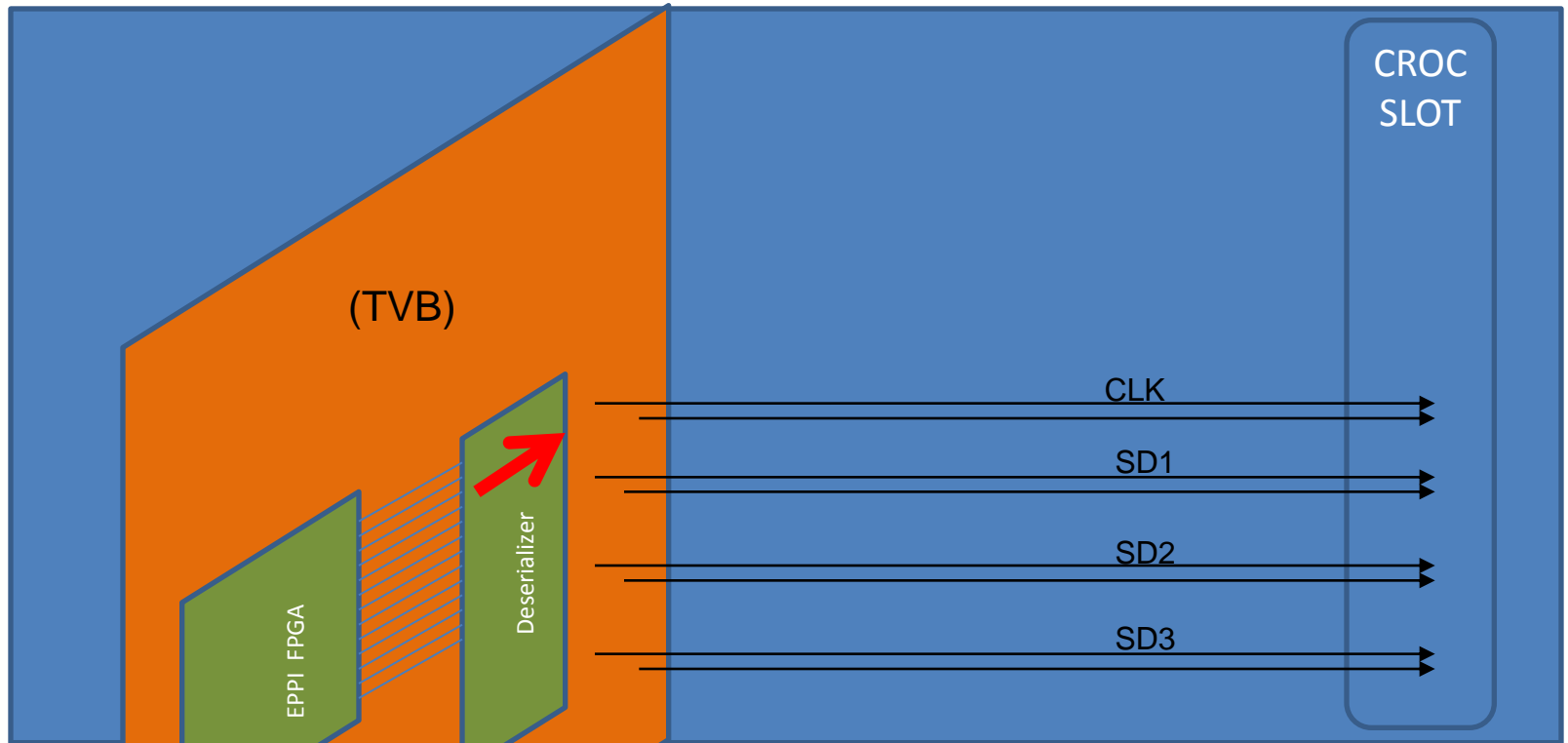
1 LVDS Point to Point- CROC to each board (FE or TVB) -

➤ Need to keep for upgrade



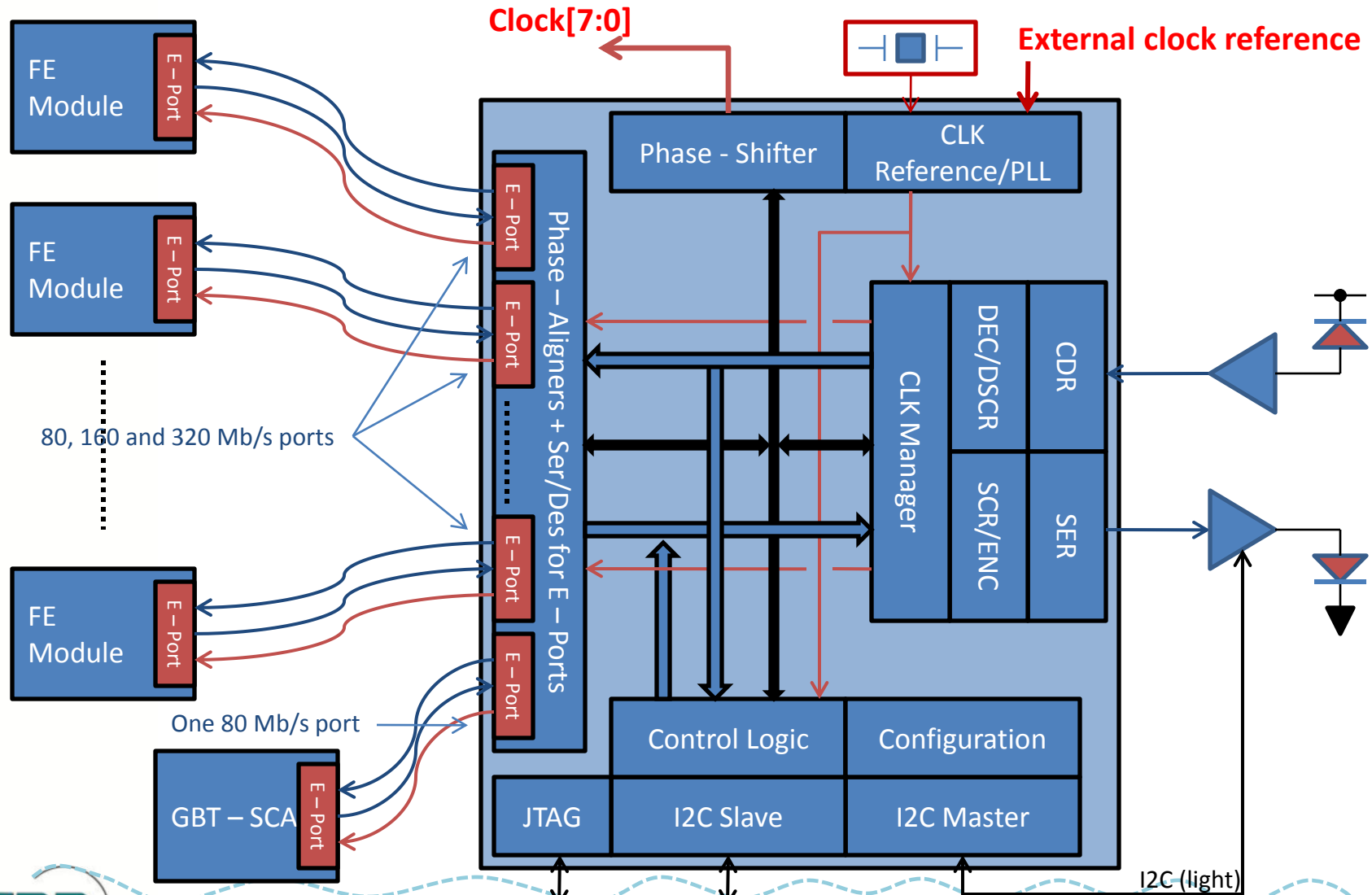
# Current backplane Spare

4 LVDS Point to Point- CROC to each TVB -

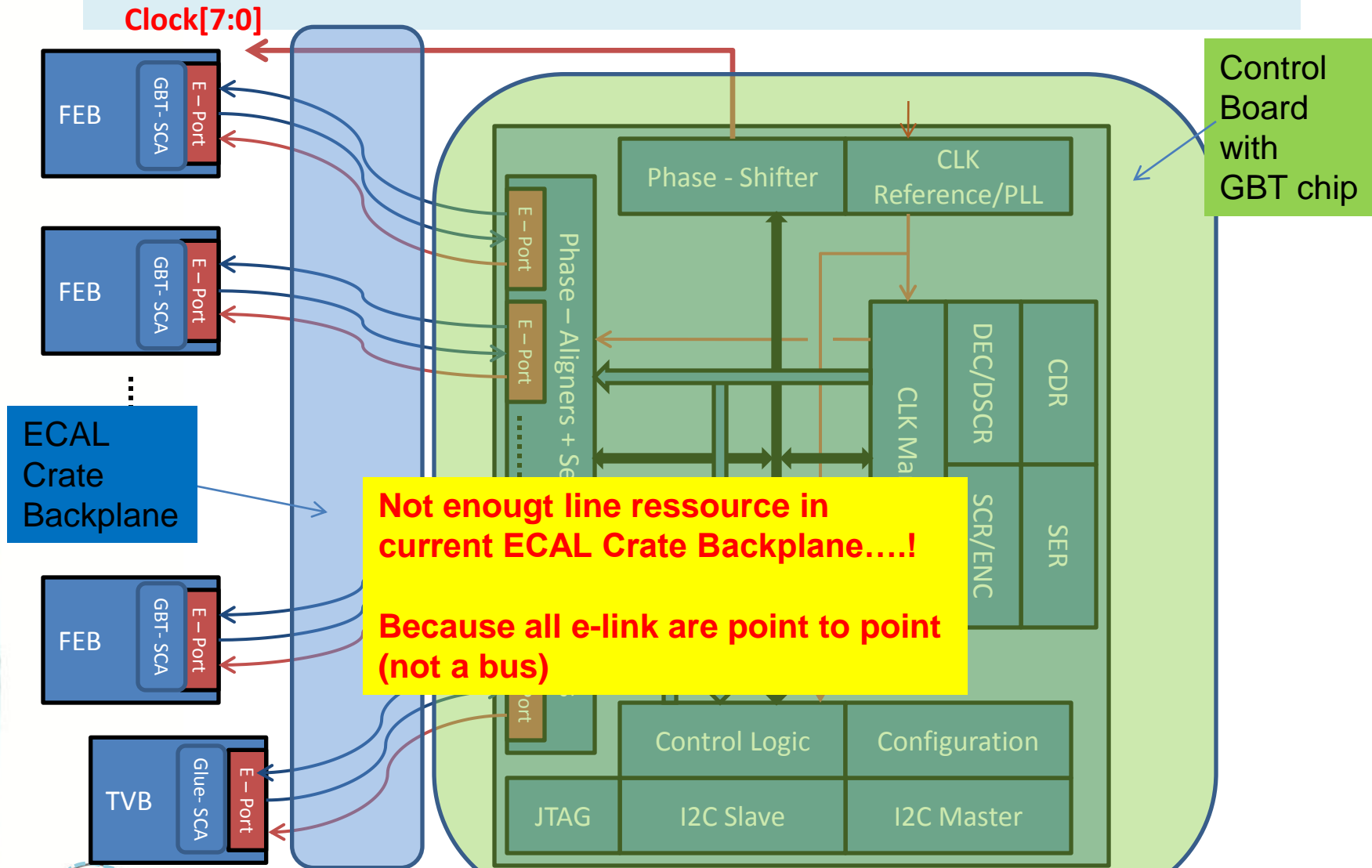


➤ LVDS Spare line Cannot use for upgrade

# TFC+ECS Interface to FE GBT link for upgrade



# TFC+ECS Interface to FE ECAL crate application



# TFC+ECSInterface to FE ECAL crate application

