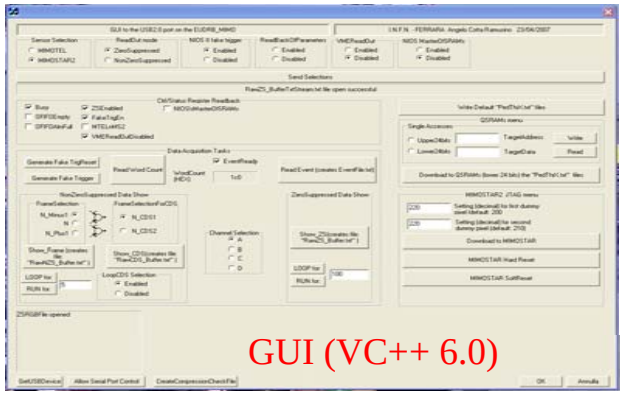
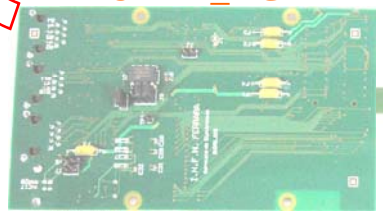


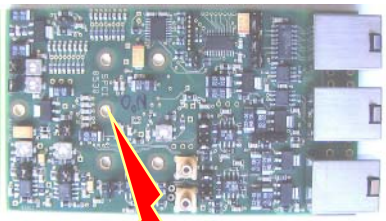
GUI (VC++ 6.0)

USB 2.0 auxiliary link

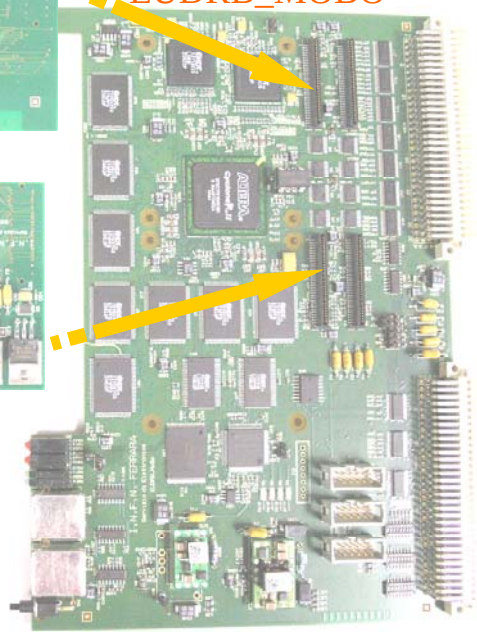
EUDRB_DCD



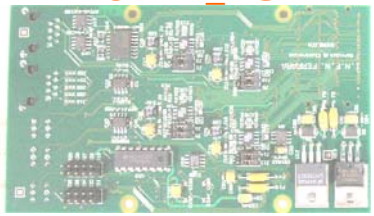
IRES-LEPSI MIMOStar2
(proto test board)

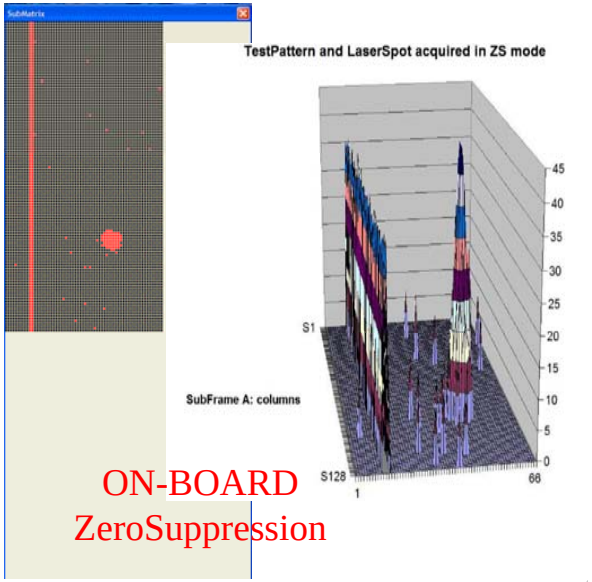


EUDRB_MOBO

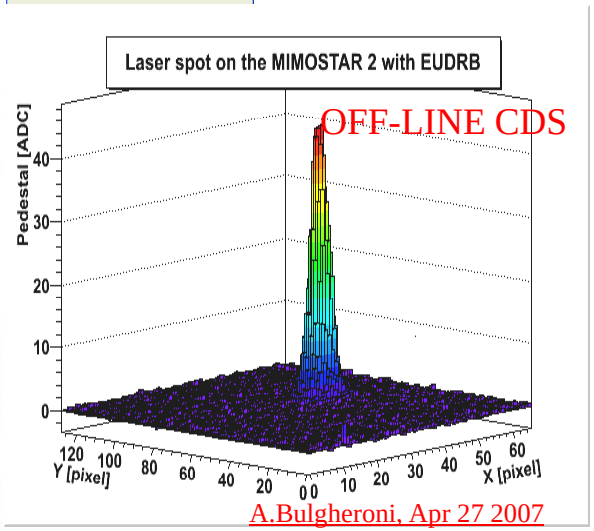


EUDRB_DCA





ON-BOARD
ZeroSuppression



OFF-LINE CDS

A.Bulgheroni, Apr 27 2007

EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMOSTAR2 sensors.
STATUS REPORT

EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

The "EUDRB-MIMO" is an EUDRB (EUDET Readout Board) whose FPGA configuration and the NIOS-II firmware have been designed (A. Cotta Ramusino) for interfacing with MIMO*2 and MIMOTEL sensors.

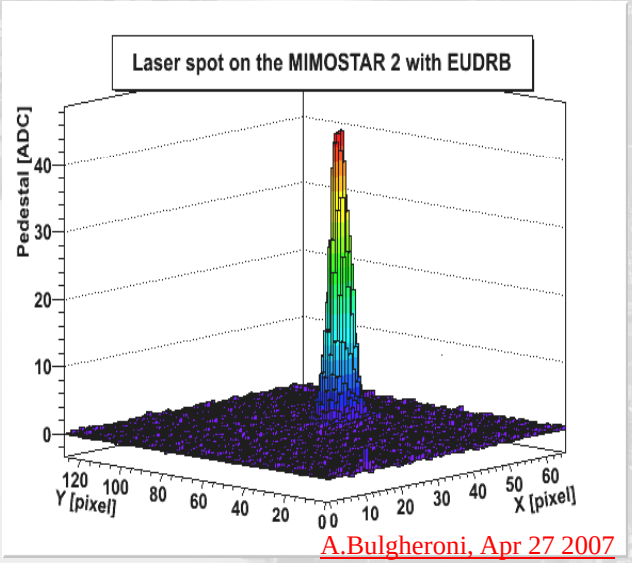
Progress since last review:

- April 27th: A team from "University of Insubria - Como" has set up a pulsed laser light source to test the readout of a MimoStar2 via a EUDRB-MIMO. Results are presented in the following.
- Beginning of May: 5 EUDRBs have been delivered by ARTEL . Details to follow.
- May 18th: EUDRB's TLU interface has been tested. Some bugs in the generation of the Trigger Number by the TLU have been spotted and have already been fixed by David Cussan.
- May 23rd: EUDRB#5, EUDRB#6 (new production lot) have been installed into the demonstrator's DAQ crate at the University of Geneva. EUDRB#3, acting as the TLU Interface, controls a private bus on the VME J2 to distribute trigger informations to the other EUDRBs in the crate.The system of the 3 EUDRBs can be readout at around 2 Hz with continuous TLU triggers (in Non Zero Suppressed mode with 3 frames readout per board per event).
- May 25th: PCBs of level adapters for MIMOTEL JTAG & timing signals have been received

Laser beam test results: OFF LINE CDS

- April 27th: A team from "University of Insubria - Como" has set up in Ferrara a pulsed laser source to test the readout of a MimoStar2 via a EUDRB-MIMO.

  Test conditions:
  - laser pulses synchronized to the fake trigger generated with each loop of the acquisition routine (controlled by the GUI written in Visual C++ 6.0 and running on notebook PC)
  - the routine looped 100 times, saving 3 raw frames per channel per event into a single "run" file.
  - The "run" file was processed by A. Bulgheroni with "SUCIMA Pix" to perform off line CDS and statistical analysis



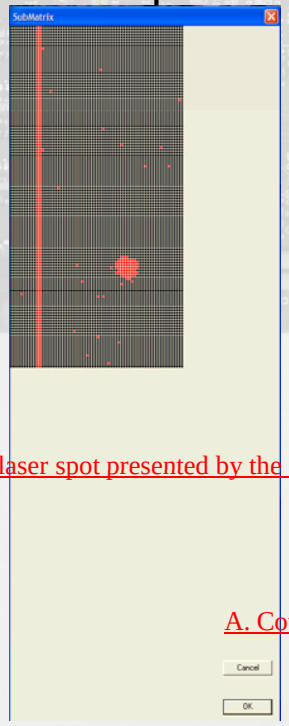
A.Bulgheroni, Apr 27 2007

Laser beam test results: ON BOARD Zero Suppression

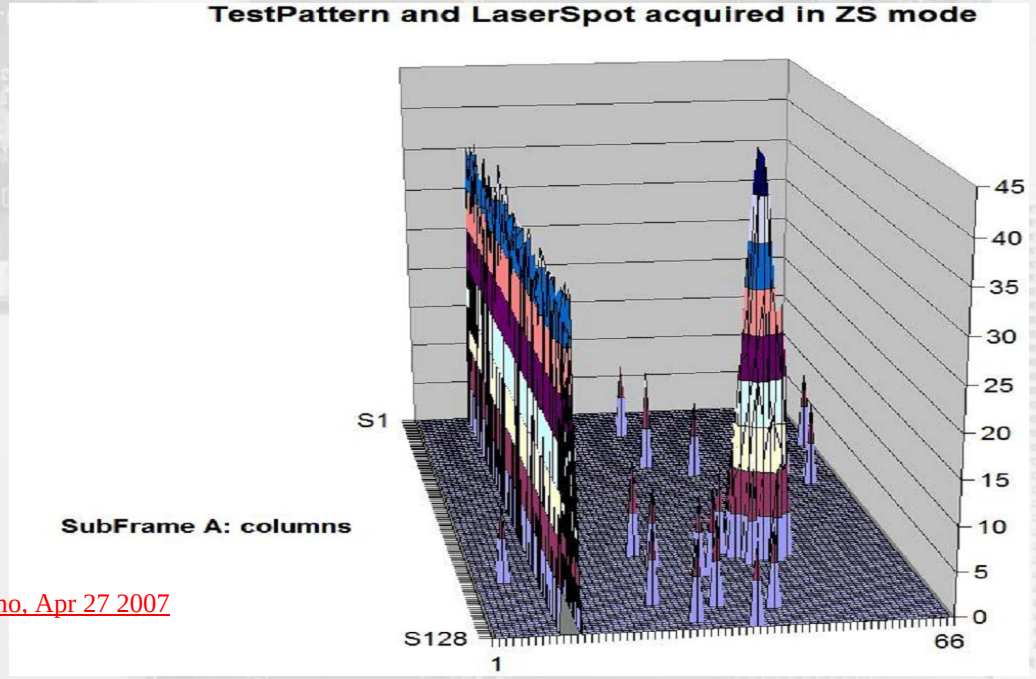
The image below is obtained by plotting the data from a single laser event captured by the EUDRB in Zero Suppressed mode.

The EUDRB is configured with ZS threshold=8 for each pixel and ZS pedestal=0 for each pixel except the 10th and 11th of each row (for channel A), for which the ZS pedestal=31.

Thus in the ZS event captured one can see the "confidence" pattern of pixels 10th and 11th of each row above threshold and then, of course, the signal from the laser pulse.



2D Image of the laser spot presented by the GUI



A. Cotta Ramusino, Apr 27 2007

EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

Status of the last production lot: 5 EUDRBs have been delivered by ARTEL .

All boards were affected by manufacturing problems going from misplaced components to poor solder joints .

The present status is :

- EUDRB#4: VME data bit 3 is inconsistent. Data collected through the USB2.0 link shows no apparent problems.
- EUDRB#5, EUDRB#6: tested OK for data taking with MIMOSTAR2
- EUDRB#7: two channels OK for data taking with MIMOSTAR2, two channels with coarse memory problems
- EUDRB#8: Nearly DEAD: the FPGA cannot complete initialization

A review of the manufacturing procedures has been undertaken to spot the sources of errors and avoid similar problems in the next production lots.

The debugging process continues, although at a lower priority level presently, and thus the boards might be recovered still.

The next production lot can anyhow be delivered by ARTEL in 8 WEEKS from the date of the order.

Installation and preliminary test of 3 EUDRBs in the VME crate for the demonstrator's test at DESY

The DAQ team at the University of Geneva has set up a VME crate with a Motorola CPU MVME6100 as the crate controller.

Presently the crate is hosting 3 EUDRBs:

- EUDRB#3: installed in slot3.

  It is configured as the TLU Interface board: it receives the trigger signal from the TLU and it provides the TLU with the Busy signals and the clock burst needed to obtain the EventNumber from the TLU.

  EUDRB#3 generates the Busy to the TLU based on its local condition and on the status of the open-collector line "TRIGBUSY_OC" to which all EUDRBs in the crate are attached.

  The EUDRBs which are not "TLU Interface" get their trigger pulse and read the EventNumber via a private backplane (driven by the TLU Interface) built over the VME J2 with cable segments and 2x32pin DIN connectors.
- EUDRB#5: installed in slot5
- EUDRB#6: installed in slot6

Preliminary loop tests achieved a sustained trigger rate of just above 1 Hz, with triggers generated by the TLU under software control as soon as the events were read from all 3 EUDRBs (3 NON-ZERO-SUPPRESSED frames per channel per board)

Installation and preliminary test of 3 EUDRBs in the VME crate for the demonstrator's test at DESY

The intended mode of operation for data taking is the "Zero Suppressed" mode, for which the FPGA starts extracting data above threshold as soon as the trigger is received.

The extraction continues for 1 frame time after the trigger is received (1,7ms @10MHz for a MIMOTEL), after which the "EventReady" flag of each board is set.

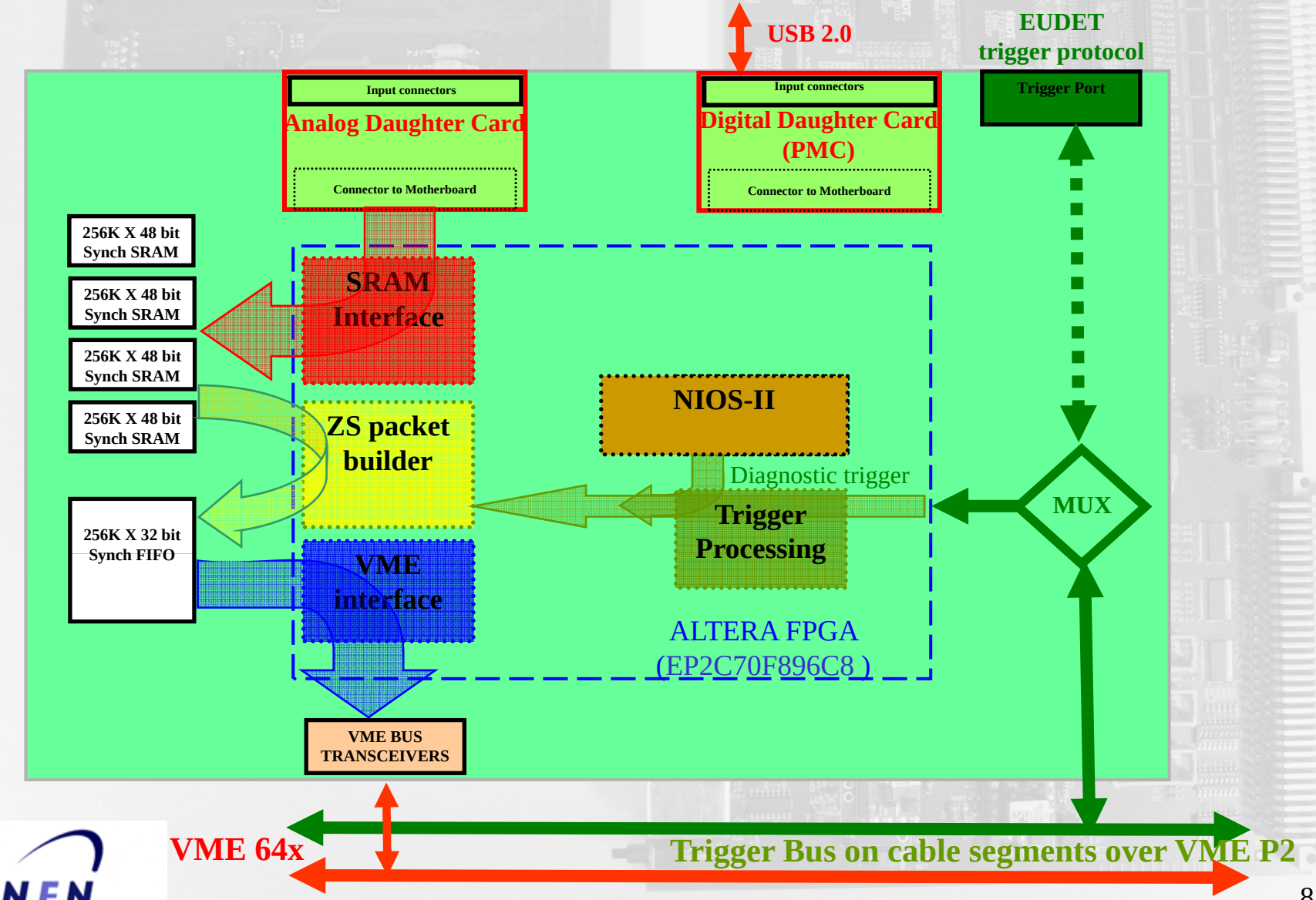
This is presently the smallest possible latency between trigger and start of readout, since it was chosen to have a complete packet to be readout in the output FIFO before issuing the "EventReady" flag.

An overview of the resources and the data paths interested in this operating mode is shown in the following slide (ZS mode overview)

As can be seen in slide 9 (MBLT loop) the execution rate of single-cycle-instructions, like the reading of the "EventReady" flag, must be increased to avoid compromising the overall throughput. The in-burst bandwidth of the MBLT reads is above 40MB/s as shown is slide 10 (MBLT detail)

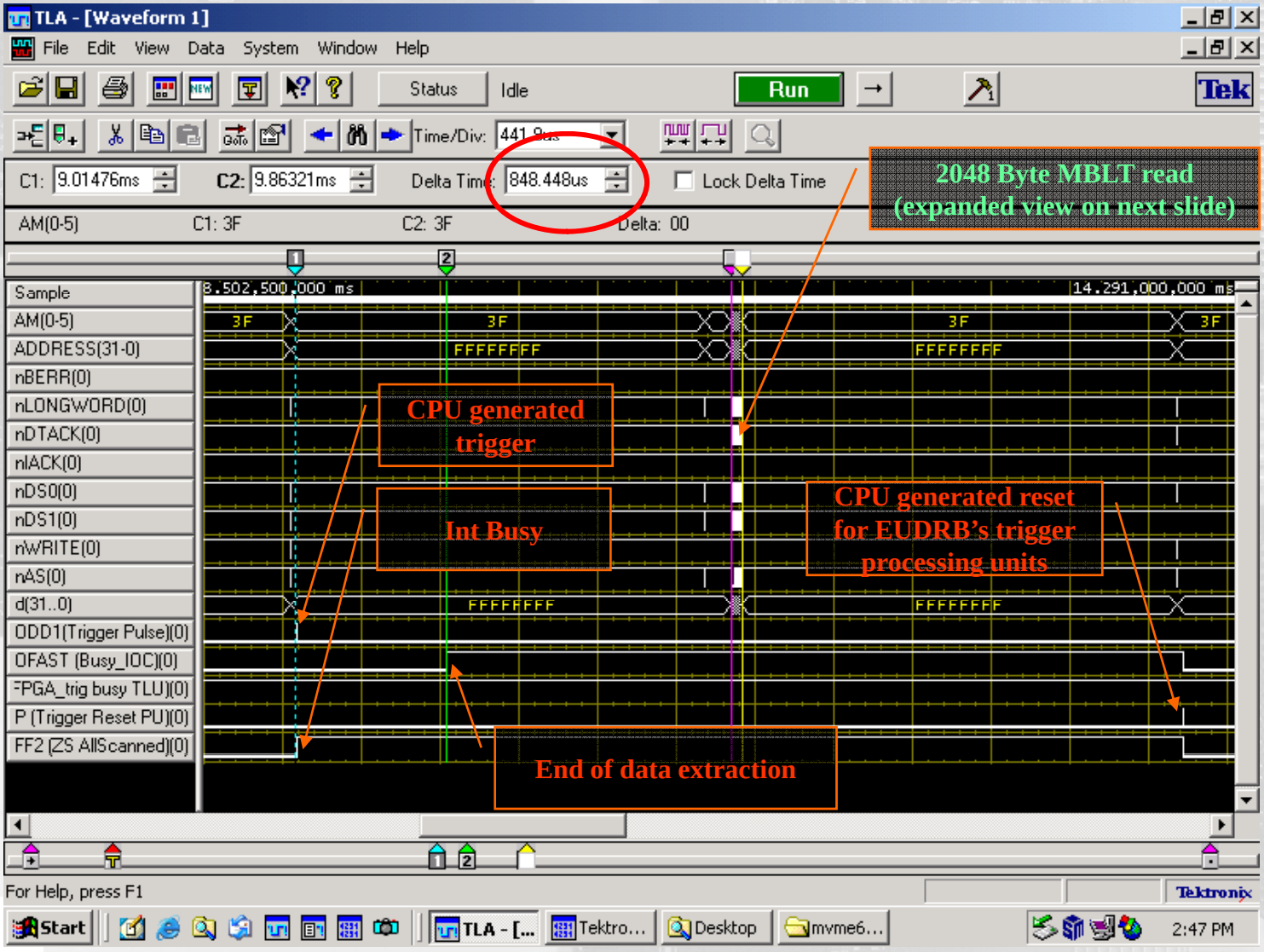
EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

Overview of Data Flow for ZS operation (mode for real data taking)



EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

Results from the workshop in Ferrara (Feb 26th): the VME CPU is running the "mimoloop" program by L.Chiarelli



EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

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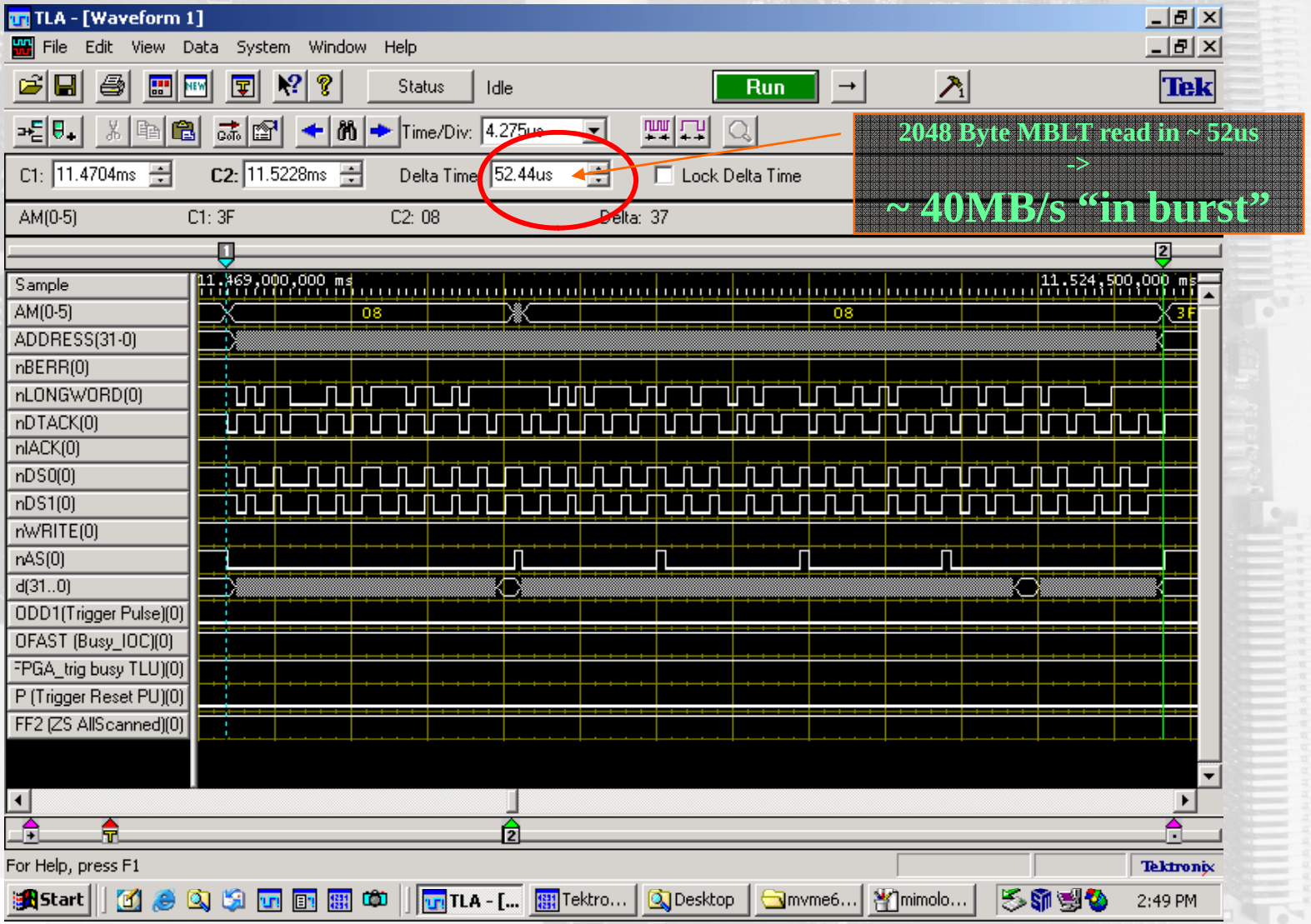


Installation and preliminary test of 3 EUDRBs in the VME crate for the demonstrator's test at DESY

On the other end, it is conceivable that the collaboration would want to use the boards in NonZero Suppressed mode at the beginning.
Presently the NIOS-II, for the sake of flexibility and testability needed in development, is in charge of transferring the contents of the pixel memories to the Output FIFO when serving a trigger in Non Zero Suppressed mode.
Since the NIOS-II needs a few us per word transferred, it causes the "EventReady" flag to be set with a large latency with respect to the trigger, in the order of a few tenth of a second, thus limiting the trigger rate capability.

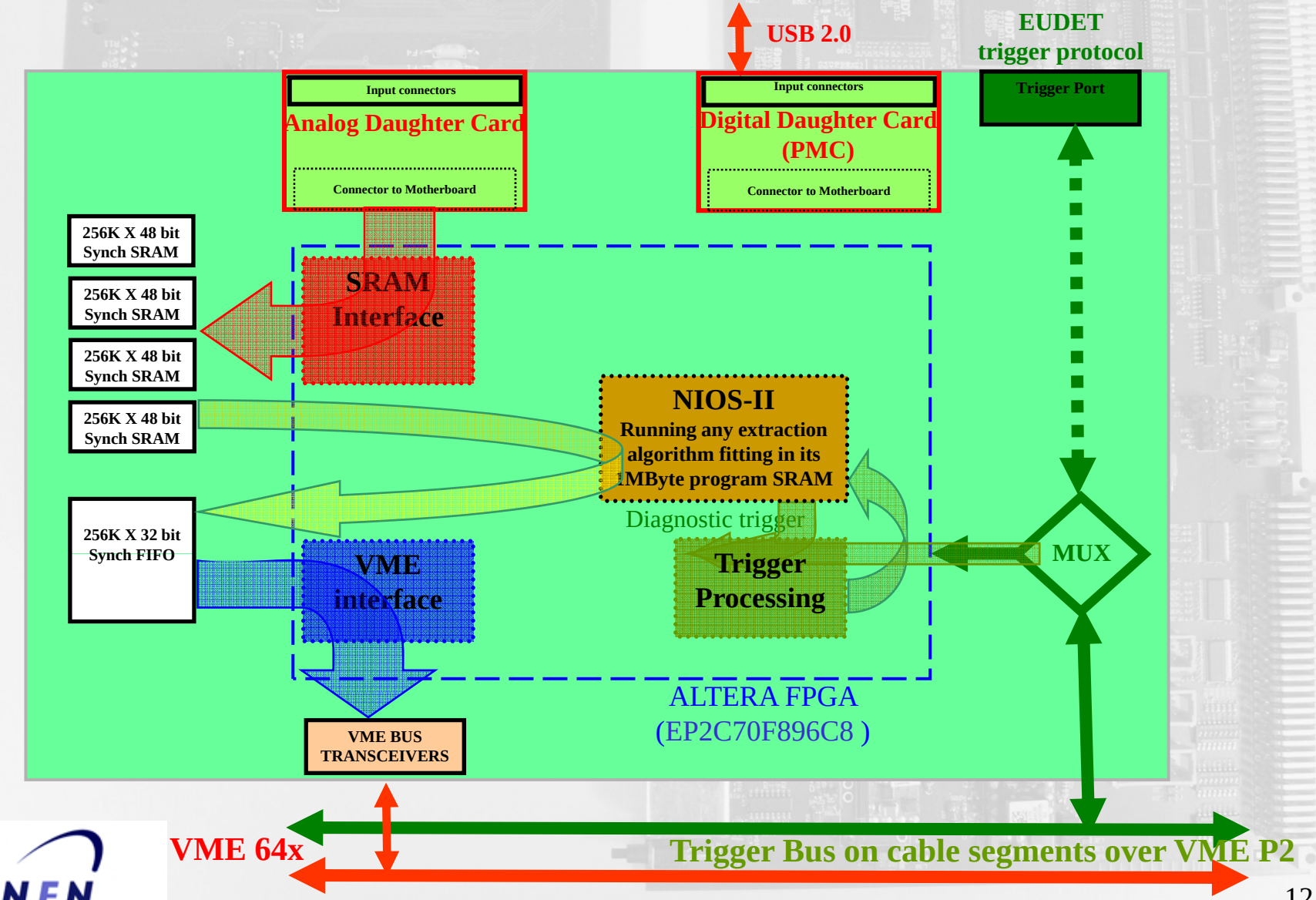
An overview of the resources and the data paths interested in the Non Zero Suppressed operating mode, as presently implemented, is shown in slide 12 (NZS mode overview)

The latency can be drastically reduced by designing a "NZS packet builder" (see slide 13, NZS packet builder overview) which could transfer pixel data to the output FIFO tens of times faster than the NIOS-II's.

The "NZS packet builder" block could be implemented (A. Cotta Ramusino) in time for the test beam in August.

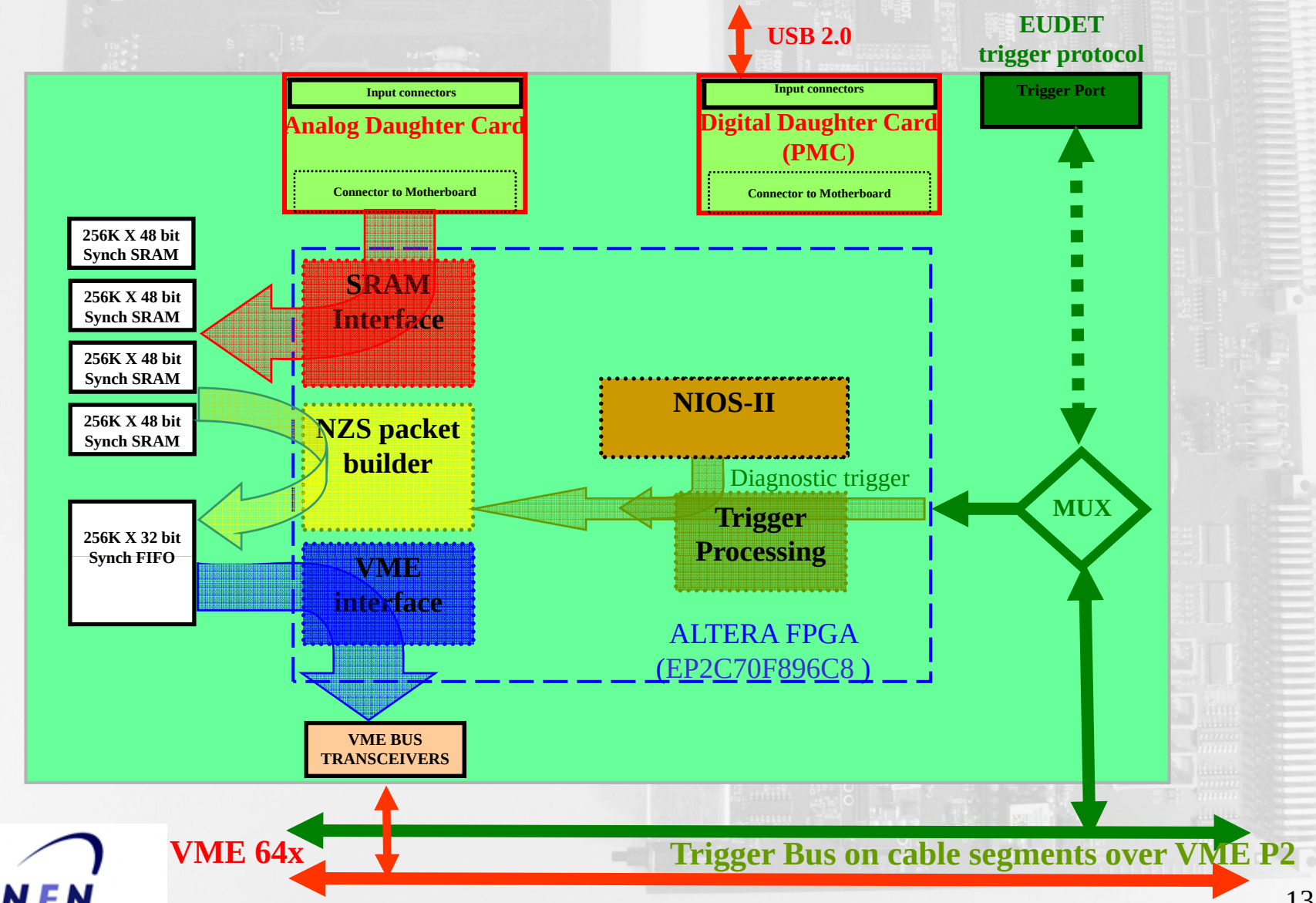
EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

Overview of Data Flow for presently implemented NZS readout via VME

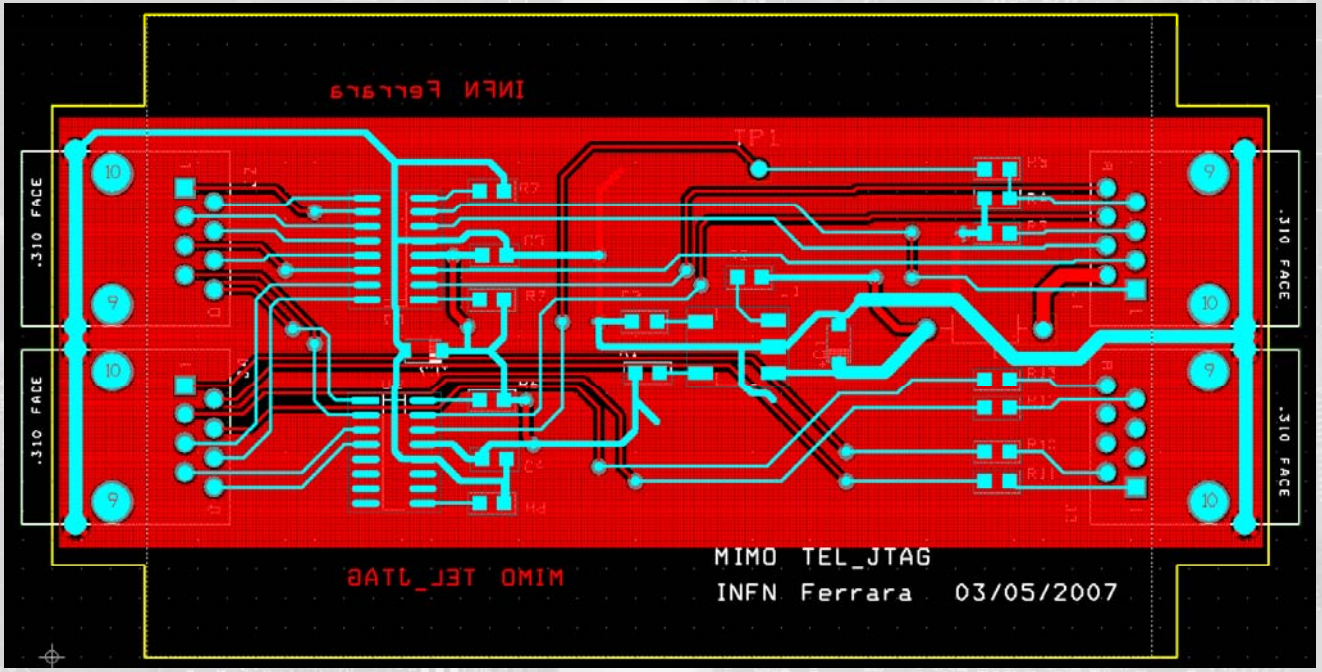


EUDRB-MIMO: A VME-64x based DAQ card for MIMOTEL/MIMO*2 sensors

Overview of improved Data Flow for NZS readout via VME



PCBs of level adapters for MIMOTEL JTAG & timing signals:



10 PBCs have been received on May25th. Components needed are all in-house. PCB stuffing can start June 1st.

The MIMOTEL-JTAG level adapters are powered from pin 2 of the J3 connector on the EUDRB_DCD …. → a small patch (remove one resistor and run a wire) is needed on all EUDRB_DCD.

Next Milestones:

EUDRB-MIMO (A. Cotta R.):

- Test the EUDRB-MIMO JTAG interface to the MIMOTEL on the prototype pro-tempore in Ferrara
- Design, integrate and test the "NZS packet builder block"
- Pedestal noise analysis on the MIMOTEL to characterize the noise performance of the EUDRB A/D section

System tasks (L. Chiarelli):

- Complete and test the installation of the new ELinOS release
- Optimize the library of functions for the VME CPU to perform:
  - generic housekeeping of the EUDRB
  - continuous data taking with pedestal noise analysis