Final Sensors for EUDET Telescope: Progress Report

Evolution since March '07

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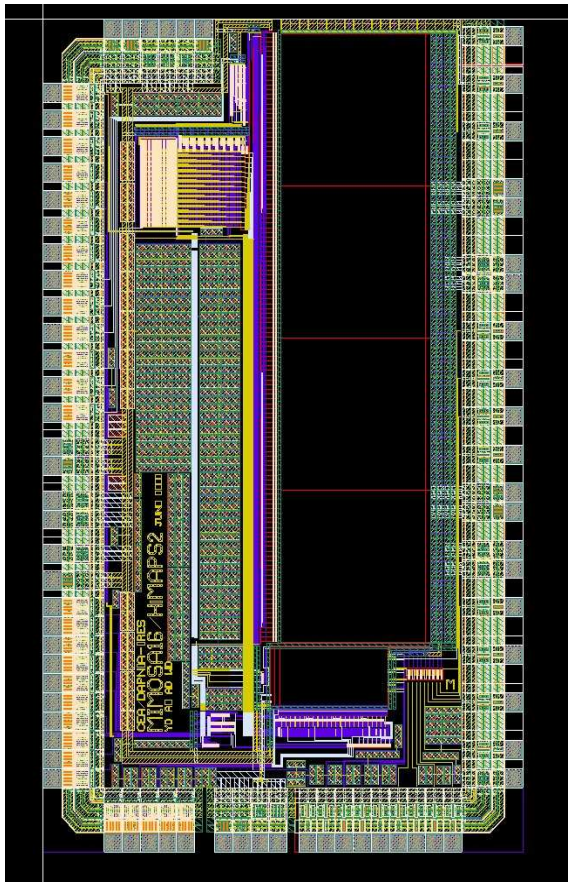
on behalf of DAPNIA-Saclay & IPHC-Strasbourg

OUTLINE

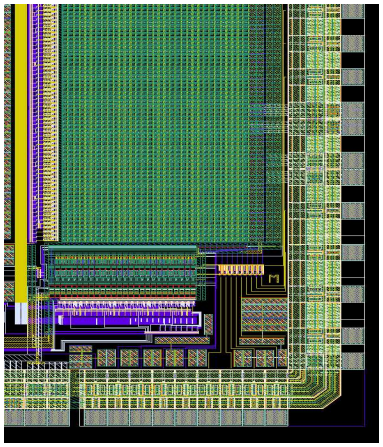
- MIMOSA-16: status of set-up for digital output tests
- MIMOSA-22: status of design
- ∅ micro-circuit : status of 1st prototype design
- Summary

Tests of MIMOSA-16

- **MIMOSA-16 design features :**
  - **AMS-0.35 OPTO translation of MIMOSA-8**
    $\hookrightarrow \sim$ **11–15** μm **epitaxy instead of** $\lesssim$ **7** μm
  - **32 // columns of 128 pixels (pitch: 25** μm**)**
  - **on-pixel CDS (DS at end of each column)**
  - **24 columns ended with discriminator**
  - **4 sub-arrays :**
    - **S1 : like MIMOSA-8 (1.7x1.7** μm^2 **diode)**
    - **S2 : like MIMOSA-8 (2.4x2.4** μm^2 **diode)**
    - **S3 : S2 with ionising radiation tol. pixels**
    - **S4 : with enhanced in-pixel amplification**
      (against noise of read-out chain)



$\Rightarrow$



- **Preliminary tests of analog part ("20** μm**" epitaxy) performed in Saclay (shown previously):**
  - **sensors illuminated with** ^{55}**Fe source and** $F_{r.o.}$ **varied up to** $\gtrsim$ **150 MHz**
  - **measurements of N(pixel), FPN (end of column), pedestal variation, CCE (3x3 pixel clusters) vs** $F_{r.o.}$
- **Tests of analog part ("14** μm**" epitaxy) in Saclay** $\rightarrowtail$ **results (CCE)**
- **Next steps :**
  - **digital part** $\geq$ **June at IPHC**
  - **beam tests** $\gtrsim$ **4 Septembre at CERN (T4 – H6)**
- **Later on : tests of sensors produced in 2nd batch**

MIMOSA-16 : Status of Test Preparation

- Setting-up of tests of the digital part of MIMOSA-16 (2006 run) under way

  $\longmapsto$ set-up expected to be completed around mid June

- Preparation of SPS beam tests (start Sept. '07)

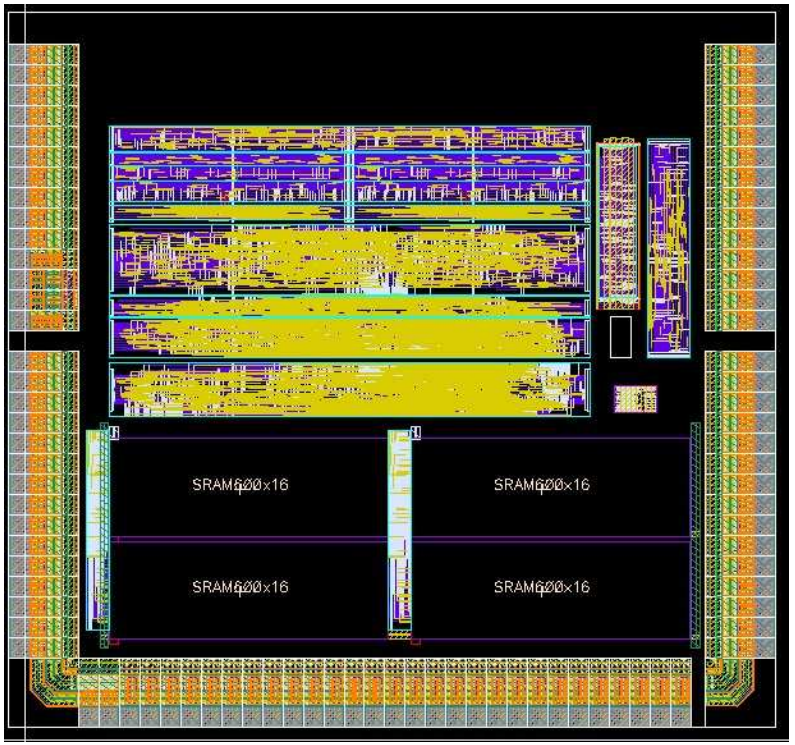
- Submission of modified version of MIMOSA-16 :

  ⁂ sub-arrays S1, S2 and S3 with enlarged sensing diodes in ordre to increase CCE ($\gtrsim$ 3x3 μm^2)

  $\longmapsto$ submitted for fabrication by end of April $\longmapsto$ back from foundry $\gtrsim$ mid July

1st chip (SUZE-01) with integrated $\emptyset$ and output memories (no pixels) :

- 2 step, line by line, logic :
  - step-1 (inside blocks of 64 columns) :
    identify up to 6 series of $\leq$ 4 neighbour pixels per line
    delivering signal $>$ discriminator threshold
  - step-2 : read-out outcome of step-1 in all blocks
    and keep up to 9 series of $\leq$ 4 neighbour pixels
- 4 output memories (512x16 bits) taken from AMS I.P. library
- surface $\sim$ 3.5 x 3.6 mm^2 $\longrightarrow$ $\sim$ 8 keuros (EUDET budget)



Status :

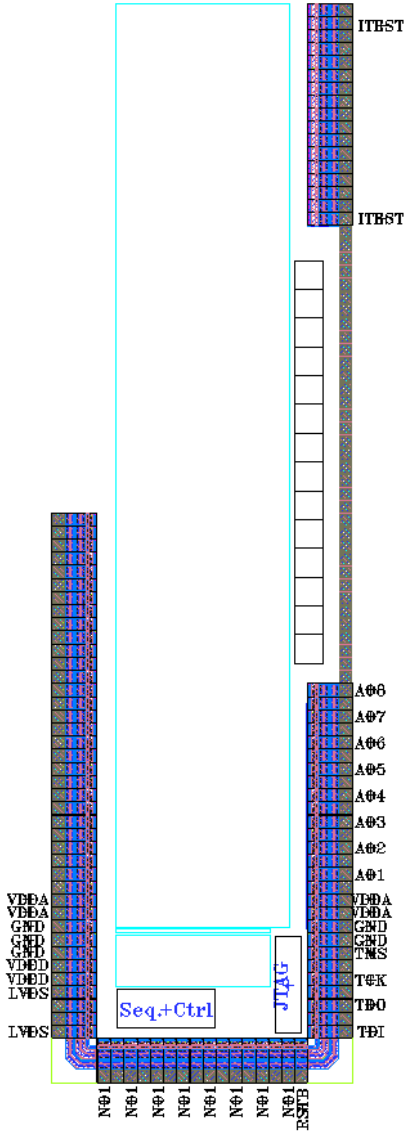
- design $\sim$ completed $\longrightarrow$ post-simulations under way
  $\longrightarrow$ progress achieved allows submission on schedule (end of June)
- back from foundry end of Sept. $\longrightarrow$ tests completed by end of year

- Next prototype with column // architecture : MIMOSA-22

♣ **Extension of MIMOSA-16 $\longmapsto$ larger surface, smaller pitch, optimised pixel, JTAG, more testability**

Pixel characteristics (still under study) :

- ✳ pitch : 18.4 μm (compromise resolution/pixel layout)
- ✳ diode surface : $\sim$ 10–20 μm^2 to optimise charge coll. & gain
  (feedback from M-16')
- ✳ 64 columns ended with discriminator
- ✳ 4–8 columns with analog output for test purposes
- ✳ $\geq$ 8 sub-matrices : $\geq$ 4 pixel designs w/o ionising rad. tol. diode
  $\Rightarrow$ active digital area : 64 x 544/576 pixels ($\lesssim$ 12.5 mm^2)



Testability (still under devt) :

- ✳ JTAG + bias DAC $\longmapsto$ programmable chip steering
- ✳ 2 additionnal DC voltages to emulate pixel's output
  for independent discriminator performance assessment
- ✳ output frequency $\leq$ 40 MHz

Status :

- ✳ Design under way $\longmapsto$ submission end of Sept. '07 seems realistic
- ✳ Funding ($\lesssim$ 30 keuros) via IPHC (CBM) and DAPNIA resources

SUMMARY

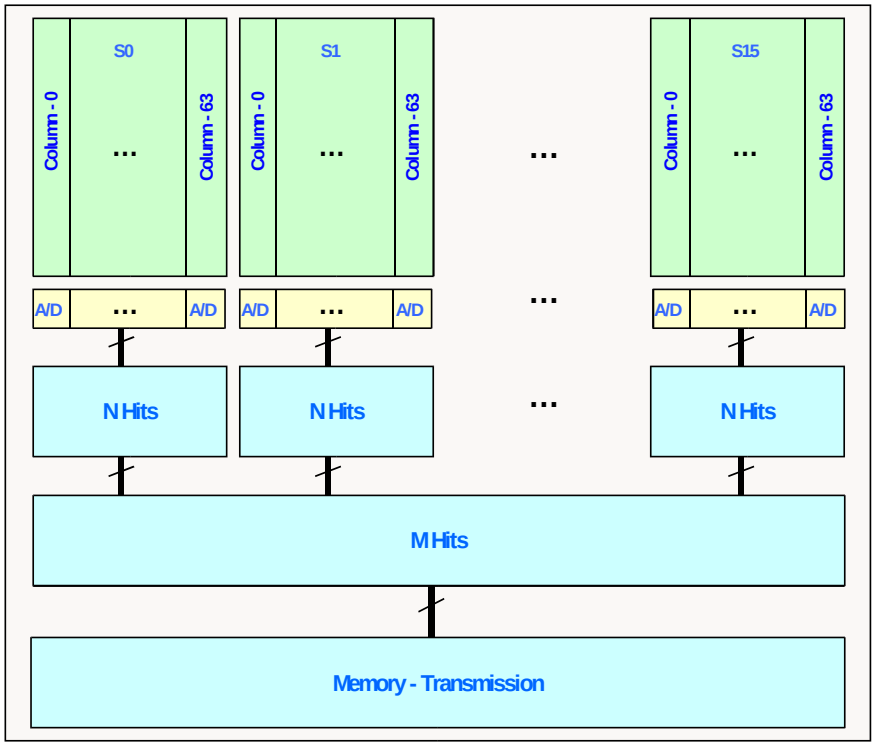
- **MIMOSA-16 tests :**
  - ⁂ **lab tests of digital part in June-July**
  - ⁂ **beam tests in Septembre $\longmapsto$ feedback for MIMOSA-22**
  - ⁂ **resubmission with larger sensing diodes (S1, S2 and S3) $\longmapsto$ in time for feedback for MIMOSA-22 ?**

- **MIMOSA-22:**
  - ⁂ **changes w.r.t. M-16 in pitch, surface, testability, JTAG being implemented**
    $\longmapsto$ on schedule for submission to foundry by end of Sept. '07
  - ⁂ **funding ($\lesssim$ 30 keuros) via IPHC/GSI and DAPNIA resources**

- **$\emptyset$ suppression micro-circuit :**
  - ⁂ **design well advanced $\longmapsto$ on schedule for submission by end of June**
  - ⁂ **funding ($\sim$ 8 keuros) via EUDET**

Zero Suppression : SUZE-01 Block Diagram

Chip readout architecture including digitization and zero suppression



Block diagram of readout architecture

- Pixel array : 1024x1024 pixels Readout row by row The row is divided into 16 groups
- Analog to digital conversion at the bottom of each column (Discriminator or ADC)

Zero suppression algorithm :

- Find N Hits for each group
  Find M Hits for each row
  (With N and M determined by pixel array occupancy rate)
- Memory wich stores M hits and serial transmission

- Submission of a small size fully digital prototype in AMS 0.35 µm in June 2007

Roadmap towards the Final Chip

Spring 2008 : MIMOSA-22+

- MIMOSA-22 complemented with $\emptyset$ (SUZE-01)
- 1 or 2 sub-arrays (best pixel architectures of MIMOSA-22)
- larger surface : active surface $\sim$ 0.5 cm^2
  - $\backsimeq$ final column depth (544/576 pixels)
  - $\backsimeq$ $\gtrsim$ 1/4 of final number of columns ($\geq$ 256 / 1088)
- total surface $\lesssim$ 5.5 x 12 mm^2 $\rightarrowtail$ 50 – 55 keuros

  $\hookrightarrow$ available funding : EUDET (27 keuros) $\&$ STAR/CBM (rest)

▶ opportunity for engineering run (100 keuros) combining various chips

End 2008 / early 2009 : Final chip

- Extension of MIMOSA-22+
- Active surface : 1088 columns of 544/576 pixels (20.0 x 10/10.5 mm^2)
- Read-out time $\lesssim$ 100 μs
- Chip dimensions : $\sim$ 20 x 12 mm^2
- Engineering run : $\sim$ 120 keuros for 6 diced and thinned wafers

  $\hookrightarrow$ available funding : EUDET (70 keuros) & STAR/CBM (50 keuros)