THE REALISATION AND OPPORTUNITIES OF AN EDUCATIONAL CLEANROOM FOR ENGINEERING TRAININGS AND HIGH-TECH PROJECTS IN CLOSE COLLABORATION WITH THE SEMICONDUCTOR ECOSYSTEM

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Europe has started to initiate, expand and strengthen Chip Competence Centers in several countries since the European Chip Act announcement in 2022 [1]. The Netherlands has initiated in 2024 the program "Operation Beethoven" to build-up training centers with the mission to educate and train technical students at different educational levels for the semiconductor industry [2].

Currently, a professional ISO-7 cleanroom is realized at The Hague University of Applied Sciences in Delft in collaboration with vocational schools, academic universities and other universities of applied sciences in the South-Holland region. The new 100 m^2 cleanroom consists of two sectors: (1) a 'microfabrication sector' for lithography process flows and micron-scale metrology, and (2) an 'assembly & testing sector' for working on macroscopic high-precision semiconductor equipment and related subsystems. Additionally, a classroom is realized dedicated to theory modules as well as courses on design, modelling and simulation software which are relevant for the microchip ecosystem.

In this presentation, I will explain how this cleanroom enables interdisciplinary education, training opportunities to develop hands-on skillsets, and cross-functional collaborations within the microchip ecosystem. I will elaborate on examples of cleanroom activities for students at different competence levels [3], from basic cleanroom trainings to innovative applied research projects (e.g., in collaboration with internal research groups, external research institutes, startups/scale-ups and SMEs). The new cleanroom will provide students unique opportunities to get-to-know the microchip ecosystem, and to connect to semicon professionals at companies who can support -and possibly guide- young professionals to start a career in the semiconductor industry.

[1] European Commission. A chips act for Europe. https://www.european-chips-act.com/COM_2022_45_1_EN.pdf
[2] Gerichte groei voor semicon-talent in de regio Delft – Nationaal Versterkingsplan Microchiptalent Regioplan Zuid-Holland Delft. https://www.dehaagsehogeschool.nl/media/beethoven-regioplan-zuid-holland-delft-30-september-2024
[3] Jeroen B. Oostinga. Lithography challenges for physics and engineering students to become competent, skillful microtechnologists for the semiconductor industry. Proceedings of the PTEE 2024. https://opus4.kobv.de/opus4-rosenheim/files/2581/PTEE2024_Oostinga_LITHOGRAPHY_CHALLENGES_FOR_.pdf