Firmware approach for TEL62 trigger and data acquisition board

B. Angelucci[1,2], E. Pedreschi[2], F. Spinella[2], M.Sozzi[1] , S. Venditti[1,2]

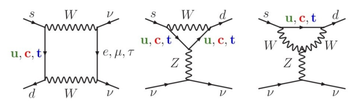
([1] University of Pisa, [2] INFN sez. Pisa)

From theory to experiment

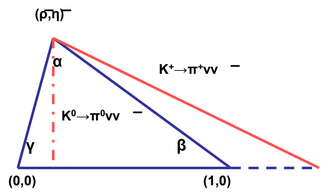
- $K^+ \to \pi^+ \nu\bar{\nu}$ process is unique as extremely accurate and clean probe for the non-trivial flavour structure of physics beyond the Standard Model
- $K^+ \to \pi^+ \nu\bar{\nu}$ is computed in a clean theoretical environment due to the small contribution by hadronic matrix elements and long distance terms.

Main backgrounds

$BR(K^+ \to \pi^+ \pi^0)$	$20.7 \cdot 10^{-2}$
$BR(K^+ \to \mu^+ \nu)$	$63.5 \cdot 10^{-2}$
$BR(K^+ \to e^+ \pi^0 \nu)$	$5.1 \cdot 10^{-2}$
$BR(K^+ \to \mu^+ \pi^0 \nu)$	$3.4 \cdot 10^{-2}$

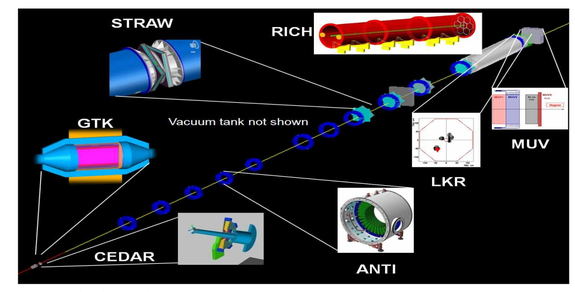


$BR(K^+ \to \pi^+ \nu\nu) = (8.22 \pm 0.84) \cdot 10^{-11}$



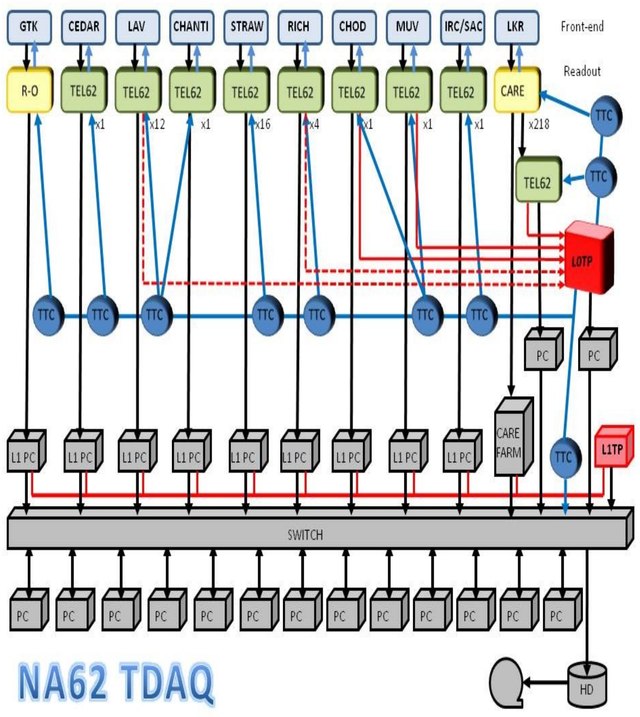
- **NA62** aims at measuring $K^+ \to \pi^+ \nu\nu$ with O(100) SM events, in two years of data taking
- Very challenging experiment. With stringent requirements:
  - **high-resolution timing** (high-rate environment)
  - **particle identification** (kaons, pions, muons,electrons, photons)
  - **hermetic vetoing**
  - **redundancy** of information

- The K+ component in the beam is identified with respect to the other beam particles by an upgraded differential Čerenkov (**CEDAR**) counter
- The coordinates and momentum of individual beam particles are registered before entering the decay region by 3 silicon pixel tracking detectors (**GTK**)
- Guard-ring' counters (**CHANTI**) surrounding the last GTK station veto charged particles upstream of the decay region
- A large-acceptance, magnetic spectrometer with tracking detectors (**STRAW Tracker**) in vacuum are required to detect and measure the coordinates and momentum of charged particles originating from the decay region.
- A ring-imaging Čerenkov (**RICH**) counter to identify pions with respect to muons
- A muon-veto detectors (**MUV**), composed of a two-part hadron calorimeter followed by additional iron and a transversally-segmented hodoscope



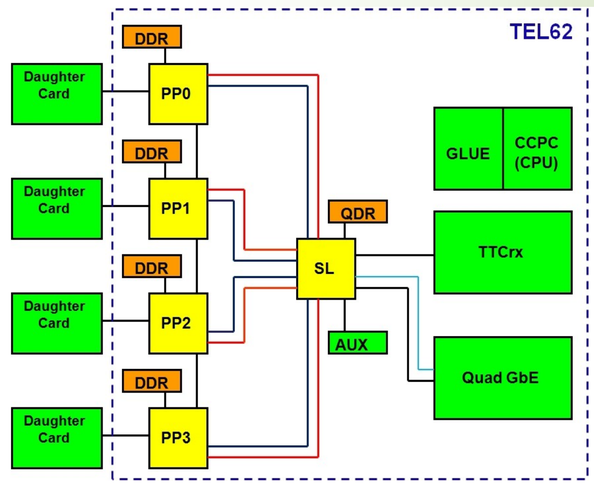
- A set of photon-veto detectors provides hermetic coverage from zero out to large (~50mr) angles from the decay region. This is assured by the existing, high-resolution, e.m. (**LKR**) calorimeter, supplemented, at small and forward angles, by intermediate ring (**IRC**) and small-angle (**SAC**) calorimeters and, at large angles, by a series of annular photon-veto (**LAV**) detectors.

The Trigger-DAQ System (TDAQ)



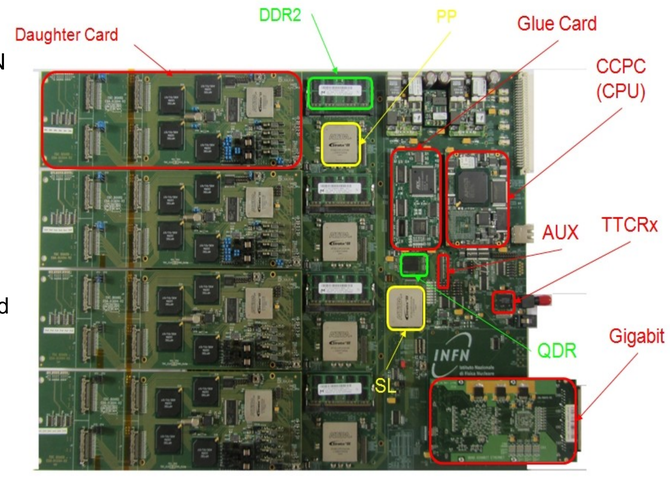
- The Trigger and DAQ System is based on a common board (TEL62)
- Each board provides support both for acquisition and generation of trigger primitives.
- Special mezzanines for TEL62 (mainly TDCs) interface with sub-detectors front-ends.
- TEL62 provides asynchronous GbE data transmission (4Gb/s) and receives synchronous trigger requests via TTC standard
- Trigger primitives are sent to the L0 processor
- Event building is performed by a PC farm.

TEL62 Architecture



- 4 Daughter Cards (DC):
  - TEL62 is able to host both the old LHCb daughter-cards and the new TDCb daughter-cards
  - most sub-d need TDCs: 1 TDCb card = 4 CERN HPTDCs (128 channels) => 4 TDC cards per TEL62 => 512 channels per TEL62
- 4 PP- FPGAs:
  - each one connected to one of the daughter cards
  - DDR2 external buffer memories used for data storage during the L0 trigger latency
  - connected to SL-FPGA with 2 independent 32-bit buses (separate paths for trigger primitives and readout data streams)
- SL-FPGA:
  - Receives trigger primitives from each PP, merges and send them to Level0 central processor via Quad-GbE mezzanine
  - Receives and merges data from PPs, performs data reduction

- AUX:
  - 2 indipendent 16-bit buses allow an expansion of the board capabilities (e.g. board to board communication through serializers)
- CCPC (CPU):
  - Embedded Credit Card PC handles the TEL62 slow control and configuration (running Linux)
- TTC:
  - Standard LHC connection for trigger and clock (CERN TTCrx module)
- Quad GbE:
  - GbE network card (4 links) allows a simple data collection on PCs
  - Inter-board connection could be implemented by using 2 of the 4 GbE links



TEL62 firmware block diagram

- PP Data Flow:
1. Each PP merges the data coming from 4 TDC boards
2. Data are received in the 4 PP FPGA from TDC boards in packets. Each packet contains the hits of the previous 6.4 μs (time window)
3. Each time window is splitted in 256 time slices of 25 ns each. Internal RAMs, 128 x 32 bits are reserved for each time slice. Each hit is copied in the first available word of the relative RAM
4. At the end of the window data readout the 256 RAMs are copied in the DDR2, while the new data coming from the TDCs are copied in a second set of RAMs (double buffering technique). The DDR2 is organized as a circular buffer, capable of storing 52 ms of data
5. The number of words received for each slice (counters) is also copied in a different portion of the DDR2

- PP Trigger Flow:
1. Data from TDC boards are merged and stored in a FIFO. Algorithms specific for each sub-detector are applied. The obtained trigger primitives are sent to the SL FPGA through a dedicated bus

- SL Data Flow:
1. Whenever the TTCRx receives a trigger it distributes it to all the FPGAs. Trigger latency is fixed and known. For each trigger the hits relative to a small number of time slices around the event time are retrieved from the DDR2 and sent to the SL
2. The SL collects and merges the data coming from the 4 PPs. Eventually data relative to several events (Multi Events Packets) are also merged. The packets are completed with an header and sent to one of the Gbit links that transmits the data to the PC farm

- SL Trigger Flow:
1. The SL receives trigger primitives from the 4 PPs, merges all of them in a MTP (Multiple Trigger Packet) , adds an header and send the packet to one of the Gbit links that transmits it to the L0 trigger processor

elena.pedreschi@infn.it, franco.spinella@infn.it