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firmware approach for TEL62 trigger and data acquisition board

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The main goal of the NA62 experiment at the CERN SPS is to measure the branching ratio of the ultra-rare K+ $\longrightarrow \pi+\nu\nu$ decay, collecting about 100 signal events in 2 years. Readout uniformity of sub-detectors, scalability, efficient online selection and loss-less readout at high rate are key issues. The TEL62 is the principal block of the Na62 DAQ and his architecture is based on a star topology.
Tel62 collects data coming from the sub-detectors, process and temporary stores them in a buffer extracting only the ones requested by the trigger system.
The complete dataflow is described.

Summary

The NA62 experiment at the CERN SPS aims at measuring the kaon decay
K+ $\longrightarrow \pi+\nu\nu$ as a highly sensitive test of the Standard Model (SM) and a search for New Physics. The detection of this process is very difficult due to the smallness of the signal and the presence of a very sizeable background.
NA62 aims to collect about 100 signal events in about 2 years of data, thanks to many detectors distributed along the 65 m fiducial decay region: GTK and STRAW are used for K+ and π+ tracking , CEDAR and RICH for particle identification while LAV, LKR and MUV as vetos for photons, positrons and muons. A scintillator hodoscope (CHOD) acts as a fast timing and trigger device.
The timing measurements of the signals coming from most of these detectors together with coincidence algorithms are used for trigger and data acquisition. The principal blocks used for this purposes are the HPTDC (High Performance Time to Digital Converter) chip, developed by CERN and hosted on a mezzanine card and the trigger and data acquisition board (TEL62)
The TEL62 is the principal block of the NA62 DAQ and about 100 cards will be mounted on the experiment. The board architecture is based on a star topology: 4 FPGAs, named Pre-Processing (PP) are connected to a single FPGA named SynkLink (SL). The 4 PPs are directly connected to 4 TDC mezzanines, each one hosting 4 HPTDC while the SL is connected to a gigabit interface hosted on another mezzanine.
The firmware for the TEL62 will be based on a common framework while each sub-detector group will be responsible for the customization of the interface to their own front-end electronics.
The amount of data arriving from the TDCs can be huge, depending on the sub-detector up to few MHz per channel. They are organized in packets; each related to "time windows" of 12.8 us. Whenever a trigger arrives the data that are up to 50 ns around the trigger timestamp are collected and sent to a farm of computers that perform additional cuts and eventually store the event.
The PP FPGA has the not easy duty of collecting and merging the data and then to organize all of them on the fly in a 2 GB DDR2 memory, where each page is related to a well defined 25 ns window. Following a trigger the right data are extracted from the memory and sent to the SL FPGA.
The PP FPGA's data are synchronized inside the SL FPGA, pre-processed and stored in a 1MByte QDR SDRAM who sends them to a 4 links Gigabit Ethernet hosted in a custom daughter card, the memory operates also like a buster in case of elevate trigger rates.
The details of the dataflow and firmware organization are described.

Primary author: PEDRESCHI, Elena (Sezione di Pisa (IT))

Co-authors: ANGELUCCI, Bruno (Sezione di Pisa (IT)); SPINELLA, Franco (Sezione di Pisa (IT)); SOZZI, Marco (Sezione di Pisa (IT)); VENDITTI, Stefano (Sezione di Pisa (IT))

Presenter: PEDRESCHI, Elena (Sezione di Pisa (IT))

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