SEU tolerant latches design for the ATLAS pixel readout chip

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On behalf of the ATLAS PIXEL Upgrade FE-I4 collaboration

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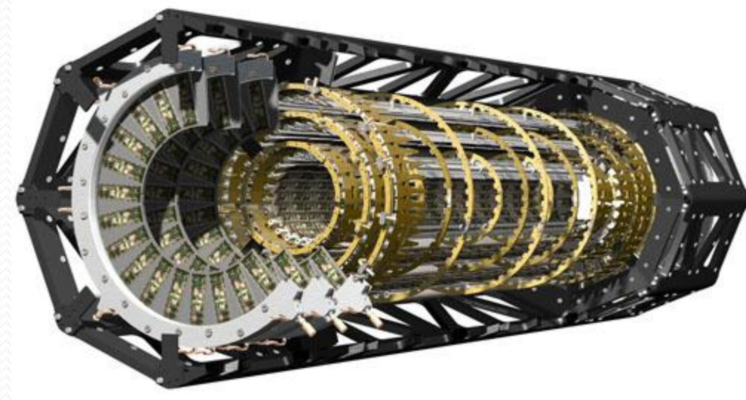
Outline

- Introduction
  - Motivations, Specifications and Description of the FEI4 chip
- The present design for the insertion of B-Layer
  - Memory Cell structure used in the FE-I4 chip
  - Pixel configuration
  - Chip configuration
  - Experimental test setup and main results
- The future design
  - Motivations of using the 65 nm process
  - Chip Prototype for ATLAS pixel
  - Organisation of the Configuration Memory
  - SEU test results
  - Dose effects
- Conclusion and perspectives

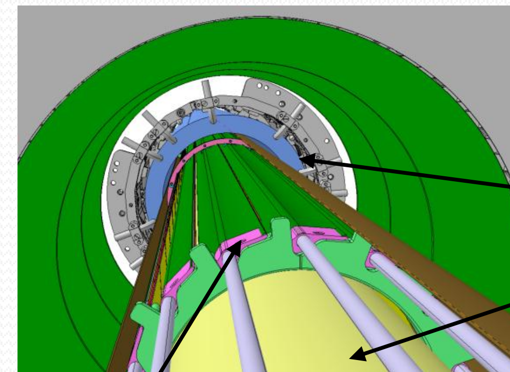
Motivations

- Two applications are foreseen for FE-I4 chip
- Insertion of the B-Layer (2013)
  - Small radius : 3.3 cm
  - Increase tracking performance
  - The FE-I4 designed to respect
    - Higher hit occupancy per pixel
    - Higher level of radiations
- Phase 1 or Phase 2
  - New pixel detector planned
    - 2 removable internal layers at radii of about 3.3 – 10 cm
    - 2-3 fixed outer layers at radii of about 15 – 25 cm
  - FE-I4 fits requirements for outer layers in terms of hit occupancy and radiation hardness
  - A new development is required for the inner layers

ATLAS Pixel Detector

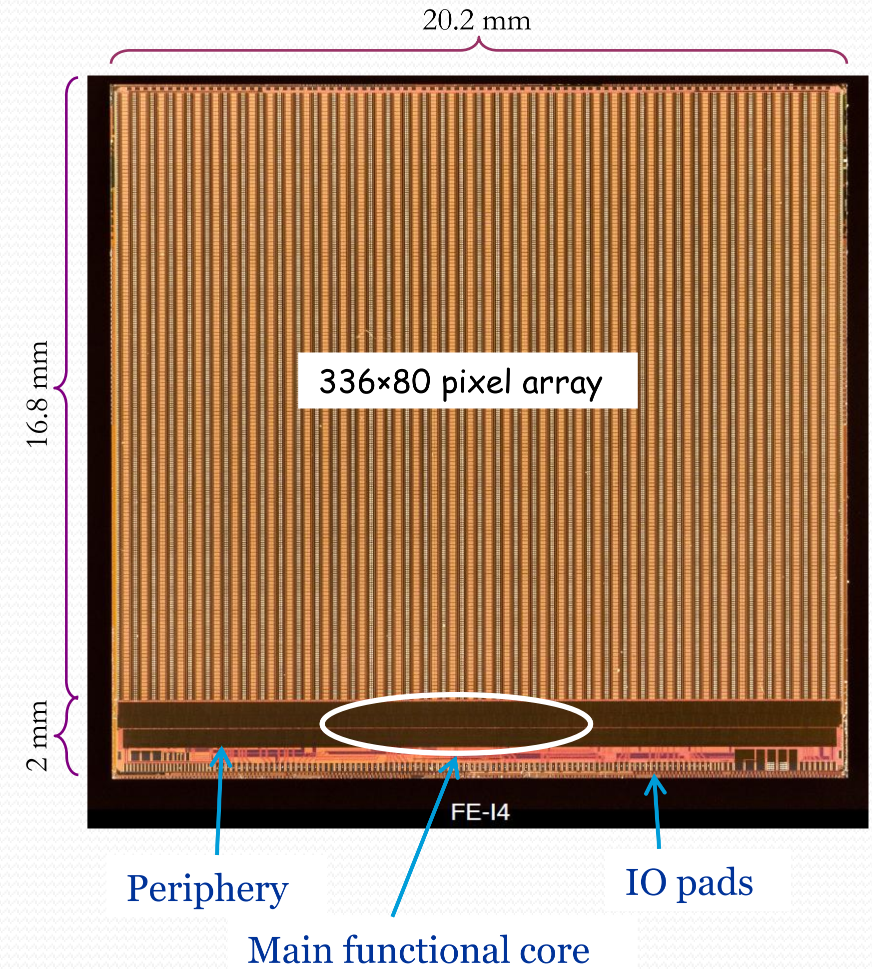


- 3 barrel layers / 3 end-caps
- end-cap: z± 49.5 / 58 / 65 cm
- barrel: r~ 5.0 / 8.8 / 12.2 cm



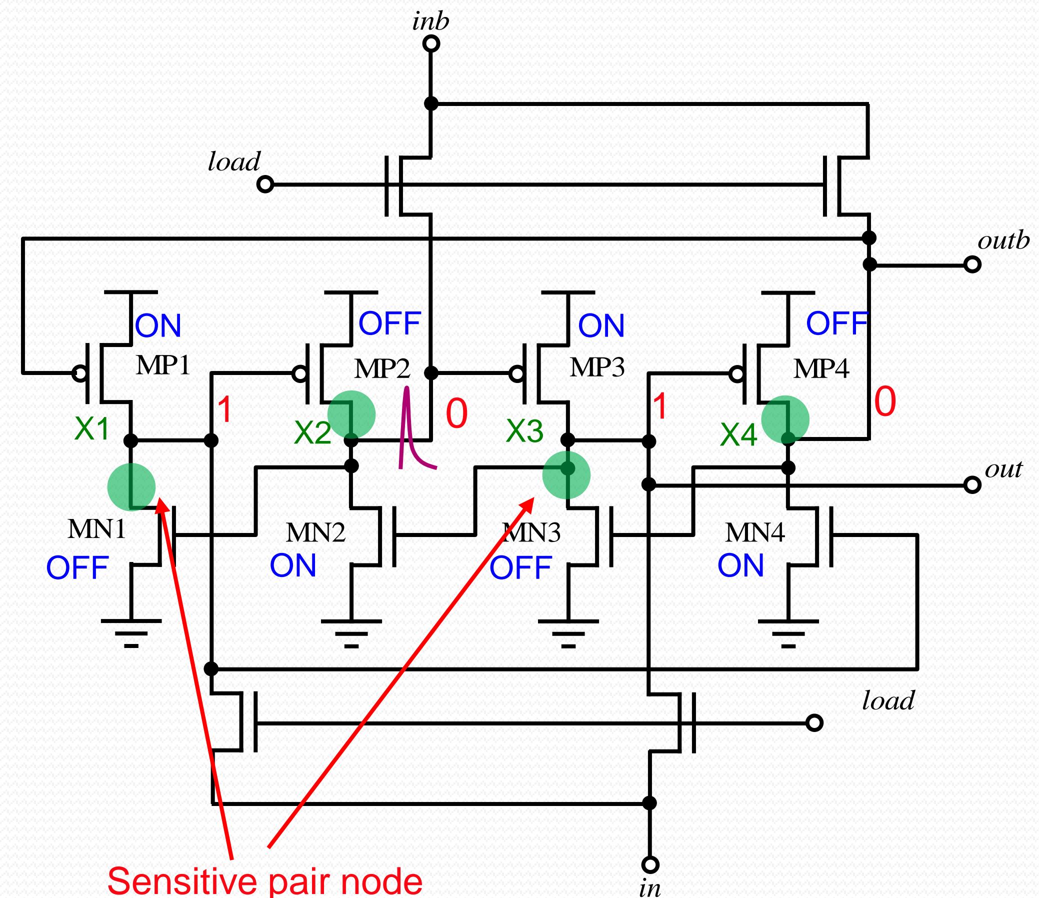
FE-I4 chip overview

- The FE-I4B chip is the production version for IBL installation
  - Designed in a 130 nm CMOS process
  - Dimensions : 20 mm x 19 mm
  - Active zone : ~ 90 % of the total area
  - Respects all the specifications
  - 96 wafers ordered in 2012
- The FE-I4 pixel array is organized in Double Columns (DC)
  - Double Column is divided into 2 × 2 pixel regions
  - 1 région : 2×2 pixel
  - Radiation tolerance > 200 Mrad
  - ~27 000 pixels where each pixel uses 13 bits for configuration

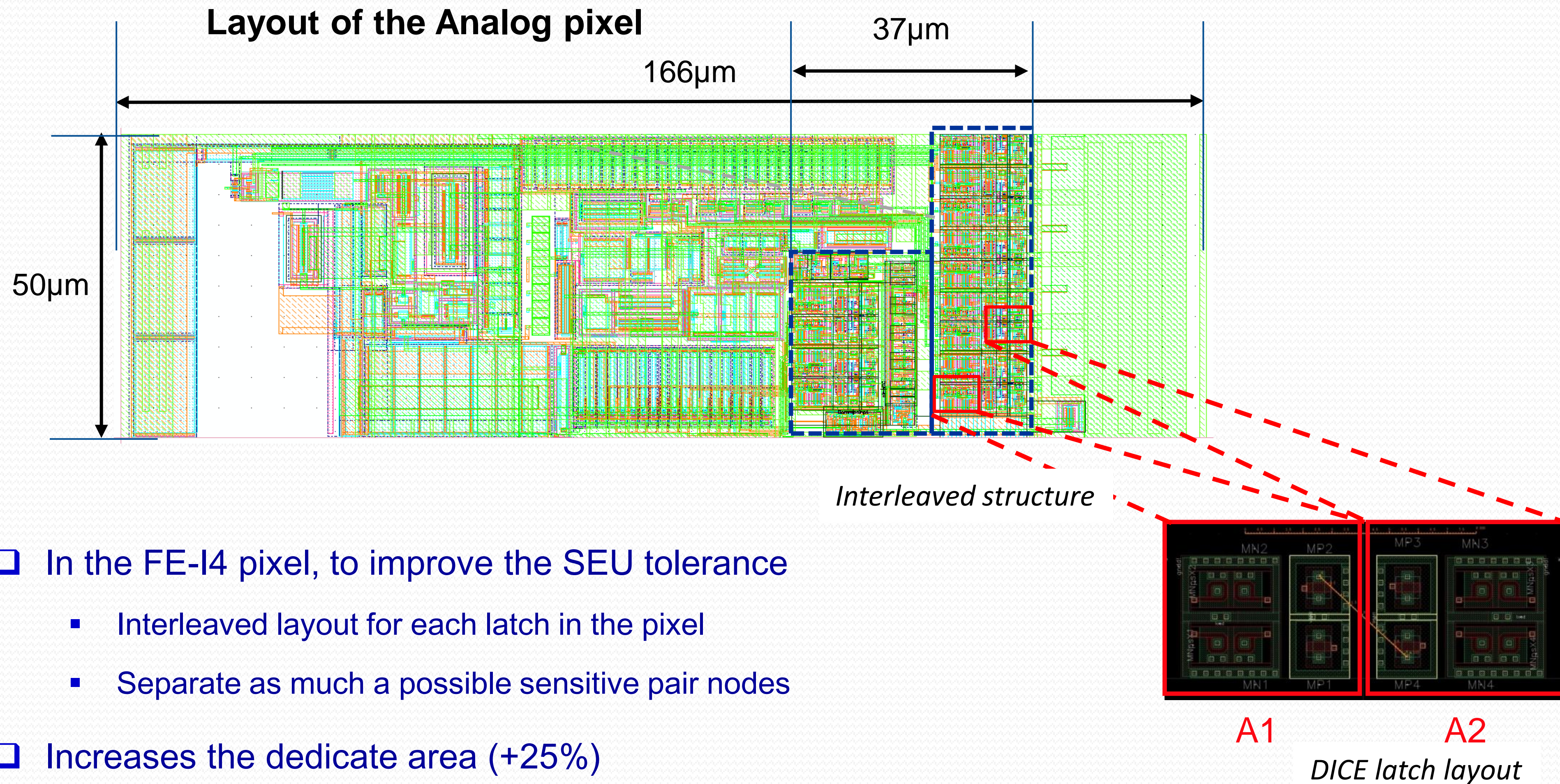


Dice Latch description

- Configuration logic in the FE-I4 is based on the DICE latch
- The DICE latch uses the conventional cross coupled inverter latch structure
- If we assume a positive upset pulse on X2
  - MP3 is turns OFF avoiding the propagation of this perturbation to the node X3 and X4
  - But, If the perturbation happens on the 2 sensitive nodes storing the same state, the immunity is lost and the Dice latch is upset.
- Spatial separation for the drain diffusions of MN1 and MN3
- Contacted guard ring and nwell separation for pmos MP1 and MP3 for isolation
- Enclosed layout to minimize the sensitive nodes area



Latches pixel implementation



- In the FE-I4 pixel, to improve the SEU tolerance
  - Interleaved layout for each latch in the pixel
  - Separate as much a possible sensitive pair nodes
- Increases the dedicate area (+25%)
- Complicates the interconnection between elementary cells

SEU Experimental Test Set up

Control room

Power Supply
VDDD-VDDA

USBPix software

~20 meters
length USB cable

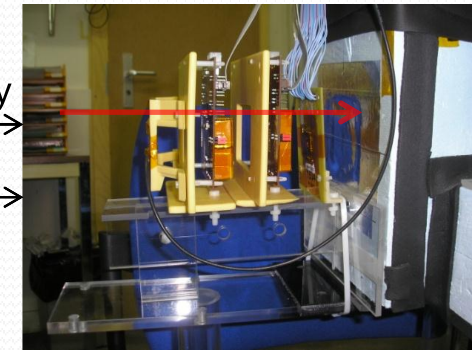
Irradiation zone

MultiIO board
- USB controller
- FPGA …

Power Supply

Data

~3 meters



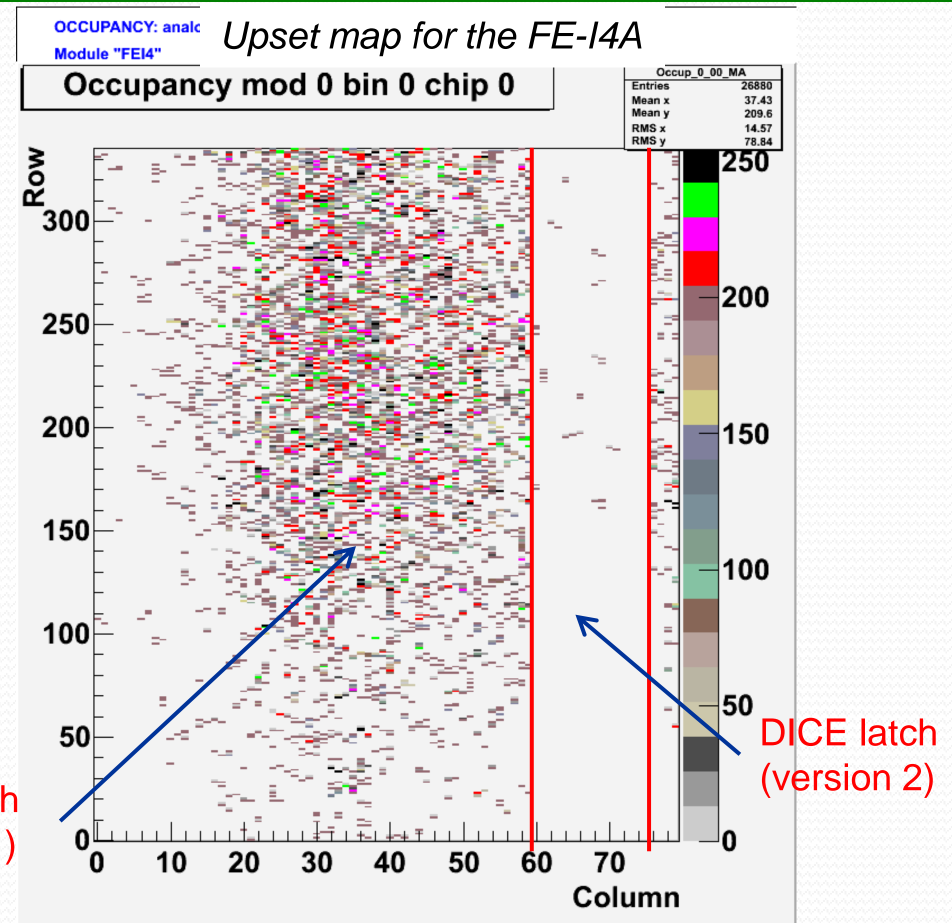
FEI4 chips as
target of the beam

Adapter card
-Regulators
-LVDS /TTL translators
--..

- Irradiation facilities : IRRAD3 beam line of the CERN Proton Synchrotron (PS)
- Beam of 24 GeV protons with a spot area around 1 cm²
- 1 to 4 spills per Cycle (CPS)
- The duration of each spill is 400 ms
- Typical fluency : 5E10 p/cm²/spill to 1.5E11p/cm²/spill
- Reach a fluency of 1 - 3 E13 p/cm2 per hour
- Data Acquisition synchronized with Spill signal or CPS

Analog Scan and cross section

- SEU Measurements were did on the FE-I4A chip where 2 versions of the DICE were implemented
- Conditions to obtain this map :
  - Enable bit is the only config bit concerned for the test
  - All pixels disabled (enable=0) before the spill
  - An upset from 0 to 1 of the enable bit will give the map corresponding to the response of the input injection charge (200 events per input)
- In this configuration, we can directly see:
  - Lower SEU rate in version 2 columns
- Pixel latches with optimized layout (Version 2) are 30 times more resistant to SEU than the version 1
- The version 2 of the pixel latch configuration was adopted in the whole FE-I4B chip

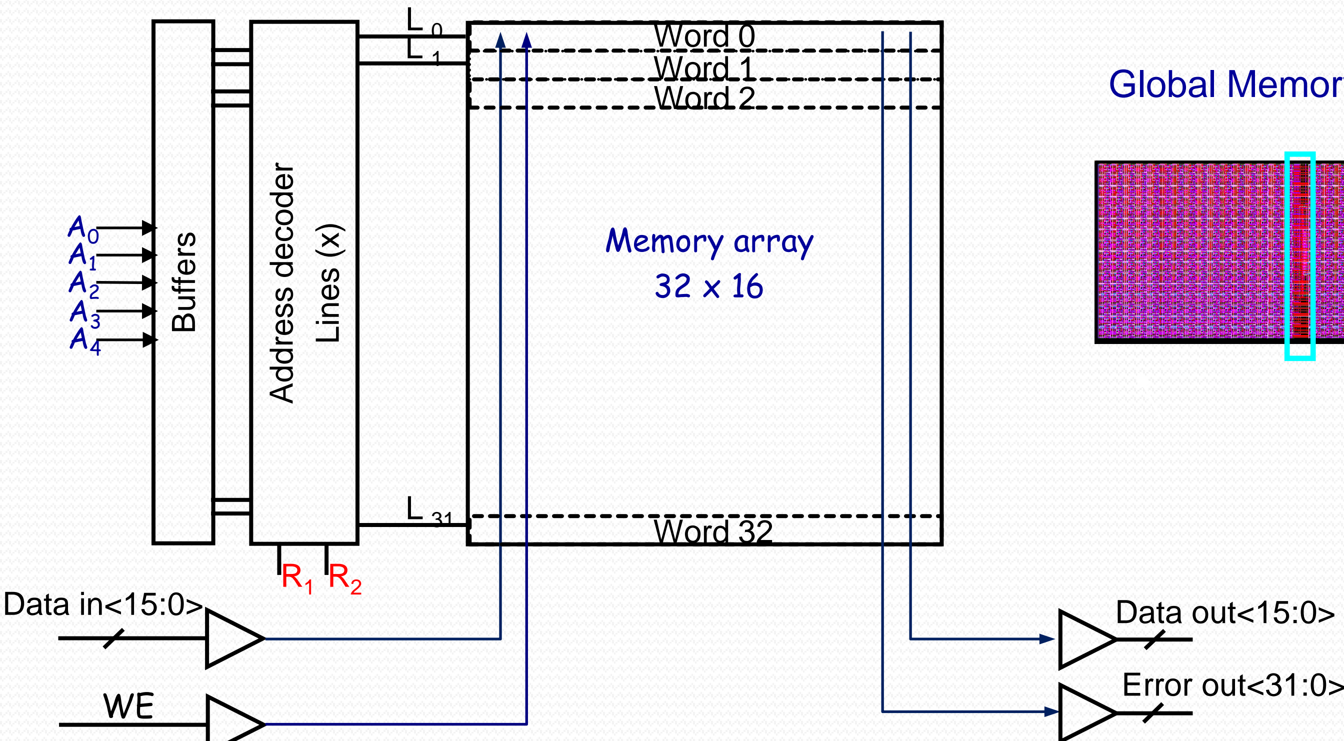


DICE latch (version 1)

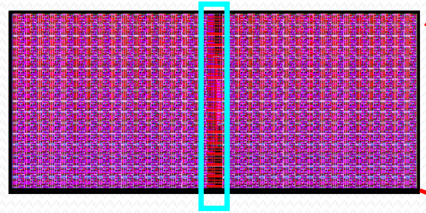
	Rate/spill	Cross-section
Version 1	3.0	31 10^{-15} cm^2
Version 2	0.1	1.1 10^{-15} cm^2

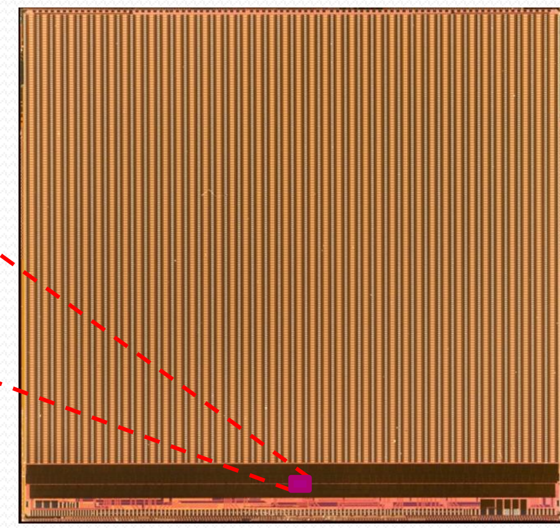
Centre de Physique des Particules de Marseille CPPM

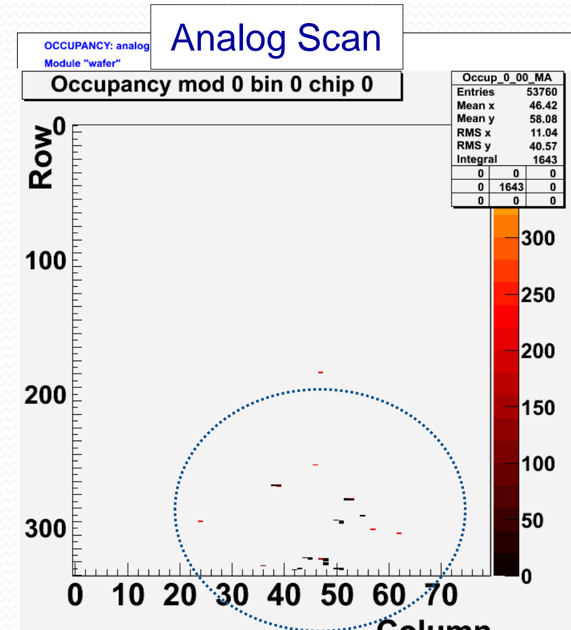
Global configuration memory



Global Memory Layout







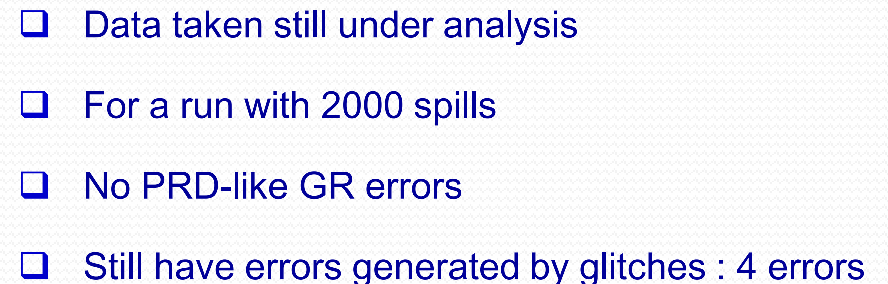
- Full custom 32 x 16 Memory array
- Layout : 900µm x 360µm
- Each cell memory is a Triple Redundant DICE Latch (TRL)
- Analog scan used to check that the beam centered on the End of Chip Logic
- R1 and R2 reset generated from the PRD bloc (Prompt Radiation Detector : Threshold =100 Mrad/s)

Classification of Errors

- During **FE-I4A** irradiation tests, the typical rate of errors is 6.8 % (102/1480 spills)
  - So higher than predicted
- Most of the errors are not related to the TRL SEU
- Error classification using Service Record Data (SR)
  - Normal GR SEU
  - PRD like resets where all GR bits are zero
  - Write glitch from Decoder
  - Internal glitch in the Global Memory
- PRD-like GR errors is the biggest effect on the FE-I4A

	TRL SEU	PRD Error	Wr glitch decoder	Internal glitch
Number of errors	2	79	11	10
Rate	0.1 %	5.3 %	0.7 %	0.7 %

- In the **FE-I4B** :
- The PRD threshold increased from 1001 to 1111
- A third detector added on the chip and separate the location of the 3 PRD detectors
- The load path triplicated inside the memory bloc to reduce the sensitivity to glitches



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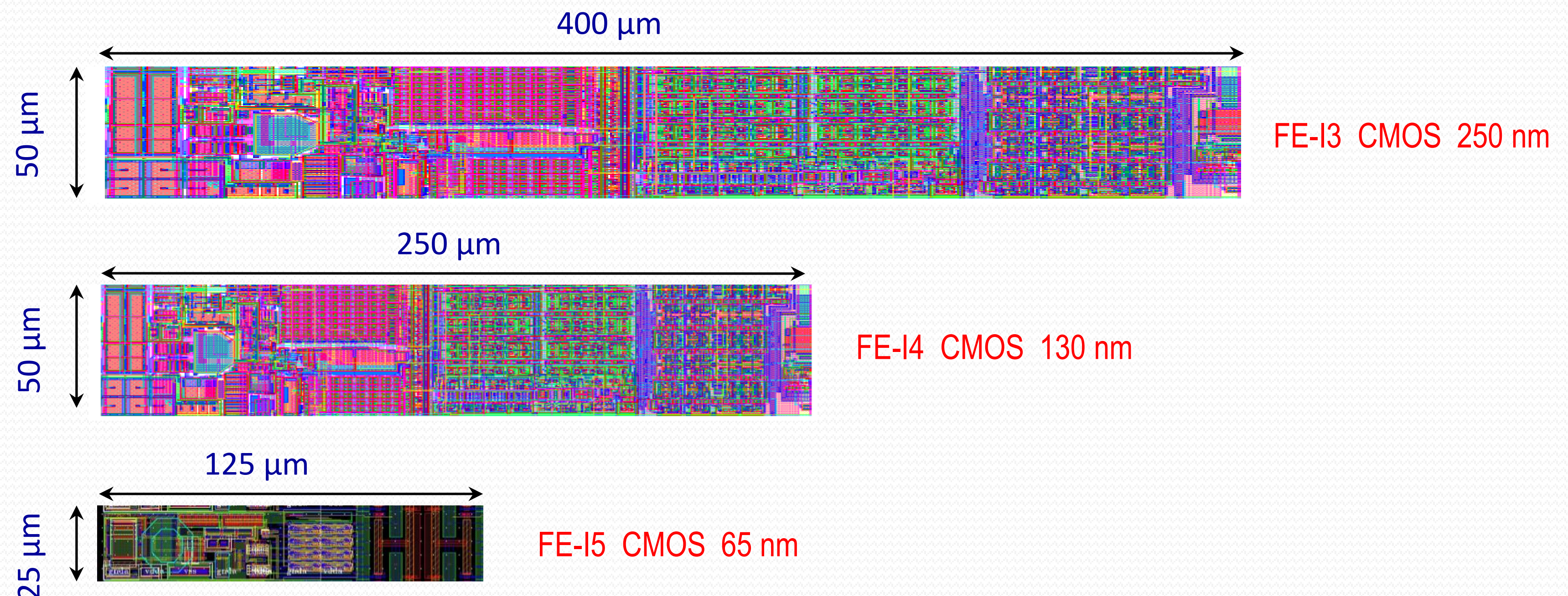
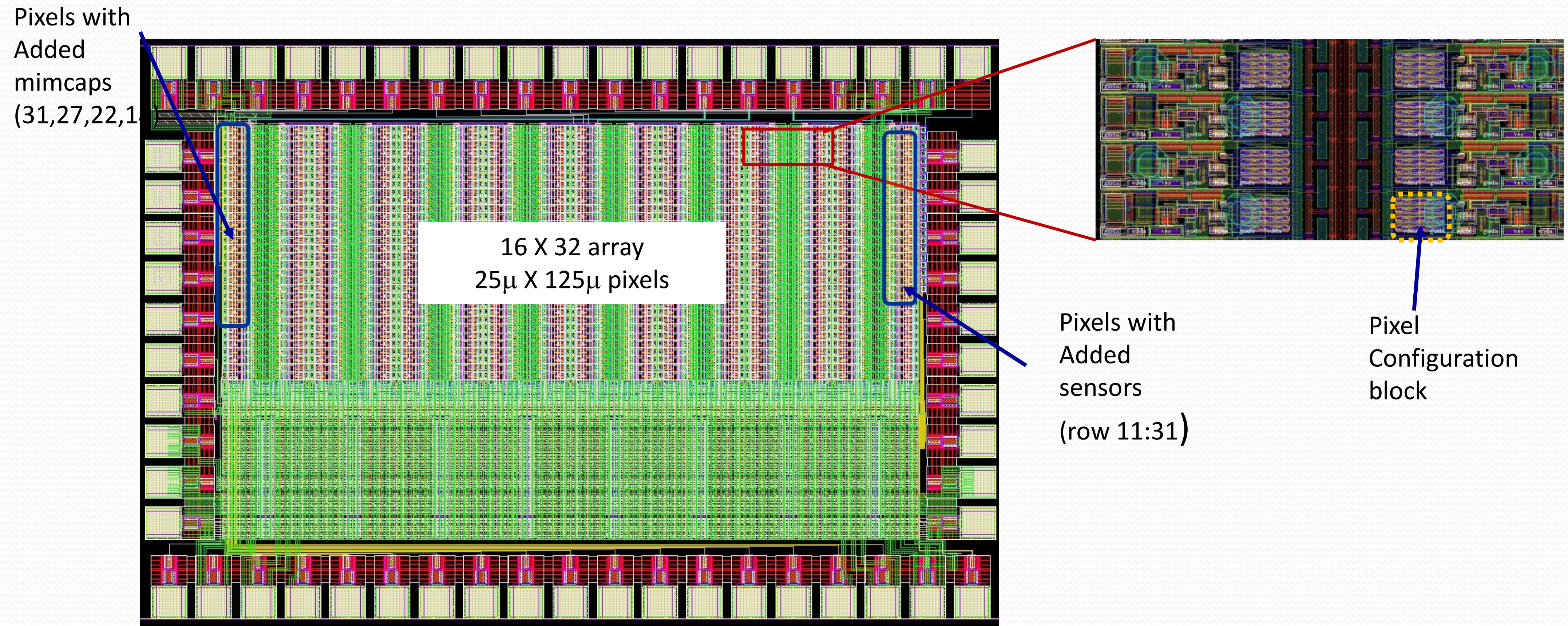
Motivations of using the 65 nm process

- For the HL-LHC, a new pixel detector is planned
  - 2 removable internal layers are planned (3.5 cm – 10 cm)
  - Reduction of the pixel size for the inner layers
  - The event rate is high and the FE-I4 architecture is not adapted (can not be processed by the FE-I4 chip)
- A new design is required : FE-I5
- R&D : CMOS 65 nm, 3D, Monolithic (HVCMOS, HRCMOS)
- CMOS 65 nm is considered as the base line solution
- A prototype has been designed to explore advanced CMOS processes and to evaluate radiation hardness and SEU tolerance



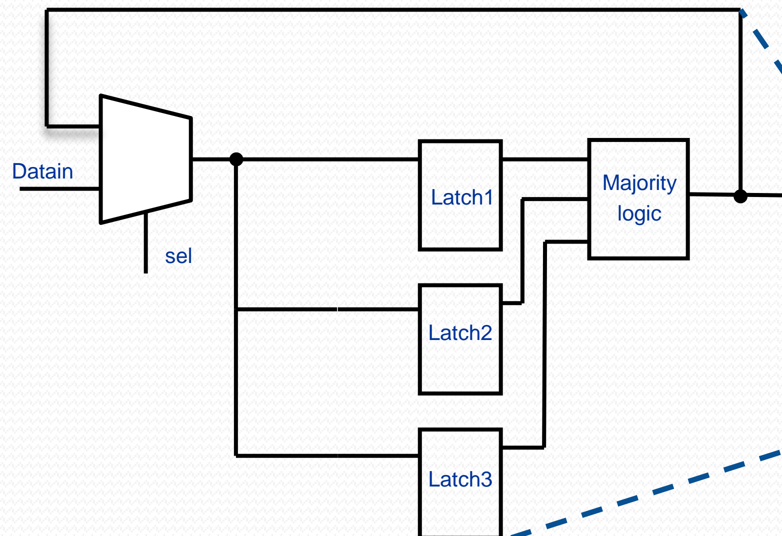
ATPIX65A: Atlas Pixel prototype array



- ATPIX65 : small array of pixels 16x32 designed at Berkeley using 65 nm CMOS process
- Pixel area : 25 μm x 125 μm
- Pixel y pitch is 25 μm and 50 μm bump y pitch
- Configuration : 8 Triple Redundant Latch (TRL) with error correction

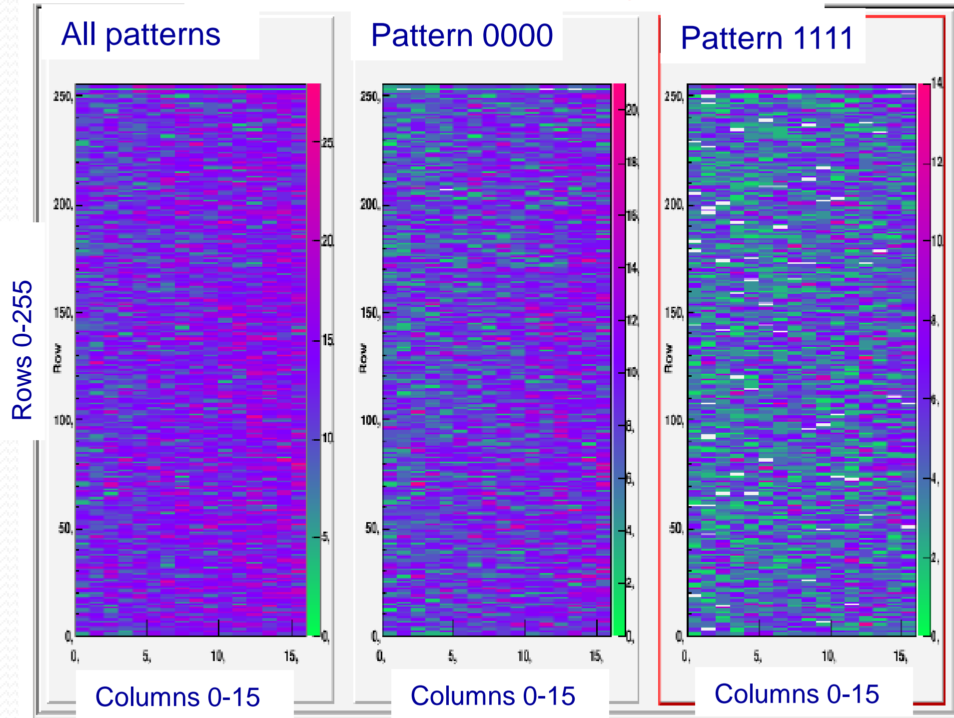
Configuration logic architecture

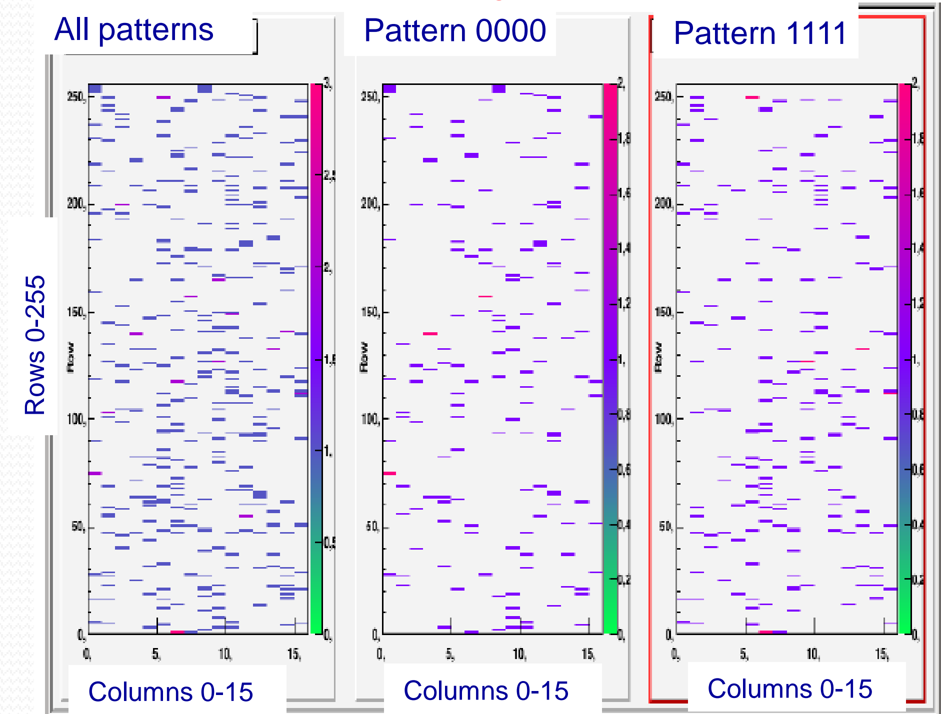
- Data loaded and readback with shift register (SR) .
- 16 columns of 256 Configuration TRL and 256 DFF
- One column is validated at the same time
- TRL with error correction
- Standard cells from ARM library



SROUT
ColAddress <3:0>
Multiplexer
SROUT_0
SROUT_1
SROUT_15
TRL 0 DFF 0
TRL 1 DFF 1
TRL 2 DFF 2
TRL 255 DFF 255
CK_0 CLR_0 LOAD_0 RDBK_0
CK_1 CLR_1 LOAD_1 RDBK_1
CK_15 CLR_15 LOAD_15 RDBK_15
SRIN_0
SRIN_1
SRIN_15
Demultiplexer
ColAddress <3:0>
SRIN, CK, CLR, LOAD, RDBACK

SEU test results





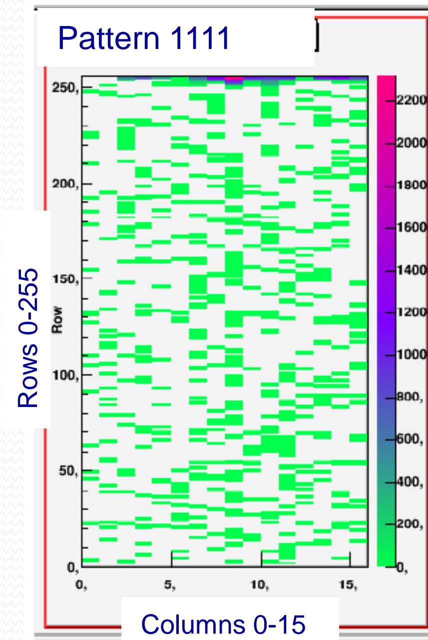
- SEU rate is computed for the DFF cell and for the TRL
- Cross section :
  - σ_{TRL} = 2.6 E-16 cm²
  - σ_{DFF} = 4.5 E-14 cm²
  - $\frac{\sigma_{DFF}}{\sigma_{TRL}} = 170$

	size	area	cross section σ (cm²/bit)		
			All	0 to 1	1 to 0
TRL for configuration	12.5µm × 4.3µm	54 µm²	2.6 E-16	2.64 E-16	2.55 E-16
DFF for Shift register	6µm × 2.4µm	14.4 µm²	4.5 E-14	5.9 E-14	3.0 E-14

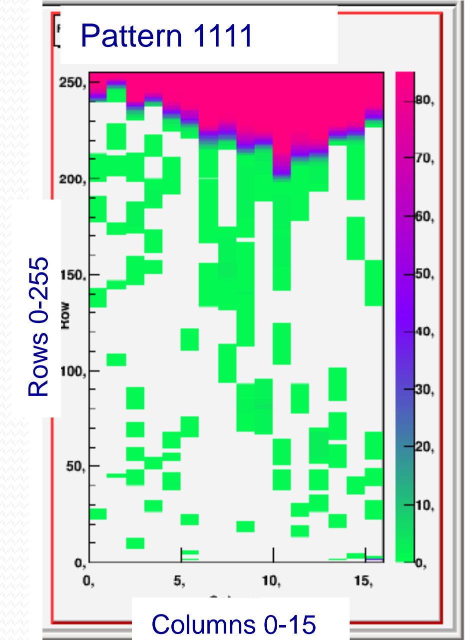
Dose effects

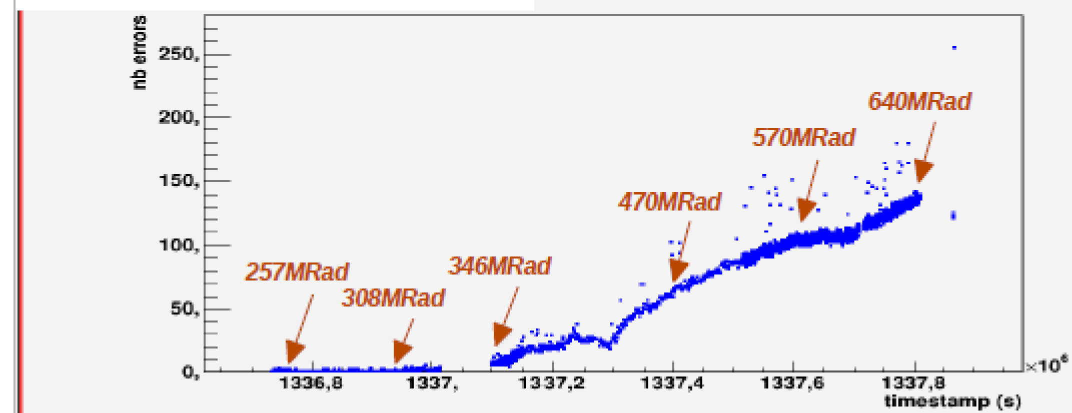
- From a dose level of 260 Mrad :
  - Systematic errors begin to appear for patterns "0000" or "1111"
  - The effect increases with the dose and cover the half of the DFF cells at 640 MRad
- The effect persists even outside the beam
- After Annealing, the number of systematic errors decreases
  - The chip seems to go back to a normal behavior after 420 hours of annealing
- But, still have a lot of errors with the pattern "1010"
- A new chip is currently being tested to check if the results are repetitive

260 Mrad to 310 Mrad



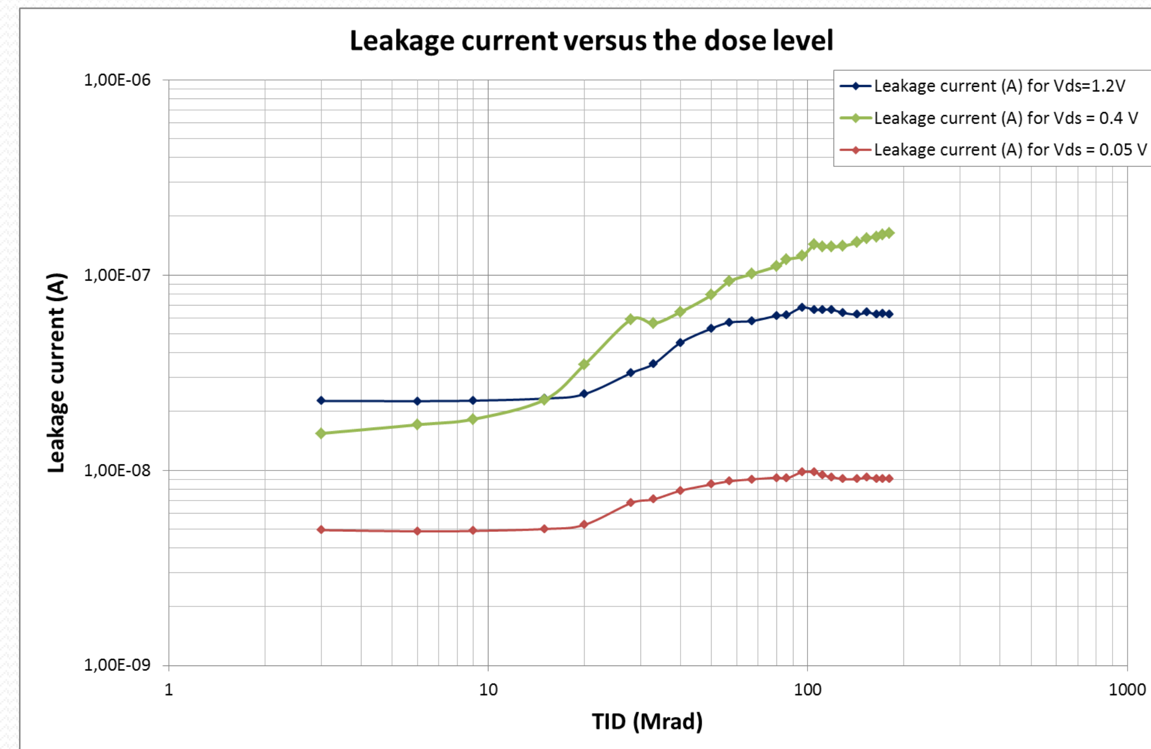
390 Mrad to 420 Mrad





Dose effects on the 65 nm device

- Measurement of proton radiation effects on a 65nm transistors
  - nMos low Vt transistor with W/L=22µm/100nm
  - We need to do this measurement on a minimum area device
  - Understand the effect for the dose level higher than 200 Mrad
- The sub-threshold slope does not change significantly at any transistor bias
- The leakage current increases by 1 order of magnitude for a total dose of 180 Mrad
- The leakage current seems to reach a saturation value for high dose levels
- Compatible with irradiation results of the Analog FE electronic
  - Los Alamos with 800 MeV protons
  - No damage observed to 600 Mrad
- Is the dose effect on the configuration memories related to a minimal size transistor used in digital cells from ARM library ?



summary

- The FE-I4B chip respects requirements in term of SEU for local and global configuration memories
- The FE-I4B chip is now used for the IBL production

- For the future pixel design : 65 nm process is considered as the base line solution
- A prototype chip with a small array of pixels have been designed and successfully tested
- In this chip, configuration memories are based on the triple redundancy
- Designed with cells from the TSMC-ARM library
- Very good results in term of cross section and tolerance to SEU
- For a high level of dose (250 Mrad), systematic errors are introduced
- Irradiation tests in progress to check for the repeatability
- A new design with different structures of configuration memories in now under development
- Do we need to design a custom digital standard cells library ?

FE-I4 Collaboration

❑ Participating institutes :

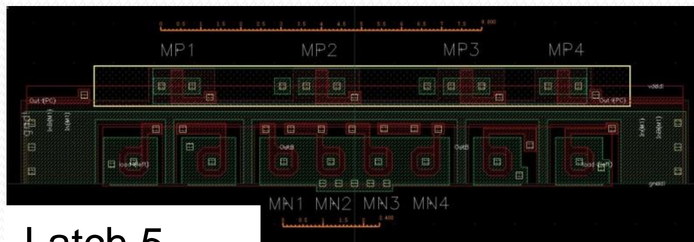
- *Bonn* : David Arutinov, Malte Backhaus, Marlon Barbero, Tomasz Hemperek, Laura Gonella, Michael Karagounis, Hans Krueger, Andre Kruth
- *Genova* : Roberto Beccherle, Giovanni Darbo
- *LBNL* : Lea Caminada, Sourabh Dube, Julien Fleury (LAL), Dario Gnani, Maurice Garcia-Sciveres, Frank Jensen, Yunpeng Lu (IHEP), Abderrezak Mekkaoui
- *CPPM* : Patrick Breugnon, Denis Fougeron, Fabrice Gensolen, Mohsine Menouni, Alexandre Rozanov
- *NiKHEF* : Vladimir Gromov, Ruud Kluit, Jan David Schipper, Vladimir Zivkovic

Error rate estimation for pixel configuration block

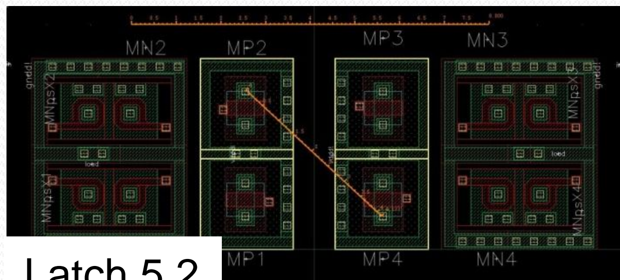
- The SEE fluency is calculated by summing the rates of charged particles (hadrons) and neutrons with kinetic energies > 20MeV.
- the estimated SEE rate based on simulations for the LHC, is 0.23 E15 particle/cm²/year for the pixel B-layer
- For the B-Layer upgrade, the luminosity is 3 times higher than at the start of the LHC. If we consider 1 year =1E7 sec and we apply a safety factor, the SEE rate is estimated to 3.0 E8 part/cm2.s

	Number of latches per FEI4 chip	Latch cross section (cm²/bit)	Mean time between 2 errors for one FEI chip (sec)
Pixel configuration	675840	3.0E-16	16 sec
Global registers	500	3.0E-16	22000 sec (6 hours)

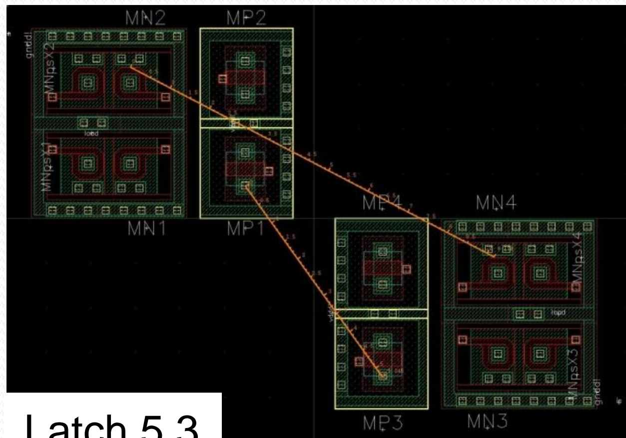
Layouts implemented in the chip SEU2



Latch 5

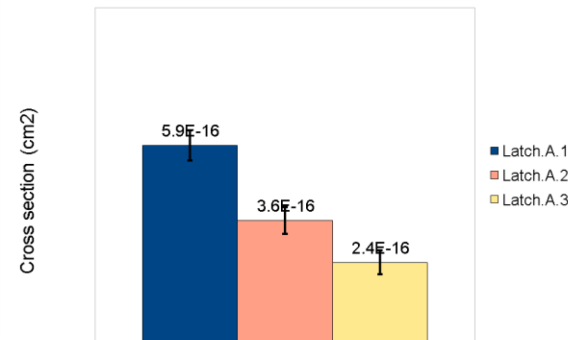


Latch 5.2



Latch 5.3

Latch type	area	Cross section cm²/bit		
		1->0	0->1	1->0 and 0->1 (*)
Latch 5	48 µm²	$(1.5 \pm 0.1).10^{-15}$	$(2.2 \pm 0.3).10^{-16}$	$(5.9 \pm 0.5).10^{-16}$
Latch 5.2	48 µm²	$(3.4 \pm 0.6).10^{-16}$	$(4.2 \pm 0.4).10^{-16}$	$(3.6 \pm 0.5).10^{-16}$
Latch 5.3	48 µm²	$(3.0 \pm 0.6).10^{-16}$	$(3.3 \pm 0.3)10^{-16}$	$(2.4 \pm 0.5).10^{-16}$



Measurements made in 2008 for the chip SEU2

- Different layout versions were implemented in the SEU2 chip
  - Same schematic but different layout
- The latch 5.3 is 2.5 times tolerant to SEU than the latch 5
- This result shows the importance of separating sensitive nodes