Contribution ID: **139** Type: **Oral**

SEU tolerant latches design for the ATLAS pixel readout chip

Friday 21 September 2012 11:30 (25 minutes)

The FE-I4 chip for the B-layer upgrade is designed in a 130 nm CMOS process. For this design, configuration memories are based on the DICE latches where layout considerations are followed to improve the tolerance to SEU.
Tests have shown that DICE latches where layout approaches are adopted are 30 times more tolerant to SEU than the standard DICE latches.
For the future pixel readout design, a prototype chip containing 512 pixels is implemented in a 65 nm CMOS process. SEU tolerant latches are implemented for the pixel configuration and the SEU tolerance is under test and evaluation.

Summary

FE-I4 integrated circuit is designed for and contains for 26 880 hybrid pixels arranged in 80 columns on 250 µm pitch by 336 rows on 50 µm pitch. It is designed in a 130 nm CMOS process.
Each pixel has 13 configuration latches based on the Dual Interlocked storage Cell (DICE) to improve tolerance to Single Event Upsets (SEU). However for such a process, the redundancy becomes less efficient because of the charge sharing between sensitive nodes in the DICE latch. This is why layout considerations are considered in this design, especially spatial separation of critical nodes, isolation techniques like isolated wells, guard rings and cell interleaving. Particular attention has been paid to the combinatorial logic controlling each bloc of the configuration latches. A relatively complex scheme is adopted to prevent the transient errors occurring in the control logic to be propagated to the latches.
SEU tests were carried out using IRRAD3 beam line of the Proton Synchrotron (PS) facility at CERN where a beam of 24 GeV protons is provided. Tests have shown that optimized latches are 30 times more tolerant than latches designed without layout precautions.
On the other hand, the effect of SEU in the 65nm CMOS process is explored and studied. In fact the 65 nm process is considered now as the best candidate for the future readout chip design which is expected for the LHC high luminosity upgrade. A pixel size of 150 µm by 25 µm can be reached and this represents only 30% of the 130 nm FE-I4 pixel area. A chip prototype containing 512 pixels has been designed and tested. In this design, the pixel configuration memories are based on the triple redundancy of a standard latches with an additional logic for error correction.
Tests are currently being conducted. Initial results show that the triple redundancy reduces hugely the number of errors. Details of these measurements will be presented and discussed.

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Session Classification: Topical