Contribution ID: **24** Type: **Oral**

A Digitization Scheme of Sub-microampere Current Using a Commercial Comparator with Hysteresis and FPGA-based Wave Union TDC

Tuesday, 18 September 2012 14:50 (25 minutes)

A digitization scheme of sub-microampere current using a commercial comparator with adjustable hysteresis and FPGA-based Wave Union TDC has been tested. The comparator plus a few passive components forms a current controlled oscillator and the input current is sent into the hysteresis control pin. The input current is converted into the transition times of the oscillations, which are digitized with a Wave Union TDC in FPGA and the variation of the transition times reflects the variation of the input current. Preliminary tests show that input charges <25fC can be measured at >50M samples/s without a preamplifier.

Summary

Digitizers interfacing directly to current sources are particularly useful in high energy physics. In our scheme, a current controlled oscillator is built using a comparator (Analog Device Inc. ADCMP605) and its oscillation frequency is determined by the input current into its hysteresis pin. The LVDS output of the comparator is sent to an FPGA and the oscillation pulse widths are digitized with the Wave Union TDC inside the FPGA. There is no preamplifier in our test.

The Wave Union TDC is a scheme developed in our previous work to improve resolution of TDC implemented in FPGA beyond its cell delay. Multiple 0-1 and 1-0 transitions are generated in the delay chain in the Wave Union TDC and registered for encoding, which effectively provides multiple measurements with one set of delay chain and register array structure and thus improves time measurement resolution. (Regular TDCs make one measurement with a single 0-1 transition.) A time measurement resolution better than 30 ps (rms) can be achieved in low cost FPGA devices carrying multiple channels, which exceeds requirement for this application.

In this scheme, the noise affecting the analog input is minimized since there is only one logic transition for each sampling point when the analog signal is converted to logic level. This is an advantage of comparator-based ADC schemes over the other ADC schemes.

In one of our tests, the oscillation pulse width is tuned to 18.8 ns, which provides a nominal sampling rate of 53 M samples/s with a current-to-time conversion ratio 5.9 ns/uA. The measured timing jitter of the pulse width is 281 ps (rms) corresponding to a current measurement resolution of 47 nA (rms). At 53 M samples/s, the product of 3-sigma current x sampling period is 2.7 fC. To test fast timing response of the digitizing scheme, we have digitized a charge movement of +-25 fC in a single-cycle sine shape with peak current +-200 nA and base width 200 ns (approximately 10 sampling points) for each half cycle. The result shows that the charge profile is clearly distinguishable from baseline noise. The oscilloscope traces and digitized data plots will be shown in the full paper. The power consumption for the comparator is ˜37 mW operating at 2.5 V and for the FPGA Wave Union TDC is ˜27 mW/channel.

It is useful to review the intrinsic advantage behind this scheme. We subconsciously apply deep negative feedback when we design analog circuits. However, the benefits of negative feedback such as better gain stability, linearity and bandwidth are secondary in digitization tasks since all waveform distortions can be calibrated in digital domain. The primary goal of processing weak signals is to amplify them before they are contaminated by the noise. Using a comparator, the difference of the input signals is fully amplified with its open loop gain. So a design strategy deviating from negative feedback is the primary reason of this achievement.

Primary author: Dr WU, Jinyuan (Fermilab)

Presenter: Dr WU, Jinyuan (Fermilab)

Session Classification: B2