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The NA62 Large Angle Veto front end electronic board

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The NA62 experiment will measure the BR(K+->π+νν) to within about 10%.
To reject the dominant background from photons, the large-angle vetoes (LAVs) must detect particles with < 1 ns time resolution and 10% energy resolution over a very large energy range.
A low threshold, large dynamic range, Time-over-threshold based solution has been developed for the LAV front end electronics. Our custom 32 channel 9U board uses a pair of low threshold discriminators for each channel to produce LVDS logic signals. The achieved time resolution obtained in laboratory, coupled to an HPTDC based readout board, is ˜150 ps.

Summary

The BR(K+->π+νν) provides a very sensitive probe of the flavor sector of the Standard Model. NA62 experiment at the CERN SPS, has the goal of detecting ˜100 decays with a S/B ratio of 10:1. The experiment must be able to reject background from K+−>π+π0 decays at the level of 10ˆ12. Kinematic cuts provide a factor of 10ˆ4 and ensure 40 GeV of electromagnetic energy in the photon vetoes; this energy must then be detected with an inefficiency of ˜10ˆ-8. For the large-angle photon vetoes, the maximum tolerable detection inefficiency for photons with energies as low as 200 MeV is 10ˆ-4. The system has to operate with signals of few millivolts, to detect low energy photons, and exceeding 10 V for 20 GeV photon showers and is expected to provide a time measurement with ˜1 ns resolution and an energy measurement with a moderate precision (of order 10\%). The LAV front end board is implemented on a 9U VME layout with the J1 power connector only at the top of the backplane. No VME bus line is connected to the board, only customs ±7V power lines are used. The 32 analog inputs are connected to the board using two DB37 connectors. Each input produces two outputs due to the presence of two programmable discriminators on each channel. The resulting 64 LVDS digital outputs are connected to a TDC using two SCSI2 connectors placed on the front panel . The analog sums of 4 and 16 channels are provided on 10 LEMO00 connectors for monitoring of the analog signal. The communication and the threshold setting are managed by the onboard CPU. To simplify maintenance and reduce costs, the board has a modular structure. The motherboard manages input, output and power distribution while the rest of the functionalities are implemented on 4 types of mezzanine: board controller, test pulse generator, time over threshold (ToT), and sum of four mezzanines. The ToT mezzanine manipulates the analog signal to produce the LVDS output. Inside the mezzanine the input signal is divided into two copies, by a passive resistive splitter. One copy is sent to the sum mezzanine while the other to the ToT chain. A clamping circuit able to sustain high rate of signal up to 10 V was designed to avoid channel saturation. A low noise, high bandwidth (800MHz), Current Feedback Amplifier (AD8001) is used to amplify the signal which is connected at high impedence to two comparators with LVDS drivers LMH7220. The threshold on each of this devices can be adjusted in the range 5-250 mV.
A first production of the FEE boards is currently being tested in Frascati. A fully automatized procedure allows to measure, using an Agilent test pulse generator, the time resolution, the effective threshold on each of the 64 channels of the board. A value of the time resolution of ˜150 ps has been measured and an efficiency of 95% for signal as low as 7mV on all channels is achieved.

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