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Implementation and Tests of FPGA-embedded PowerPC in the control system of the ATLAS IBL ROD card

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The Insertable B-layer is planned for the upgrade of the ATLAS at LHC. A silicon layer will be inserted into the existing Pixel Detector together with new electronics. The readout off-detector system is implemented with a Back-Of-Crate module implementing I/O functionality and a Readout-Driver card (ROD) for data processing. The ROD hosts the electronics devoted to control operations implemented both with a back-compatible solution (via DSP) and with a PowerPC embedded into an FPGA. In this document major firmware and software achievements concerning the PowerPC implementation, tested on ROD prototypes, will be reported.

Summary

The ATLAS experiment at LHC plans to upgrade the existing Pixel Detector with an innermost silicon layer, called Insertable B-layer (IBL). A new front-end ASIC (named FE-I4) has been designed as well as improved off-detector electronics, having increased read-out performances, but also being compatible with the existing system.

In particular, the Read-Out Driver module (ROD) is a VME-based board designed to process a four-fold data bandwidth with respect to the current card. Moreover, the ROD hosts the electronics devoted to control operations whose main tasks are: providing setup busses to access configuration registers on several FPGAs, receiving configuration data from external PC, managing triggers and running calibration procedures. In parallel with a back-compatible solution with a DSP, a new ROD control circuitry with a PowerPC embedded into a Xilinx FPGA has been implemented.

Experience on using the PowerPC has been gained during last year with tests on prototypes of the ROD card. In particular, efficient implementation of several peripherals has been realized, by means of Xilinx IP cores (to manage standard interfaces like Ethernet, Flash and DDR2 memories) as well as custom ones. The latters are firstly developed and simulated in a stand-alone environment, in order to verify the compliance with PowerPC and then integrated and connected to the internal microprocessor bus. They are mainly designed as interfaces with specific hardware blocks: the VME bus, the internal ROD bus which connects all FPGAs hosted into the card and the front-end control path, devoted to the FE-I4 configuration and control.

Firmware issues on peripheral deployment, test and performance will be shown.

A further step is to appoint a proper operative system (OS) running on the PowerPC as well as custom software applications managing the control tasks. Xilinx provides tools to implement and test different strategies: minimal OS, minimal with enhanced capabilities (f.i. multi-threading), embedded Linux. They are currently under test as well as their relative booting implementation.

Software development and major results are presented both in terms of peripheral management, OS implementation and possible integration strategies.

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