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Performance of the AMBFTK board for the FastTracker Processor

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Modern experiments at hadron colliders search for extremely rare processes hidden in much larger background levels. As the experiment complexity and the accelerator backgrounds and luminosity increase we need increasingly complex and exclusive selections. The FastTracker (FTK) processor for the Atlas experiment offers extremely powerful, very compact and low power consumption processing units for the far future, which is essential for increased efficiency and purity in the Level 2 trigger selection through the intensive use of tracking.
We report on the test results of the first prototype of the AMBFTK board assembled with a few prototypes of the AMchip04.

Summary

The FastTracker (FTK) processor [1] provides massive computing power to minimize the online execution time of complex tracking algorithms. The time consuming pattern recognition problem, generally referred to as the "combinatorial challenge", is beat by the Associative Memory (AM) technology [2] exploiting parallelism to the maximum level: it compares the clusters found in the event ("hits") to pre-calculated "expectations" or "patterns"(pattern matching) at once looking for candidate tracks called "roads". This approach reduces to linear the typical exponential complexity of the CPU based algorithms. The problem is solved by the time data are loaded into the AM devices.
The AMBFTK [3] is a 9U VME board that contains the Associative Memory chips (AMchip04 [4]). It is an essential part of the FTK core, whose computing power is such that a few hundred such boards will enable pattern recognition in ATLAS events to be carried out up to Phase II instantaneous luminosities (5×1034 cm-2 s-1) with an event input rate of 100 kHz and a latency of approximately a hundred microseconds. The AMBFTK has a modular structure consisting of 4 smaller boards, the Local Associative Memory Banks (LAMB) mezzanines. Each LAMB can contain 32 Associative Memory (AM) chips, 16 per side. The AMBFTK has to support a challenging traffic of data: a huge amount of "hits"must be distributed at high rate with very large fan-out to all patterns (10 Millions of patterns will be located on 128 chips placed on a single board) and a huge amount of roads must be collected and sent back to the FTK post-pattern-recognition functions.
We report on the test results of the first AMBFTK prototype assembled with few prototypes of the AMchip04. It is an important test of the FTK feasibility. We report on the timing performance of the whole system and power consumption of the AMchi04.
Hits are downloaded through VME inside the AMBFTK input FIFOs. Hits are partially distributed by a network of high speed serial links on the AMBFTK to the LAMBs up to the few AMchip04s. The new LAMB prototype realization has represented a significant technological challenge due to the high density of chips populating both sides, and the use of advanced packages and high frequency serial links.
The AMchip04 design provides a big improvement of all AMchip parameters with respect to the existing AMchip03[5]. A full-custom cell has been the most important achievement. The new chip, with extremely high pattern density (8000 patterns in a area of 14 mmˆ2), also contains new functional elements [6] and will be faster by at least a factor of 2 than the previous version.

[1] IEEE Trans. Nucl. Sci. 59, 348. (2012).
[2] Nucl. Instr. and Meth., vol. A278, pp. 436-440, (1989).
[3] CHEP 2012, New York (USA) May 21-25, (2012).
[4] NSS/MIC, Conference Record, Page(s): 141 –146, (2011).
[5] IEEE Trans. Nucl. Sci. 53, 2428 (2006):
[6] Animma 2011, Ghent, Belgium, June 6th to 9th, (2011).

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