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# An FPGA based topological processor prototype for the ATLAS Level-1 trigger upgrade

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By 2014 the LHC will collide proton bunches at 14 TeV with an increased instantaneous luminosity up to 3×10ˆ34cm−2s−1. A reduction on the trigger rate can be achieved by applying topological cuts adopting a new FPGA based module in the L1 trigger: the Topological Processor (TP). This presentation focuses on the design of the first TP prototype and on the test results on algorithm implemented in the TP demonstrator in order to measure latency and FPGA logic utilization.

## Summary

Due to the gradual increase in the LHC instantaneous luminosity up to 3 × 1034cm−2s−1 in 2014, the calorimeter trigger needs to be upgraded to cope with the higher background rate in order to keep Level-1 trigger rates at current levels without pre-scaling trigger streams of physics interest.
The current L1-Calo trigger allows making selections on multiplicity of objects (numbers of jets at various thresholds and clusters) identified via sliding window algorithms and Missing Transverse Energy. To achieve additional background rate reduction at Level-1, the information on jet or muon flying direction can be used. The current L1- Calo scheme is not designed to handle such amount of information in the Real Time Data Path (RTDP). To explore this feature, a new element in the L1-chain is needed: the Topological Processor (TP). The TP will make it possible to use the geometrical information of objects (jets, electrons, muons etc.) in the L1 trigger.
Technically, the TP works as a data concentrator from the calorimeters and muon detectors and feeds such data into specific topological algorithms which provide an output to the Central Trigger Processor CTP, where the final decision on the acceptance of an event is taken. As a consequence, the TP requires optical connectivity (data concentrator), high bandwidth, and high processing power (algorithms coded into FPGAs). Some modules in the existent L1 trigger signal chain will have to be upgraded or replaced to make topological information available to the TP.
For the intended use as future module in the L1Calo trigger chain, high bandwidth and low processing latency on the Real-Time Data Path (RTDP) are crucial. The initial aggregate bandwidth required for electron, tau, jets and muon topological information is about 820 Gb/s. The main-board design is fully AdvancedTCA compliant and will host two FPGAs of Virtex7 family XC7V485T (later on XC7V690T) with up to 80 embedded multi-Gb transceivers.
The track length on the PCB from 14 o/e converter to the MGT is kept as short as possible and no on-board electrical duplication of real-time data is provided. Multi-Gb o/e converters of high density (mini POD) are adopted and mounted as close as possible to the FPGAs. The output to the CTP is located on the front panel, via 2 multi-Gb output links.
This presentation focuses on the design of the first TP prototype which follows the R&D carried out using technology and functional demonstrators. The latest results on algorithm implementation in the demonstrators and test on latency and FPGA logic utilization are illustrated.

**Primary author:** SIMIONI, Eduard (Johannes-Gutenberg-Universitaet Mainz (DE))

**Co-authors:** REISS, Andreas (Johannes-Gutenberg-Universitaet Mainz (DE)); Mr BAUSS, Bruno (Johannes-Gutenberg-Universitaet Mainz (DE)); Mr DEGELE, Reinhold (Johannes-Gutenberg-Universitaet Mainz (DE)); MORITZ, Sebastian Erich (Institut fuer Physik-Johannes-Gutenberg-Universitaet Mainz); Prof. TAPPROGGE, Stefan (Johannes-Gutenberg-Universitaet Mainz (DE)); Dr SCHAEFER, Ulrich (Johannes-Gutenberg-Universitaet Mainz (DE)); Prof. BUESCHER, Volker (Johannes-Gutenberg-Universitaet Mainz (DE)); WENZEL, Volker (Johannes-Gutenberg-Universitaet Mainz (DE)); JI, Weina (Johannes-Gutenberg-Universitaet Mainz (DE))

**Presenter:** WENZEL, Volker (Johannes-Gutenberg-Universitaet Mainz (DE))

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