A low-latency, low-overhead, quick resynchronization line code for the optical data links of the ATLAS liquid argon calorimeter upgrade

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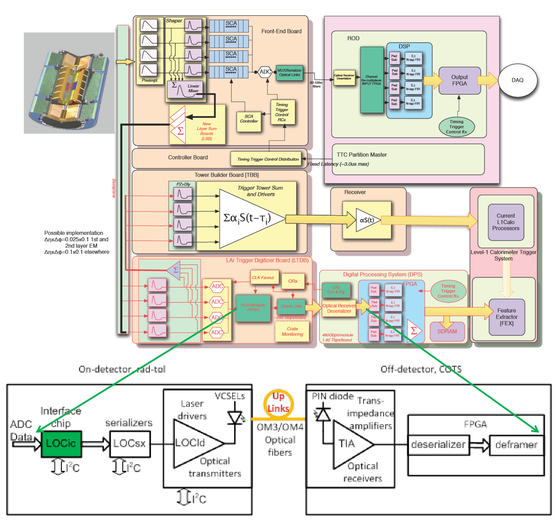
Abstract

We propose a line code for the optical data links of the ATLAS liquid argon calorimeter upgrade. The line code features low latency, low overhead, fast resynchronization capability and flexible frame size. Both the encoder and decoder have been verified in an FPGA and the performance has been evaluated. The encoder will be implemented into an ASIC.

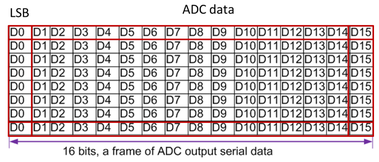
Introduction

- The readout electronics upgrade of the ATLAS liquid argon calorimeter has been proposed for the high luminosity LHC [1].
- In the proposed upgrade scheme, the readout electronics will transmit all digitized data out of the front-end through optical links to generate the Level-1 trigger signal.
- The optical links include the interface, serializers, optical transmitter modules (composed of laser drivers and laser diodes) on the front-end and optical receiver modules (composed of PIN diodes and trans-impedance amplifiers) and FPGAs on the back-end.
- A line code is needed in an optical link for clock recovery, DC balance and boundary identification.
- A receiver must be able to detect from the serial data which analog channel the data come from (i.e., the word boundary) and where a digitizing sample starts and ends (i.e., the frame boundary). The commonly used line codes (e.g., 8B/10B and 64B/66B) have no framing function. It is favorable to combine the low-level line code and the high-level framing to reduce the overhead.
- An optical data link operating in a harsh radiation environment may be disturbed by single-event effects. For example, in the irradiation test of a serializer ASIC we have observed a one-bit data shift following a burst of errors [2]. It is highly desirable that a line code have a fast resynchronization capability to minimize data loss.
- Due to the size limit of the analog buffers, the latency of the encoder and the decoder should be kept as low as possible.
- A bunch crossing identification (BCID) should be embedded in the data for event identification and the alignment of optical link channels.

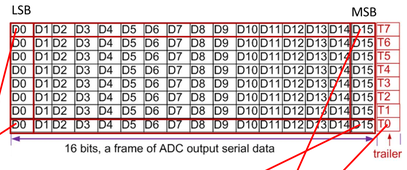


Frame Definition

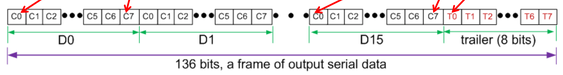
The input data format of the interface chip (LOCic)



The output data format of LOCic



The output format of the serializer



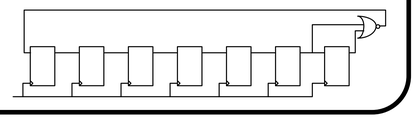
The frame trailer consists of 4-bit pseudo-random binary sequence (PRBS) and 4-bit cyclic redundant code (CRC) of the original data

- We choose 2^7-1 PRBS as the identification of frame ending. The period of the 2^7-1 PRBS is 127. The underlined bits shown in the right figure are the start of the sequence.
- We put 4 bits out of each 16 bits of the PRBS sequence in the trailer of each frame (green bits shown in the figure).
- The PRBS codes in consecutive frame trailers are used together to identify frame ends.
- The PRBS codes can be considered as an encoded counter and can be used as a BCID. The period of the counter shown in the figure is 2032 (= 127 x 16).
- We choose 4-bit CRC $x^4 + x + 1$ as the error detection code.

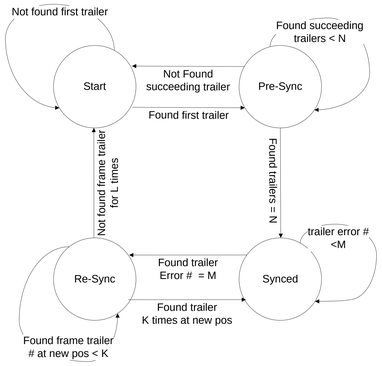
An original 2^7-1 PRBS starting with underline bits and the green code used in the trailers

1111111000000100
0001100001010001
1110010001011001
1101010011111010
0001110001001001
1011010110111101
1000110100101110
1110011001010101
1111110000001000

A block diagram of a PRBS generator



Frame Synchronization

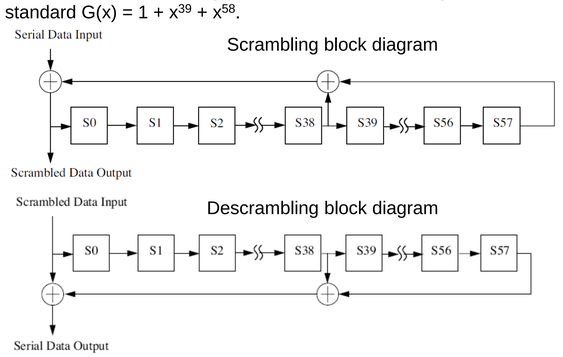


The state machine of frame synchronization process

- The receiver starts at the check state.
- After N correct consecutive 4-bit PRBS codes, the receiver goes into sync-ed state.
- After M trailer errors, the receiver goes into re-sync state.
- After K correct trailers, the receiver goes back to sync-ed state. Otherwise, receiver goes back the original check state.
- M, N, K can be adjustable. If a data shift occurred in a serializer, the receiver can recover the synchronization in K frames (minimum = 1).

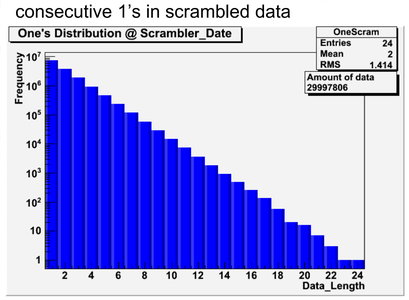
Scrambling and Descrambling

- We choose the scrambling scheme used in the 10 Gbps Ethernet standard $G(x) = 1 + x^{39} + x^{58}$.



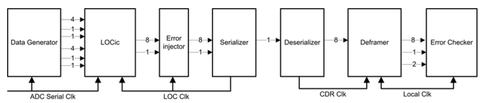
- We have simulated the effects of scrambling with unbalanced input data and found that probability of the running length (n) of 1's (or 0's) in the scrambled data is about $2^{-(n+1)}$. For example, the probability of 64 consecutive 1's is about $3x10^{-20}$.

The frequency versus the running length of consecutive 1's in scrambled data



Verification & Implementation

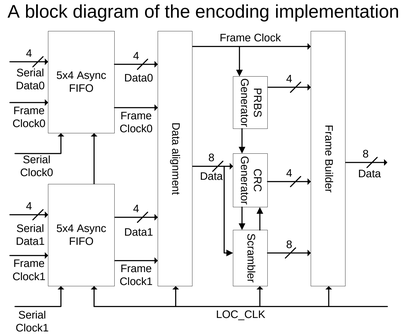
- The proposed encoding/decoding scheme has been verified in an Altera Stratix II GT FPGA.
- A data generator is used to simulate ADCs in a real application.
- The error injector is used to simulate single bit flips and data shifts observed in the serializer irradiation test.



A block diagram of the FPGA implementation

- The input data are synchronized to an internal clock using asynchronous FIFOs.
- The data from two 4-channel ADC chips are aligned each other.
- The original data are scrambled before a PRBS and CRC are inserted to the end of each frame.

A block diagram of the encoding implementation



- The decoder will be integrated in an ASIC together with the serializer in a 0.25 μm commercial silicon-on-sapphire (SOS) process. The ASIC design has been started.

Summary

- We propose a line code featuring low latency, low overhead, fast resynchronization capability and flexible frame size for the optical data links of the ATLAS liquid argon calorimeter upgrade.
- Both the encoder and decoder have been verified in an FPGA and the performance has been evaluated. The encoder will be integrated in an ASIC.

Comparison of proposed code and common used codes (assuming 8-bit parallel input data at 640 Mbps)

	8B/10B	64B/66B	Proposed
Overhead	25%+framing	3.125%+framing	6.25%
Framing included	No	No	Yes
BCID included	No	No	Yes
Latency of encoder (clock cycle)	2.5	2 (+gearbox)	2
Decoder latency (clock cycle)	4.5	4 (+gearbox)	4
Serial bit # needed to re-sync	30	4224 (min)	136

References

1. Hucheng Chen, Readout Electronics for the ATLAS LAr Calorimeter at HL-LHC, the Technology and Instrumentation in Particle Physics (TIPP) conference, Chicago, U.S.A, June 9-14, 2011.
2. Datao Gong, A 16:1 Serializer ASIC for Data Transmission at 5 Gbps, 2010 JINST 5 C12009.