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Results of 65nm pixel readout chip demonstrator array

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we have explored the use of the 65 nm CMOS technology node for pixel readout. A demonstrator 500-pixel matrix containing analog front ends only (no complex functionality), was designed and fabricated in Summer 2011, and irradiated with protons in Dec. 2011 and May 2012. We present the design and measurement results for this prototype.

Summary

We have explored the use of the 65 nm CMOS technology node for pixel readout. A demonstrator 500-pixel matrix containing analog front ends only (no complex functionality), was designed and fabricated in Summer 2011. The achieved dimensions translate to a pixel size of 25 microns by 150 microns, assuming a slightly greater amount of digital circuitry per pixel than in the FE-I4 chip in production for the ATLAS IBL upgrade. this new pixel is 30% of the 130nm FE-I4 pixel area, proving that the analog circuitry can be scaled down despite roughly equal specific gain of transistors in the 65nm and 130nm nodes. This prototype has been irradiated at the Los Alamos proton linac to a dose exceeding 600\,Mrad with no failures and very small change in performance (noise increase of 10%). Diode structures have been included in the array to be able to test pixels with actual signal from a radioactive source. Design considerations about the possibilities for extremely dense digital logic in this process will be discussed.

Primary author: Dr MEKKAOUI, Abderrezak (LBNL)

Co-authors: GNANI, Dario (LBNL); GARCIA-SCIVERES, Mauricio (Lawrence Berkeley National Lab. (US))

Presenter: MENOUNI, Mohsine (Centre National de la Recherche Scientifique (FR))

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