Testing and firmware development for the ATLAS IBL BOC prototype

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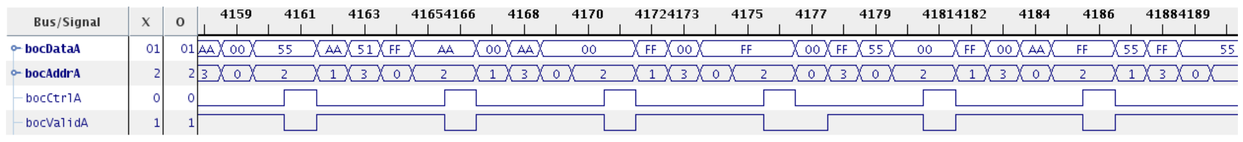
ATLAS Pixel Detector

The ATLAS Pixel Detector at LHC will be up-graded in 2013. This upgrade is called “Insertable b-Layer” (IBL) and will provide a new innermost detector layer with 448 front-end chips serving about 12 million pixel cells. To meet the communication requirements of the front-end chips (FE-I4) a new readout system will be developed. The Read Out Driver (ROD) and the Back of Crate card (BOC) are responsible for data acquisition and processing. These cards were completely redesigned and are equipped with state-of-the-art FPGA technology.

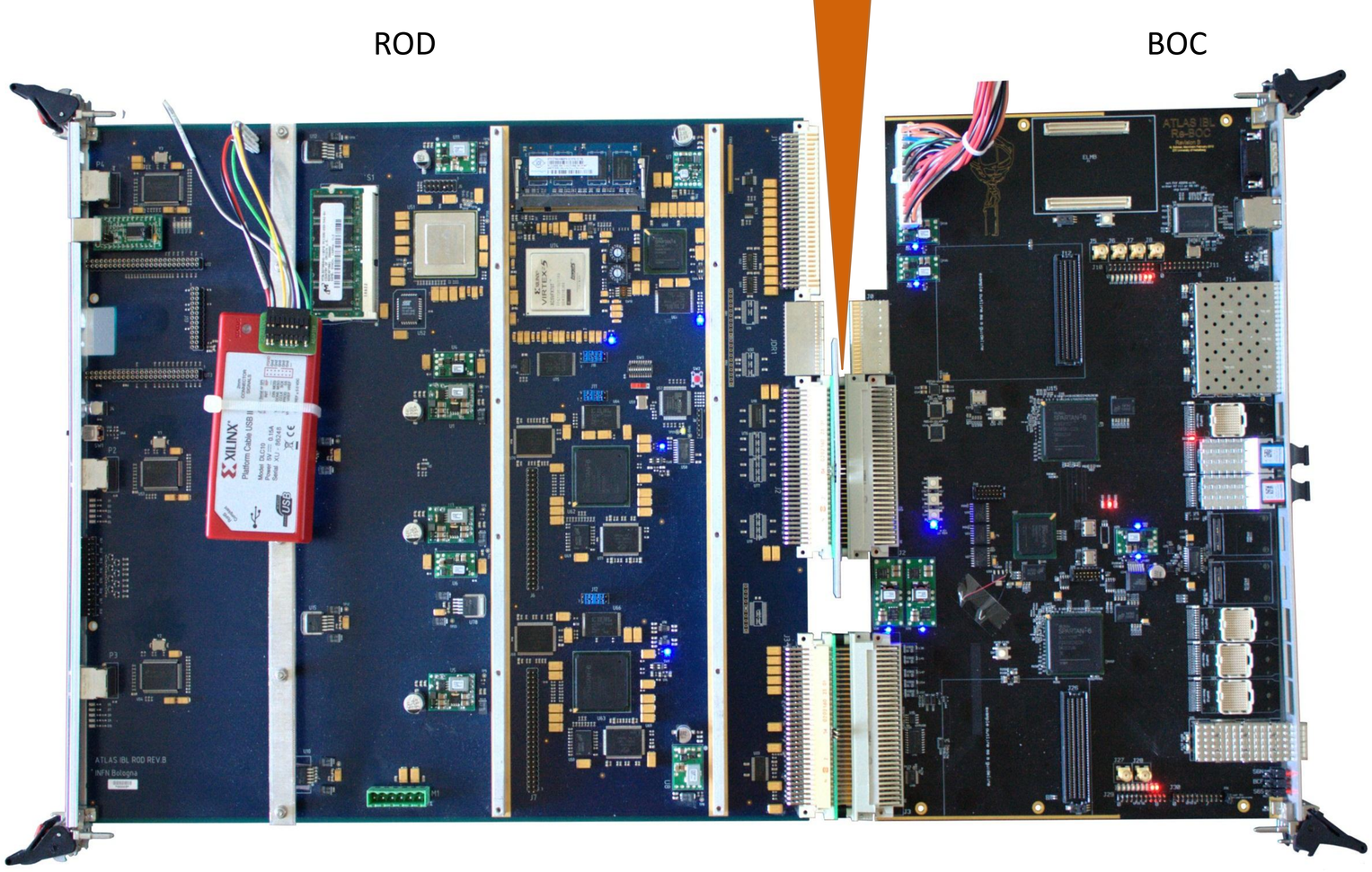
BOC-to-ROD interface

The BOC-to-ROD interface is designed as 8 parallel 8 bit wide bus with 2 address bits and 2 control bits. It is running at 80 MHz and transfers the data of 4 front-end modules. The maximum transfer rate of this interface is around 5 Gbit/s. The timing diagram on the right shows one of these 8 busses transmitting data to the ROD card.
It has been extensively tested with a bit error rate tester. Over 2 Terabyte of data has been exchanged between the two cards without any errors. This results in a bit error rate which is less than $5 \cdot 10^{-14}$.

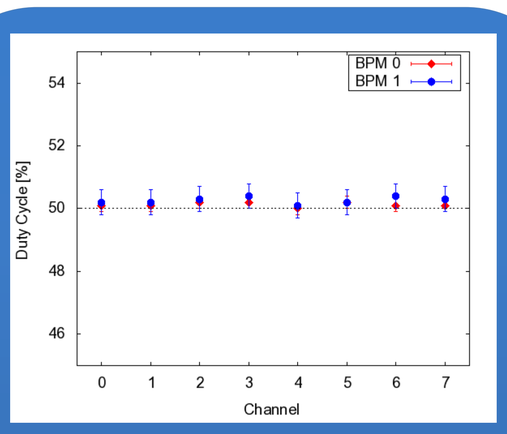


The IBL BOC card

The IBL BOC card is part of the newly developed readout system for the additional innermost pixel layer of the ATLAS detector. Three Xilinx Spartan-6 FPGAs are responsible for controlling the card and processing the data from and to the detector as well as to the higher-level readout system. Modern FPGA technology makes the BOC card very flexible for future tasks.
The BOC Control FPGA (BCF) is responsible for the control communication to the “outer”-world via the Setup-Bus and Ethernet. The two BOC Main FPGAs (BMF) serve 16 BPM-encoded TX (40 Mbit/s) and 32 8b10b- encoded RX (160 Mbit/s) links to and from the detector and the SLINK interface to the higher level readout system. The BOC card also distributes the global 40 MHz clock to the detector and to the ROD card.
The most important part of the firmware development was done in the signal processing part of the firmware. The TX part is responsible for the BPM coding of the serial configuration data stream from the ROD card to the front-end chip. For testing purpose the transmitter has the possibility to send data standalone without the ROD card as well as an 8b10b-transmitter for loopback tests. The deserialization of the incoming data from the front-end chip is part of the RX path. After the data recovery and the word alignment the data is decoded and sent to the ROD card. But the BOC card has monitoring modules that check for data and frame errors constantly. A snapshot of the incoming data can also be taken.

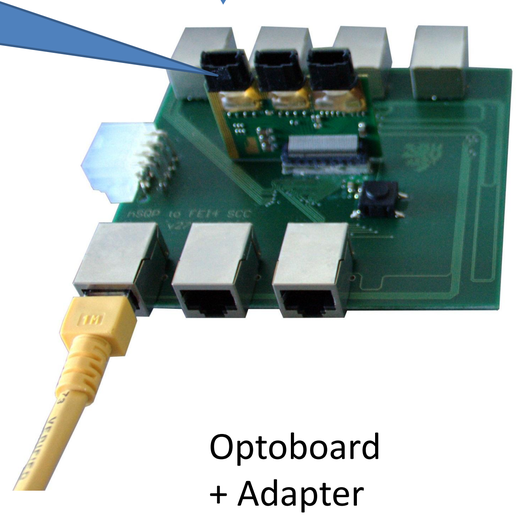


Optical link

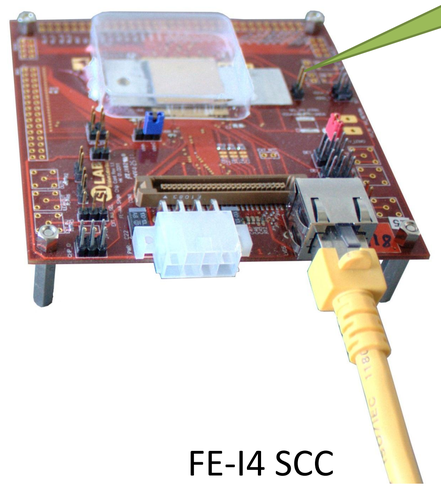


Detector interface

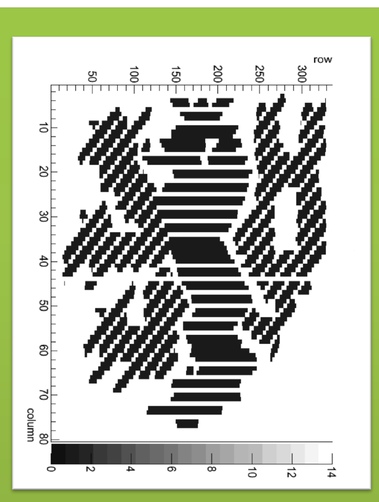
The detector interface has been tested extensively as it is the most complex part of the BOC card. All signals going to the detector need to be delayed to adjust the timing of the detector modules with respect to the bunch crossing. This is done by the BOC card. Also the Optoboard has certain requirements on the signal integrity. The most important part of the signal integrity on the optical link is the duty cycle of the signals from the BOC card to the Optoboard. To meet these requirements a duty cycle between 45 and 55 percent is needed. All 8 channels have been analyzed with an oscilloscope and have a duty-cycle of nearly 50%. So the signal integrity on the optical link from the BOC card to the Opto-board is fine.



Optoboard
+ Adapter

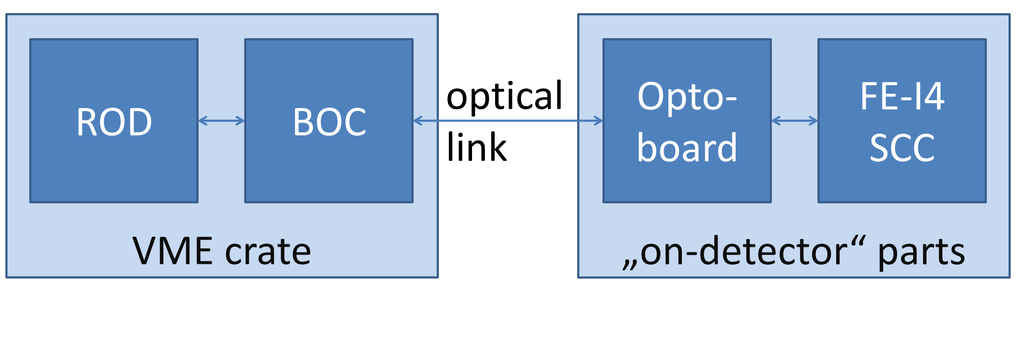


FE-I4 SCC



FE-I4 scan tests

To test the communication of the whole readout chain from the BOC card through the optical interface with the FE-I4 a Single Chip Card (SCC) was connected to the Optoboard in the same way as it will be used in the detector. Then a digital ToT scan was performed showing the logo of the University of Wuppertal.
This test is the most important test as it tests all functionality of the card and the firmware. It uses integrated debug functionality in the firmware, like memories for data transmission or reception and data monitoring. All functionality can be controlled by an integrated Microblaze processor which resides in the BCF.



Find more information here:
http://hepweb.physik.uni-wuppertal.de/index.php/detlab/optolink.html