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Testing and firmware development for the ATLAS IBL BOC prototype

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For the coming upgrade of the ATLAS pixel detector at CERN a redesign of the current data readout is necessary. To communicate with the additional 448 front-end chips assembled in the Insertable B-Layer (IBL) new FPGA readout cards consisting of a Back of Crate card (BOC) and a Read Out Driver (ROD) have been developed. This paper will describe the firmware and hardware development of the new BOC prototype. Firmware tests, like electrical and optical loopback and communication tests with the new IBL front-end modules and the ROD will also be presented in the paper.

Summary

The Large Hadron Collider (LHC) is the largest and highest-energy particle accelerator in the world. The pixel detector is a subsystem of the ATLAS detector and provides a lot of data to be used for identification and reconstruction of primary and secondary vertices.

In 2013 a new layer called the Insertable B-Layer (IBL) will be installed as an additional pixel layer. This innermost layer of the pixel detector will provide 448 front-end chips (FE-I4) serving about 12 million pixel cells. To meet the communication requirements of these chips the readout system must be updated. On the off-detector side the Read Out Driver (ROD) and the Back of Crate card (BOC) are responsible for data acquisition and processing. Both cards were completely redesigned and are equipped with state-of-the-art FPGA technology.

The BOC consists of three Xilinx Spartan 6 FPGAs. The signal processing of the incoming data and the conversion to the optical interfaces to and from the detector and to the higher-level readout is done by two BOC Main FPGAs (BMF). The BMFs are connected to several optical interfaces that are mounted on the BOC. To and from the detector custom-made TX-plugins and commercial SNAP12 modules can be used. The connection to the higher-level readout is made with commercial (Q)SFP modules. The third FPGA is the BOC Control FPGA (BCF) and provides the control logic for all modules on the BOC.

Between ROD and BOC different types of interfaces are used. The Setup Bus connects the control interfaces of both cards and allows easy access to all BOC registers. The data from the detector is sent over eight 8-bit wide busses with four address and control signals. The ROD processes this data and sends it back to the BOC over the S-LINK interface to the higher-level readout.

The communication to the front-end chips (FE-I4) is an important part of the BOC firmware. All data to the FE-I4 has to be multiplexed with the system clock. This is done with the bi-phase-mark encoding and allows clock and data to be sent over the optical interface to the detector. In the direction from the detector to the off-detector readout 8b10b-encoded signals are used. This allows easy data recovery and word alignment on the receiver side. The serial data stream is parallelized and forwarded to the ROD. Redundancy in the 8b10b-encoding can be used to provide certain control words, e.g. “start of frame”or “end of frame”, and also allows error detection capability on the receiver side.

The first measurements performed with the new prototype were very successful. The readout of an electrically connected FE-I4 single chip card can be done. The communication to the BOC is done over the Setup Bus which is working very well. This paper will present the result of these and many other tests, that have been performed for firmware and hardware testing.

Primary author: WENSING, Marius (Bergische Universitaet Wuppertal (DE))

Co-authors: GABRIELLI, Alessandro (Universita e INFN (IT)); POLINI, Alessandro (Universita e INFN (IT)); KUGEL, Andreas (Ruprecht-Karls-Universitaet Heidelberg (DE)); FALCHIERI, Davide (Universita e INFN (IT)); DOPKE, Jens (CERN); GROSSE-KNETTER, Joern (Georg-August-Universitaet Goettingen (DE)); SCHROER, Nicolai Christian (Ruprecht-Karls-Universitaet Heidelberg (DE)); KRIEGER, Nina (Georg-August-Universitaet Goettingen (DE)); MAT-

TIG, Peter (Bergische Universitaet Wuppertal (DE)); TRAVAGLINI, Riccardo (Universita e INFN (IT)); HEIM, Timon (Bergische Universitaet Wuppertal (DE)); FLICK, Tobias (Bergische Universitaet Wuppertal (DE))

Presenter: WENSING, Marius (Bergische Universitaet Wuppertal (DE))

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