The 120Gbps Optical Transmitter Development for the High-Luminiosity LHC Experiments

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Introduction

The development of a high-speed, low power, radiation-tolerant optical data link is a critical task for the LHC upgrade. We conceive a 120Gbps transmitter module, i.e., a 12-channel, 10Gbps per channel, parallel pluggable module to operate on the detector front-end. The parallelization is realized via dense multiplication (120G_MTx) or array photonics (120G_ATx).

The 120G_MTx module incorporates individual 10Gbps single TOSA and driver components, densely placed in a compact package. Customized optical latch mechanism provides reliable performance and material reduction. The 120G_ATx module is based on array VCSEL and array driver components. This module provides even higher density and consumes less power. These designs are based upon emerging commercial parallel transceiver platforms and will be customized in collaboration with industrial partners.

For applications with an emphasis on HI-LHC tracker level radiation resistance, various custom ASICs are being designed while several commercial optical transceivers (QSFP, PPOD and miniPOD) and sub-components (single channel VCSEL driver and array driver) are investigated for their irradiation effects.

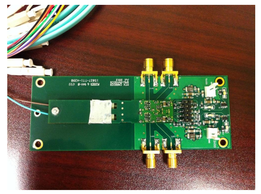
MTx Design

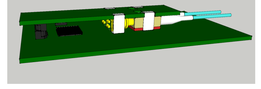
Given the challenge of array ASICs and array optics, the multiplexing of single transmitter with reduced footprint is to be explored first.

The MTx module is an adaptation from the SF_VTRx module proposed by the Versatile Link project. Two transmitters are included in each module card, with six cards fill a 120Gbps transmitter interface.

The following mechanical designs are implemented

- The Low profile locking connectors render a stack height of 6mm and a looping of the data transmission path.
- The milled notches on the module PCB provide both lateral and axial confinement. The U clamps and shims provide the vertical stability.
- Commercial LC connector without the tab can be used.





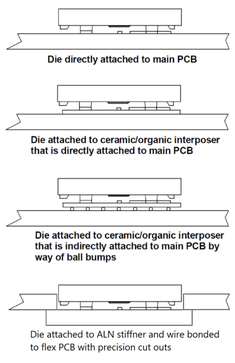
Prototype

The following process options are been discussed with assembly vendors

- Die on PCB – difficult due to surface smoothness
- Ceramic substrate -- substrate can be too thin to be stressed by PCB flexure
- Ceramic interposer – complex but reduced strain through ball bumps
- FPC with stiffener and cutout -- fiducial and pattern needed for precisic placement

These design objectives are to be evaluated with the prototypes

- The construct accommodates 10Gbps signal integrity
- There is no significant change in intrinsic attenuation under irradiation
- Reasonable hermasticity under humid condition
- Sufficient thermal conductivity for a compact 1W/unit power dissipatio and for stable optoelectronics performance



Future Work

- Neutron tests on selective COTS and components are schedule in Oct, 2012.
- Evaluation boards for SiGe and CMOS based commercial array driver are designed for irradiation tests and are submitted for fabrication.
- System margin on MTX front-end transmitter and commercial parallel receivers will be further investigated.

Proposal

With today' s data center application demands, there is a ubiquitous use of multi-mode data links of 10Gbps with reach up to 300 meters. The parallel VCSEL array transmitter and receiver (transceiver) technology is also in production. There is obvious advantage to customize the commercial modules with radiation tolerance components. An alternative approach is the integration of silicon IC and III-V light emitters (silicon photonics). Such single mode link is capable of 10Gbps or higher transmission over 10km. Parallelization is realized by PLC based optical wavelength multiplexing.

The Colliding Detector Research and Development High Speed Data Links Program collaborators have proposed a synthetic project as the following.

		Tracker (500kGy)		Calorimeter (25kGy)	
SM	TOSA	COTS _FP	TOSA	COTS _FP	
		GBLD		ONET1101L	
	Integrated Modulator	COTS PIC	Integrated Modulator	COTS PIC	
		BSTO MZI		BSTO MZI	
MM	TOSA	COTS_VCSEL	TOSA	COTS _VCSEL	
		custom_driver		ONET8501V	
	Array	COTS _VCSEL_array	Array	COTS _VCSEL_array	
		opto inteface		opto interface	
		custom_driver_array		custom_driver_array	

ATx Designs

Three array packaging design concepts are researched:

1) Optical interface with photonic turn connector

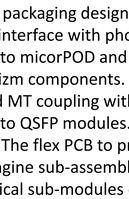
Adaptation to micorPOD and mid-board modules. Use Usconec MOI and Prizm components.

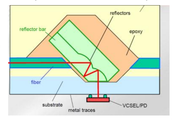
2) Standard MT coupling with flex circuitries

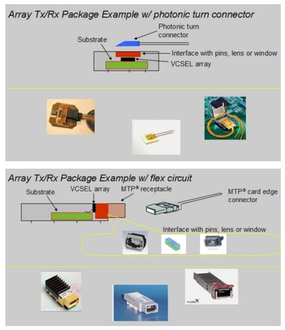
Adaptation to QSFP modules. Use Usconec lens holder and DOC lens arrays. The flex PCB to provide 90 degree turn.

3) Opto-engine sub-assembly

Drop-in optical sub-modules developed by Xloom. Complete transceiver module Avdat development roadmap envisioned.







Pictures courtesy MENO Co. Ltd, Usconec, Xloom

System Consideration

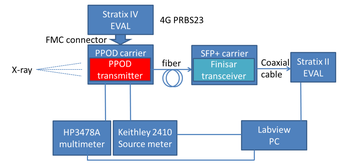
- The parallel transmitters are designed to work with commercial parallel receivers at the back-end, which have relaxed specifications as compared to single channel transceivers.
- A retrofit of the link model is conducted with the these assumptions: 100m OM3, TP2 DJ input 26.2ps, TP3 DCD 17.5ps, Rise/fall 40ps. The dispersion induced penalty simulation fits well with specification. The receiver sensitivity reduction is set by a conservative number.
- For the ATx transmission to be stretched from 100meter to 150meter, link penalty will increase by another 1dB as compared to the exampled SR10 link budget. This has to be compensated by higher Tx_OMA or lower Rx_sen.

Tx over Rx	8.30	dB
attenuation	0.40	dB
connetor loss	1.50	dB
ISI	2.80	dB
RIN, reflect etc.	0.00	dB
MPN, MN, cross etc.	0.70	dB
unallocated (crosstalk)	2.90	dB
link margin for rad-tal	0.00	dB

Summary

A 120Gbps optical transmitter (12-channel, 10Gbps per channel, parallel pluggable module) to operate on the detector front-end for the readout and control of High-Luminosity LHC (HL-LHC) experiments is proposed. We present the design concepts based on multiple TOSAs, precision array coupling and drop-in opto engines and the prototype development up to date.

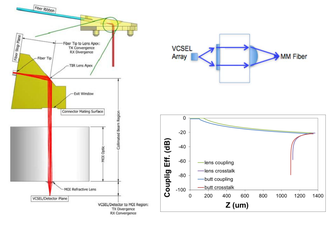
Commercial Module Irradiation Tests



- Gamma tests of QSFP transceiver and edge emitting laser driver have demonstrated total dose up to 75krad and 900krad. Only the target device was exposed to radiation while the rest of a complete optical transmission link at 5Gbps was shielded.
- X-ray tests of miniPOD, PPOD and VCSEL driver have demonstrated total dose up to 66krad, 150krad and 178krad respectively.
- In all cases, the I2C link broke down first, preventing proper link configuration upon power recycle.

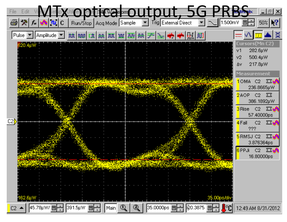
Optical Interface

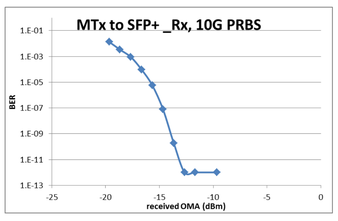
- Both butt-coupling and lens coupling are reasonably tolerant to lateral and axial alignment, with minimal cross talk impact.
- Aside from packaging reliability, as data rates and power level increase, the VSCEL divergence angle may start to cause problems in a butt couple.
- Mirco optical interface from array devices become commercially available for module vendors recently.
- We are in pursuit with more detailed micro lens parameters; the assumed simulation results are reasonably close to the vendor provide specification.



coupling scheme	-1dB insLoss		-3dB insLoss	
	lateral	axial	lateral	axial
butt-coupling	10um	90um	21um	126um
microlens array	14um	110um	24um	150um

Test Results





- Stand alone bit error rate testers and oscilloscopes are used to characterize individual channels. FPGA based bit error rate testers with FMC connectors (Altera S4GT kit and Kintex7 kit) are used to drive a complete module.
- 5Gbps eye diagram of the optical output of MTx prototype version 1 and BER waterfall curve of an MTx to commercial receiver 10Gbps transmission are shown above.

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