MULTI-GIGABIT WIRELESS DATA TRANSFER AT 60 GHz

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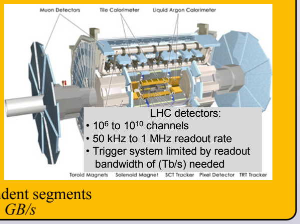
Motivation

- The ATLAS and CMS experiments@LHC consists of several million channels
- Data Transfer rate is today limited by the available:

- ***Bandwidth***

limited by

- ***Power budget (Gbps/W)***
- ***Mass (Gbps/g)***
- ***Space (Gbps/cm²)***



LHC detectors:
- 10^6 to 10^{10} channels
- 50 kHz to 1 MHz readout rate
- Trigger system limited by readout bandwidth of (Tb/s) needed

Example: Innermost silicon layer:

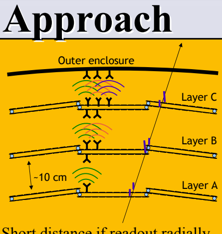
- Required bandwidth is *50-100Tb/s*
- Detector divided into *20-50K* independent segments
- Required bandwidth per link is then *5 GB/s*

Our Approach

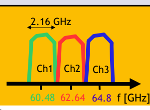
Use of the MilliMeter Wave (MM-Wave) technology at 60 GHz

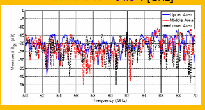
Offers:

- Wireless ***unlicensed spectrum of 7-9 GHz bandwidth*** available world-wide.
- Largely unused today: *low interference probability*
- ***60 GHz*** does not penetrate walls: *security*
- Able to send ***Gigabits/s*** (depend on modulation sch.) of information over short distance (1-10m) and ***LOS*** relaxes a few physical limitations
- Small form factor
- High transmit power: ***40 dBm EIRP*** (Effective Isotropic Radiated Power) allowed in most regions.
- Flexibility of placement and no cables needed
- Allows for integration of antenna(s)



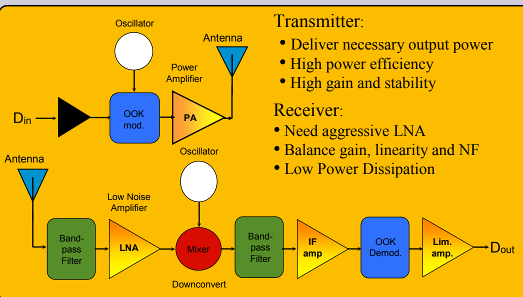
Short distance if readout radially.





- 60 GHz signal cannot penetrate through the silicon layers
- *Solution*:
- Send the data through the Silicon layers by a wire connection, with an antenna on both sides.

Transceiver Architecture



Transmitter:
- Deliver necessary output power
- High power efficiency
- High gain and stability

Receiver:
- Need aggressive LNA
- Balance gain, linearity and NF
- Low Power Dissipation

Link Budget Calculation

Required Bit-Errror-Rate (BER: 10-12

OOK Modulation: (Eb/No = 17dB

$$SNR_{\min} = \left(\frac{E_b}{N_0}\right) \cdot \frac{R}{B} = 14\ dB$$

$$P_{RX} = SNR_{\min} \cdot N_0 \cdot B \cdot F = -57\ dBm$$

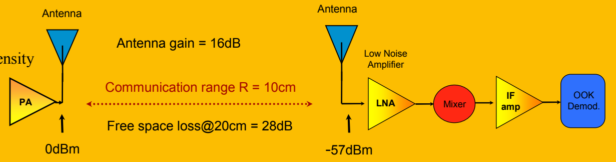
- Eb/No: Energy per bit to noise power spectral density
- R: Data bit rate
- B: Bandwidth
- F: Noise Figure
- PRX: Receiver sensitivity

$$P_{RX} = P_{TX} + G_{TX} - L_{TX} - L_{FS} - L_M + G_{RX} - L_{RX} = -57\ dBm$$

$$SNR_{in} = P_{in} - N_{Floor}$$

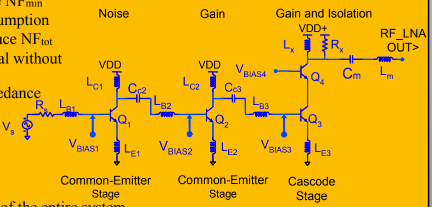
$$N_{Floor}\ -174\ dBm/Hz + 10\log(B) = -77\ dBm$$

$$NF_{RX} = SNR_{in} - SNR_{o(\min)} = P_{in} + 174\ dBm/Hz - 10\log(B) - (E_b/N_o) - (R/B)dB = 7\,dB$$

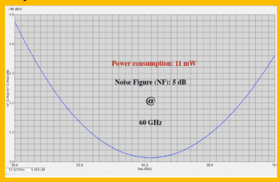


Low Noise Amplifier (LNA)

- Low Noise Figure NF_{min}
- Low Power Consumption
- Large gain to reduce NF_{tot}
- Handle large signal without distortion
- Input, output impedance matching
- Isolation between input and output



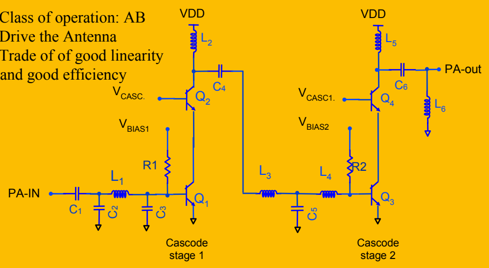
- Sets a lower limit of the entire system
- Optimized for minimum NF and maximum gain



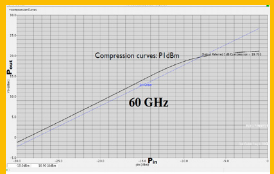
Noise Figure NF:	5dB
Reverse Isolation S_{12}:	-20 dBm
P_{1dB}:	-20dBm
Gain:	20dB
3dB bandwidth:	20 GHz
Power supply:	1.5V
Power consumption:	11mW
Input match S_{11}:	-40 dB
Input/output imped.:	50 Ω

Power Amplifer

- Class of operation: AB
- Drive the Antenna
- Trade of of good linearity and good efficiency



- Provide the signal with the required power level to insure that the transmitted signal reaches the receiver with the required power level.
- To provide high gain, and improve the Power Added Efficiency (PAE) and isolation is a two-stage cascode topology chosen.



Preliminary

Compression point P1dB:	20dBm
Forward gain S_{21}:	30dB
Reverse Isolation S12:	-65dB
Power Added Efficiency:	25dBm

Technology

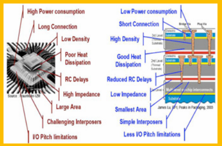
SiGe HBT BiCMOS compared to CMOS

- For equal performance, SiGe requires less aggressive lit.(2 gen.)
- Higher breakdown voltage at fixed performance
- Much larger gm/um2 (need big MOSFETs for high fmax)
- Lower 1/f noise
- Modeling is easier for high frequency design
- Matching is superior compared to CMOS devices
- Radiation hardness

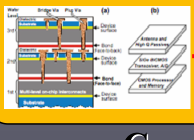
SiGe BiCMOS technology combines both high speed HBTs with relatively high breakdown voltage and standard CMOS transistors allowing a very high integration level

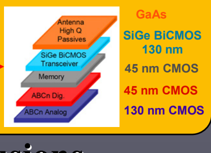
3-D Development

- **Better electrical performance**
- **Lower power consumption and noise**
- Smaller wire-length will decrease the average load capacitance and resistance.
- Lower wire to wire capacitance reduce noise coupling between signal lines.
- Form factor improvement
- Lower cost
- More functionality
- Heterogeneous integration



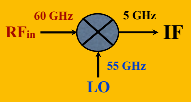
- Move from horizontal 2-D chip layouts to 3-D chip stacking.
- Increased performance - Outscaling Moores's law (More than Moore).
- **Decreasing system risk.**
- E.g. Stacking a 130 nm analog die with a 65 nm digital die, rather then trying to build a 65 nm mixed signal SOC.
- **Reducing cost: at some point, 3-D integration will be cheaper than shrinking further the 2-D design.**





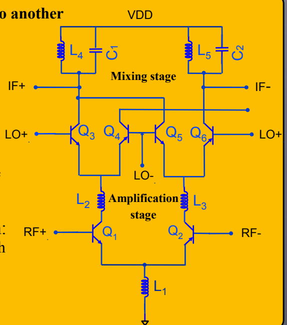
Gilbert Mixer

Convert the signal from one frequency to another



- Linearity is an issue since it must handle amplified signals

Double balanced Gilbert cell chosen:
- Differential structure, LO-IF feedthrough is suppressed
- All even harmonics are cancelled
- It provides reasonable gain

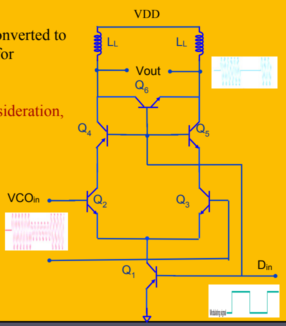


Modulation

Analog or Digital information is converted to signals at RF frequencies suitable for transmission.

Modulation technique is a key consideration, since it determines:

- System bandwidth
- Efficiency
- Power efficiency
- Sensitivity
- Complexity

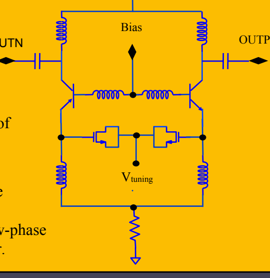


Voltage Controlled Oscillator

Used as the Local Oscillator (LO) for the modulation and the mixer

VCO metrics:
- Accuracy of oscillation
- Phase noise
- Tuning sensitivity and linearity
- Output power

- The voltage controlled frequency of operation is achieved by a voltage dependent capacitance.
- The VCO provides the reference frequency to modulate/demodulate the RF signal.
- Colpitts topology is chosen for low-phase noise and high frequency behavior.



References

1. ATLAS Tracking Trigger: Matt Warren ACES 2011
2. Radio Frequency Integrated Circuit Design: J. W. M. Rogers and C. Plett
3. R.Brenner and S. Cheng, "Multigigabit wireless transfer of trigger data through millimetre wave technology" Workshop on Intelligent Trackers 2010
4. H.K Soltveit et al, " Multi-Gigabit wireless transfer at 60 GHz" Workshop on Intelligent trackers 2012

Conclusions

•mm-wave technology presented as a possible solution for current bandwidth limitations of LHC experiments (ATLAS, CMS)

- A 60 GHz transceiver has been proposed
- Schematic of some blocks shown
- Simulations of some blocks shown
- SiGe BiCMOS (and CMOS) technology very well suited for 60 GHz wireless communication front-ends.

- There are several challenges to integration of mm-wave systems on a silicon substrate in spite of its numerous advantages
- 3-D integration opens up new possibilities for the near future that can potentially remove the drawbacks of the 2D solution.