Prototype linear voltage regulators for the ABCN130 front-end chip

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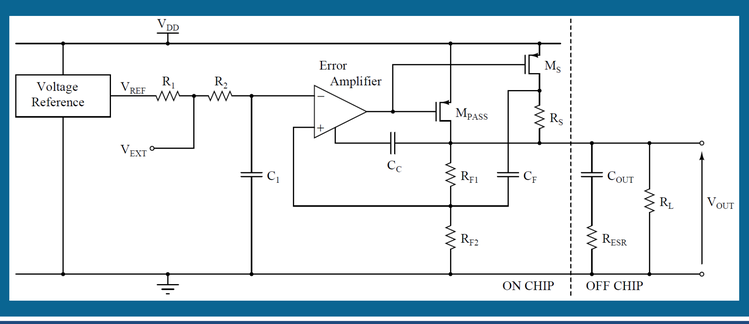
The power distribution systems in the ATLAS Inner Tracker Upgrade require linear voltage regulators on the front-end chips as the last stages of the powering chains. We present two different designs of the linear voltage regulators. One design is a true Low Dropout (LDO) voltage regulator employing a PMOS transistor in the common source configuration as the pass element. Another regulator prototype is based on an n-channel pass transistor in the classical source follower configuration. Both regulators have been designed and prototyped in the 130 nm CMOS process and are foreseen to be integrated in the ABC130 front-end chip.

Low-dropout regulator using a *p*-channel MOS device for voltage regulation

Supply voltage : **V_{DD} = 1.25 V – 1.60 V**
Nominal output current : **I_{OUT} = 70 mA**
Dropout voltage : **V_{DO} = 50 mV**

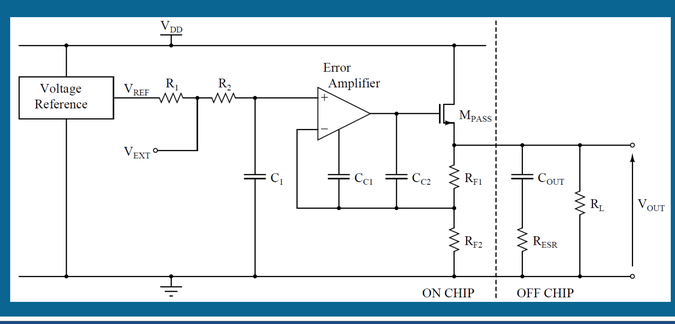


The regulator consists of the following blocks:

- bandgap voltage reference circuit,
- *R-C* filter (R_1, R_2, C_1),
- **error amplifier,**
- **pass PMOS transistor (M_{PASS})** of dimensions W/L = 15 mm / 0.12 µm,
- sensing network (R_{F1}, R_{F2}),
- **compensation network (M_S, C_F, C_C, R_S),**
- external output capacitor C_{OUT} = 100nF

Low-dropout regulator using a *n*-channel MOS device for voltage regulation

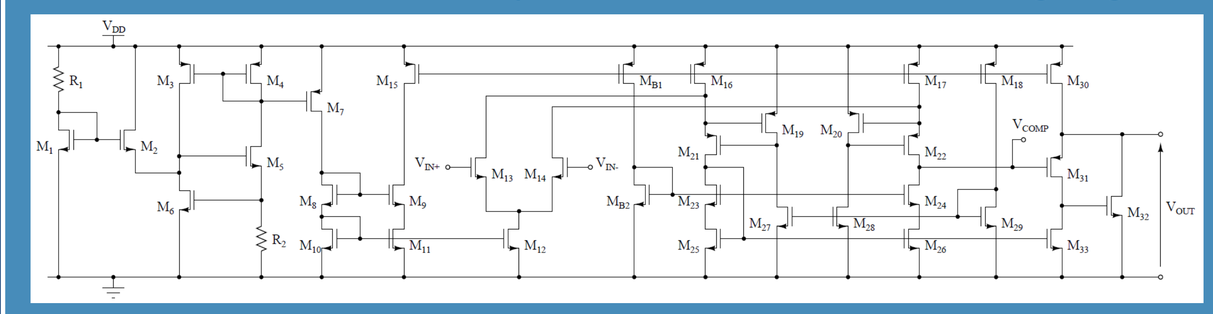
Supply voltage : **V_{DD} = 1.30 V – 1.60 V**
Nominal output current : **I_{OUT} = 70 mA**
Dropout voltage : **V_{DO} = 100 mV**



The regulator consists of the following blocks:

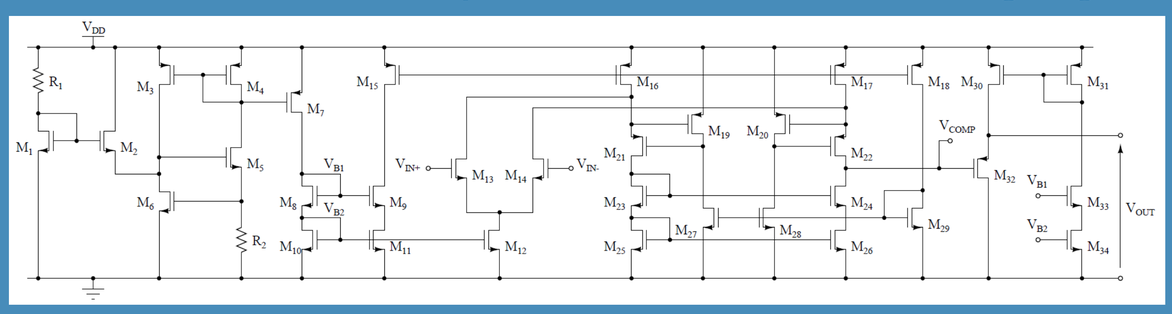
- bandgap voltage reference circuit,
- *R-C* filter (R_1, R_2, C_1),
- **error amplifier,**
- **pass zero-V_T NMOS transistor (M_{PASS})** of dimensions W/L = 40 mm / 0.42 µm,
- sensing network (R_{F1}, R_{F2}),
- **compensation network (C_{C1}, C_{C2}),**
- external output capacitor C_{OUT} = 100nF

The architecture of the error amplifier used in the PFET-based voltage regulator



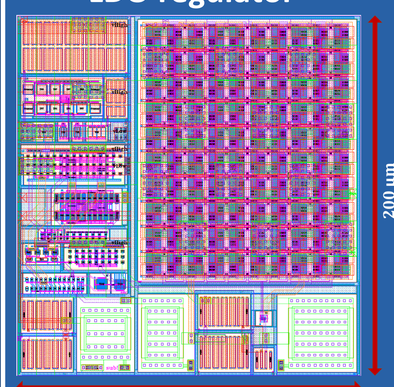
Start-up circuit | Current reference circuit and biasing | 1st stage: gain-boosted folded-cascode with high-swing cascode current sink | Biasing | 2nd stage: "super" source follower

The architecture of the error amplifier used in the NFET-based voltage regulator

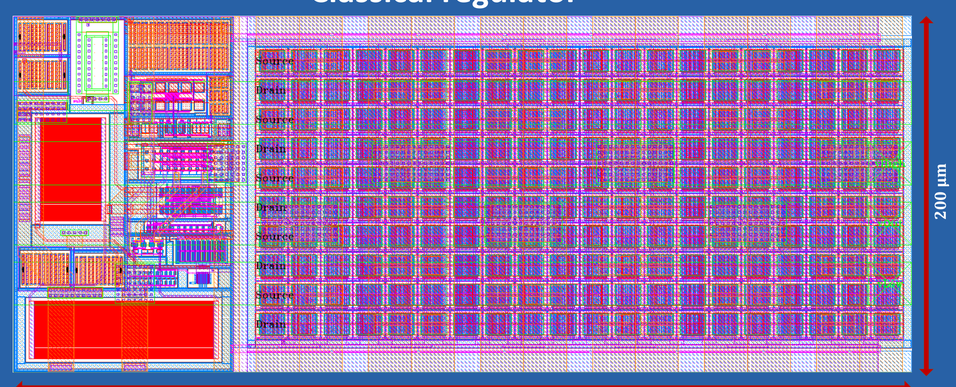


Start-up circuit | Current reference circuit and biasing | 1st stage: gain-boosted folded-cascode | Biasing | 2nd stage: source follower | Biasing

LDO regulator



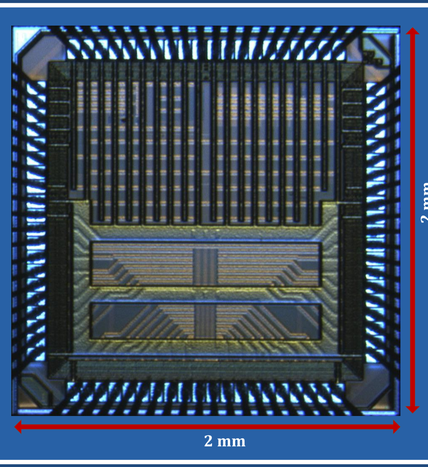
Classical regulator



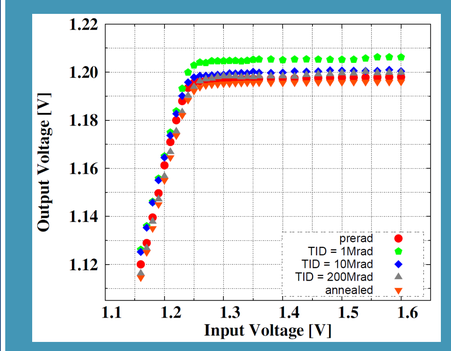
The VREG013 chip is a 2x2 mm² ASIC designed and manufactured using the IBM 130 nm CMOS technology.
The chip contains two prototypes of the linear voltage regulators, planned to be used in the design of the future ABCN130 chip.

- **PFET-based voltage regulator – area of 0.04 mm² (190 x 200 µm²)**
- **NFET-based voltage regulator – area of 0.10 mm² (520 x 200 µm²).**

Each voltage regulator is additionally equipped with separate bandgap voltage reference circuits with dimensions of 1000 x 200 µm².

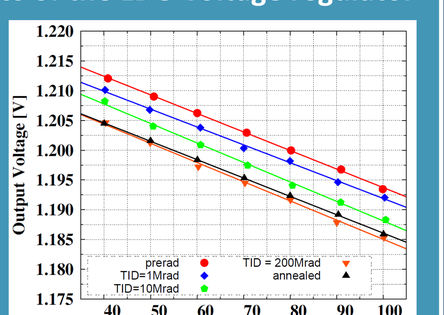


Transfer characteristics of the LDO voltage regulator



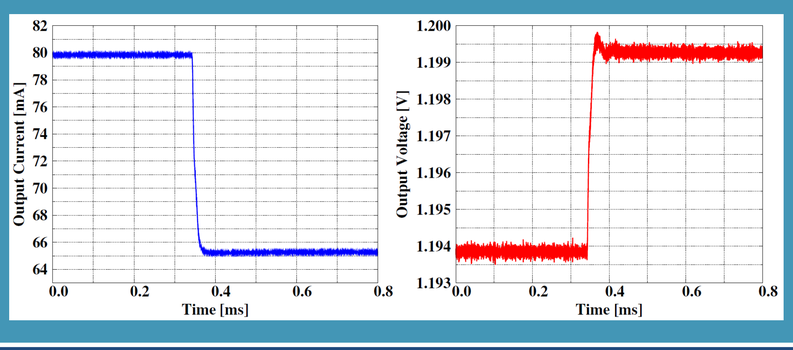
In order to measure the transfer characteristics, the input voltage was swept from 1.15 V to 1.6 V and the output voltage was monitored. This procedure has been applied to the pre-irradiated chip and then repeated after every irradiation step, and the annealing. The curves have been collected for the external reference voltage of 637 mV. The regulated output voltage remains close to 1.2V all the time during the irradiation. The measured dropout voltage is only 50 mV. Due to this fact, the input voltage range is very wide, between 1.25 V and 1.6 V.

Output characteristics of the LDO voltage regulator



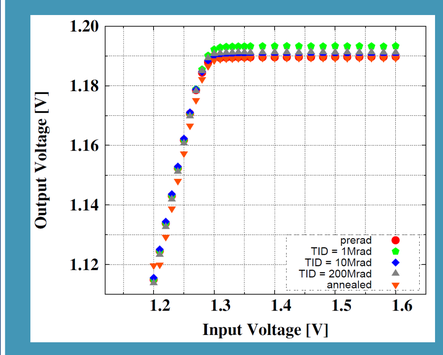
The characteristics have been measured by applying different load to the output of the regulator and monitoring the output voltage at the same time. All the presented output characteristics have been measured for the supply voltage of 1.5 V and the reference voltage of 637 mV. The output resistance calculated on the basis of these curves is 0.26 Ω and it remains constant regardless of the TID.

Measured transient response of the LDO voltage regulator to a current step applied at its output.



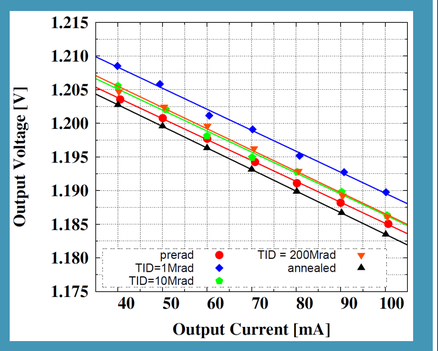
Using a simple switched current source, a step of the amplitude of $\Delta I_{OUT} \approx 14.5$ mA is applied. The output voltage fluctuation caused by the change of the load is $\Delta V_{OUT} \approx 5.4$ mV.

Transfer characteristics of the classical voltage regulator



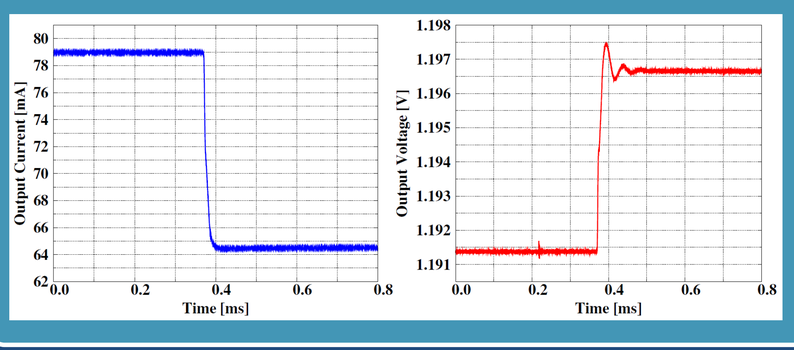
The presented curves have been measured before irradiation, for the TID of 1 Mrad, 10 Mrad, 200 Mrad and after annealing. During the test, the regulator was loaded with 70 mA. The regulator provides a stable output voltage of 1.2 V for an input voltage range between 1.3V and 1.6 V, the maximum supply voltage at which the thin gate oxide devices may be operated. The dropout voltage is V_{DO} = 100 mV.

Output characteristics of the classical voltage regulator



The characteristics have been measured by applying different load, changed from 40 mA up to 100 mA. The calculated DC output resistance is 0.28 Ω, measured for the circuit with the external reference voltage of 637 mV. The output resistance does not change significantly with the TID. However, it is higher than expected from the simulations.

Measured transient response of the classical voltage regulator to a current step applied at its output.



The presented results confirm the good AC performance of the regulator. High phase margin allows fast and smooth transient response to be obtained, and no ringing is observed. It has been measured that a change in the output current of around 14.5 mA causes the output voltage to change by 5.3 mV.

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