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Prototype linear voltage regulators for the ABC130 front-end chip

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The power distribution systems in the ATLAS Inner Tracker Upgrade require linear voltage regulators on the front-end chips to be the last stages of the powering chain. In the paper we present two designs: a classical voltage regulator based on an NMOS transistor as the pass element and an LDO voltage regulator employing a PMOS device. Both prototype regulators have been implemented in the 130nm CMOS process and are foreseen to be integrated in the ABCN130 front-end chip. The designs as well as the pre- and post-radiation test results for both prototypes will be presented and discussed.

Summary

In the ATLAS Inner Tracker Upgrade the power distribution system is one of the critical aspects, which limits the tracking performance of the detector. An approximately 10-fold increase of the number of front-end channels puts stringent requirements on power dissipation in the front-end chips and on the efficiency of the power distribution system. Currently two alternative power distribution systems are being developed; a system with serial powering of silicon strip detector modules and a system with one or two DC-DC conversion stages placed on the detector modules. For each of these two possible systems linear voltage regulators are assumed to be implemented in the ABC130 front-end chip.

The first of two linear voltage regulators prototypes is based on an n-channel pass transistor in the classical source follower configuration. The IBM 130nm CMOS process offers the zero-Vth NMOS transistor hence it can be used in the design. The regulator provides a stable output voltage of 1.2V for an input voltage range between 1.3V and 1.6V, the maximum supply voltage at which the thin gate oxide devices may be operated. This means that the dropout voltage, the minimum source-to-drain voltage at which the pass transistor still has the ability to regulate the voltage, is 100mV. A low value of the dropout voltage results in significant reduction of power losses and high power efficiency. The quiescent current measured for the classical voltage regulator is approximately 0.5mA. The layout of the design (without the bandgap circuit) is compact and occupies an area of around 0.1mm2.

The second design of the linear voltage regulator prototype employs a PMOS transistor as a pass element in the common source configuration, so it can be called a true Low Dropout (LDO) voltage regulator. The regulator's output voltage has also been set to 1.2V. The measured dropout voltage is only 50mV. Due to this fact, the input voltage range is slightly wider, between 1.25V and 1.6V. The measured quiescent current for the LDO voltage regulator is 0.6mA. The layout of the LDO voltage regulator is very compact, with total area less than 0.04mm2.

The presented circuits have been integrated on a test chip manufactured in the IBM 130nm CMOS process. Each regulator is equipped with a bandgap voltage reference circuit and requires an external capacitor of 100nF. The measurements of the voltage regulator prototypes show that they fulfill the requirements concerning the level of the output voltage, output current range and voltage regulation.

The test chip with both voltage regulators has been irradiated up to 200Mrad of total ionizing dose with the measurements taken after 1Mrad, 10Mrad, 200Mrad and after annealing. The results show noticeable effects on the regulation characteristics but the effects are small and the circuits remain fully operational. Thus, we conclude that the elaborated designs are suitable to be implemented in the ABC130 chip for readout of silicon strip detectors in the future ATLAS Inner Tracker.

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