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VMM1 - An ASIC for Micropattern Detectors

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We present a 64-channel ASIC designed for micropattern detectors. The ASIC discriminates and measures the amplitude and timing of events, including sub-threshold neighbors. With 200 pF input capacitance it provides charge resolution <5,000 electrons and sub-nanosecond timing resolution at 25 ns. The shaper, based on the concept of delayed dissipative feedback, gives an analog dynamic range in excess of 5000 at 200pF and 200ns. The discriminator, of new concept, can process sub-hysteresis amplitudes. The ASIC also provides sparse readout, trigger and address of the first event in real time, and direct timing outputs.

Summary

The Micromegas and Thin Gap Chambers to be used for the ATLAS muon system upgrade will need to provide the momentum measurement as well as participate in the Level1 trigger. The challenging detector requirements must be coupled with appropriate readout electronics which must provide pulse amplitude, timing measurements and trigger information for more than 2 million channels. The limited bandwidth of the readout link requires on-chip zero suppression. For reliable operation in the environment of ATLAS, radiation tolerance, SEU imunity are also required.

VMM1 is a first prototype ASIC designed for this upgrade, but it integrates features that make it suitable for other applications. Fabricated in 130nm CMOS, it has 64 channels, each providing low noise charge amplification, shaping with baseline stabilization, discrimination with trimming, peak/timing measurement. It also integrates a temperature sensor, a pulse generator, and mixed signal multiplexers. The address of the first event and the direct timing are also available. A revision of the architecture (VMM2) will integrate counters, ADCs, and a FIFO. The main features are briefly summarized below.

Analog section - Optimized for 200pF the front end can operate with sensor capacitances from 2pF to 1nF, and with charges up to 2pC. At 200pF it offers a resolution <5,000 e- at a peaking time of 25ns. The gain is adjustable (full scale 0.11 to 2.0 pC) and the polarity selectable. The shaper, a third order realized using the delayed dissipative feedback, has adjustable peaking time (25 to 200 ns).

Discrimination - Comparator circuits use positive feedback for fast response in presence of small differences. The feedback introduces hysteresis, and in order for the comparator to return to its original state after the event, the signal amplitude must exceed the hysteresis. The minimum threshold is consequently limited to a value equal to the baseline plus the hysteresis. VMM1 implements a discriminator of a new concept, capable of providing sub-hysteresis discrimination.

Peak/timing measurement - The peak/timing measurements are based on a multiphase configuration. The timing is measured at the pulse peak, resulting in sub-nanosecond resolution and negligible time-walk.

Neighbor processing logic - In normal operation only signals exceeding the threshold are processed. Optionally, also the neighbors can be processed. The edge channels can communicate to corresponding channels of a neighbor chip through bidirectional IOs.

Sparse readout - The peak and timing amplitudes and the address of processed channels are sequentially multiplexed to dedicated outputs. In VMM2 the analog amplitudes will be converted on chip and stored in a digital memory.

Address of first event in real time - When a first signal exceeds the threshold or a first peak is found, a flag is asserted and the address of that signal is made available at dedicated outputs. The sub-circuit self-resets after 40ns.

Direct timing - For 16 selected channels the pulse timing is available at dedicated digital outputs. The timing is selectable between time-over-threshold and time-to-peak.

The architecture, circuit details, and experimental results will be presented.

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