CLARO-CMOS, an ASIC for single photon counting with PMTs, MCPs and SiPMs

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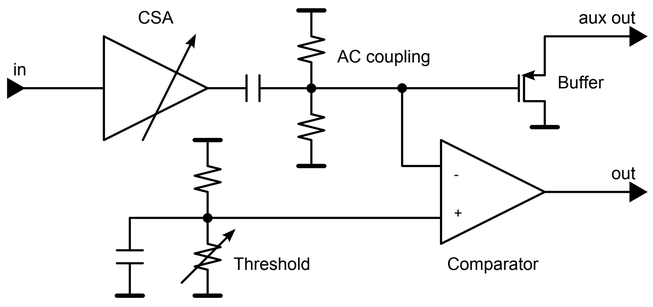
Overview

The CLARO-CMOS is a 4 channel ASIC prototype designed for fast photon counting with pixelated photodetectors (Ma-PMTs, MCPs and SiPMs).
Each channel is composed of a charge sensitive amplifier with settable gain (3 bits) and a discriminator with settable threshold (5 bits).
The prototype was realized in AMS 0.35 CMOS technology.

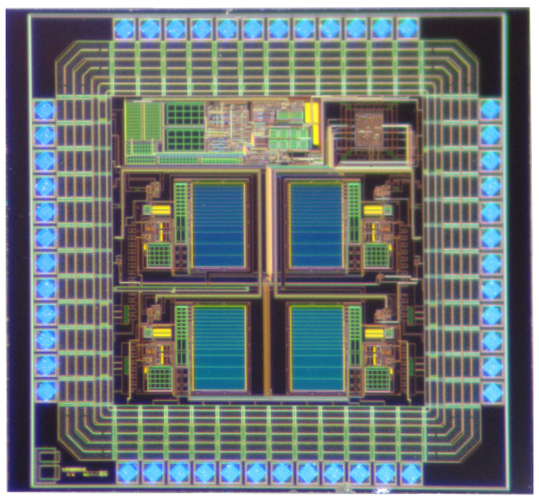


Block diagram of a CLARO-CMOS channel

Main features of the CLARO-CMOS:

- Recovery time below 25 ns for single photon signals
- Power consumption of 1 mW per channel from a 2.5 V supply
- Noise of about 7 ke- (1.2 fC) RMS with a 3.3 pF input capacitance
- Jitter down to 10 ps with a 3.3 pF input capacitance

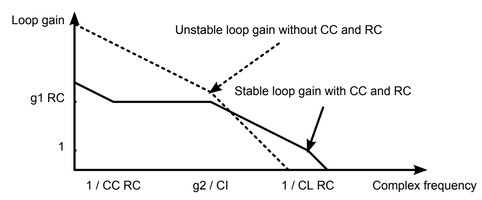
For more info: **http://arxiv.org/abs/1209.0409**



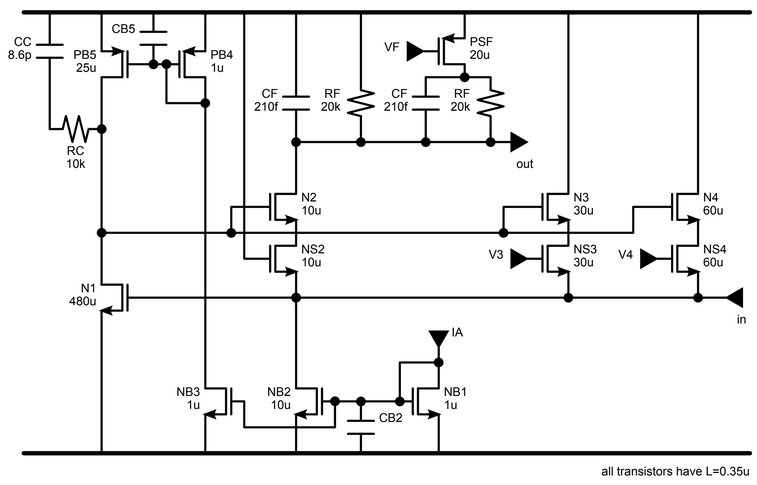
A photograph of the CLARO-CMOS die (2x2 mm^2)

The charge sensitive amplifier (CSA)

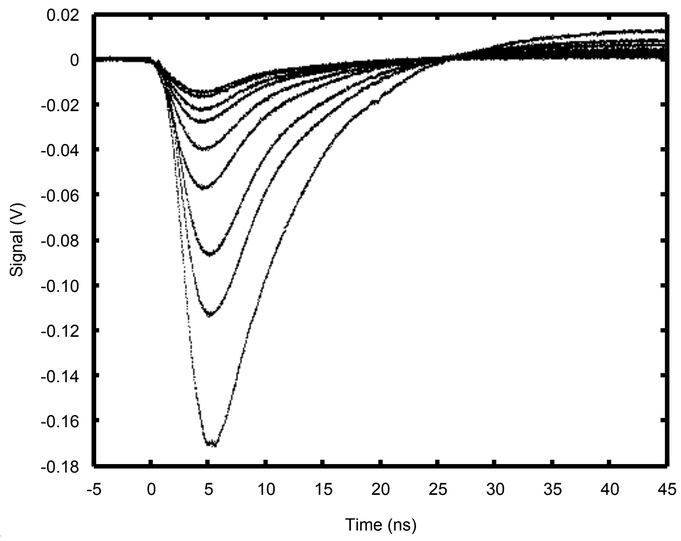
The design of the CSA is based on the "super common base" topology.
The transistor N2 is an active cascode which reads the input current pulses on a low impedance input node.
The input impedance is kept low by the feedback loop provided by N1.
The feedback loop gain at moderate frequency is g1 RC, where g1 is the transconductance of N1.
The current pulses are integrated on the capacitor CF, which is then discharged through RF. The time constant CF RF was chosen to be 5 ns.



The loop gain is made stable by RC and CC, which are used to compensate the low frequency pole due to the stray capacitance at the drain of N1.
The dominant pole of the feedback loop is at complex frequency g2 / CI, where g2 is the transconductance of N2 and CI is the input capacitance.
The switches NS3, NS4 allow to attenuate the signal at the input, while the switch PSF allows to change the value of CF and RF, giving 3 bits of gain control per channel.



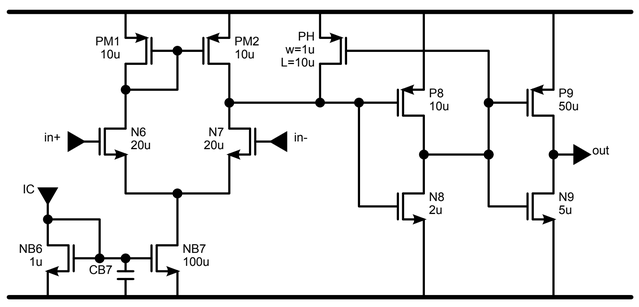
Two operating modes can be chosen for the CSA, a "low power" mode, optimized for low power consumption, and a "timing" mode, where the pulse as the output of the CSA is faster, allowing higher timing resolution.
The power consumption of the CSA is about 300 uW (120 uA at 2.5 V) in "low power" mode, and about 800 uW (250 uA at 2.5 V) in "timing" mode.



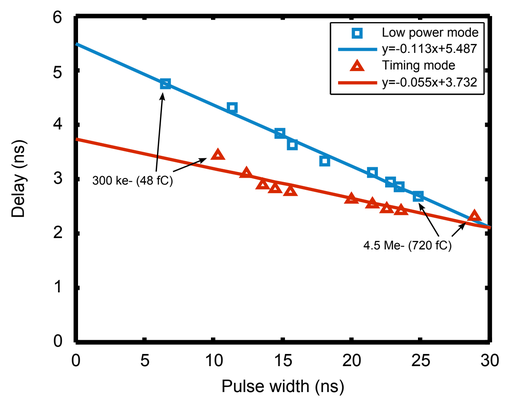
330 ke- (53 fC) to 3.3 Me- (530 fC) pulses at the auxiliary CSA output

The comparator

The comparator is composed of a differential input stage and two inverter stages.
The threshold is set at the non-inverting input by a 5-bit DAC implemented as a simple resistive divider.
At the largest gain, each threhold step corresponds to about 150 ke- (24 fC).
Transistor PH provides hysteresis, making the recovery of the input stage slower after triggering.
The output stage is designed to drive a small capacitive load, such as a PCB trace to a FPGA placed nearby.
The output inverter is not symmetric, to allow the fastest possible swing to the positive rail when a pulse is triggered.
The DC power consumption of the comparator is 250 uW (100 uA at 2.5 V).
When the circuit is triggered at a 10 MHz rate, the power consumption increases to 800 uW.

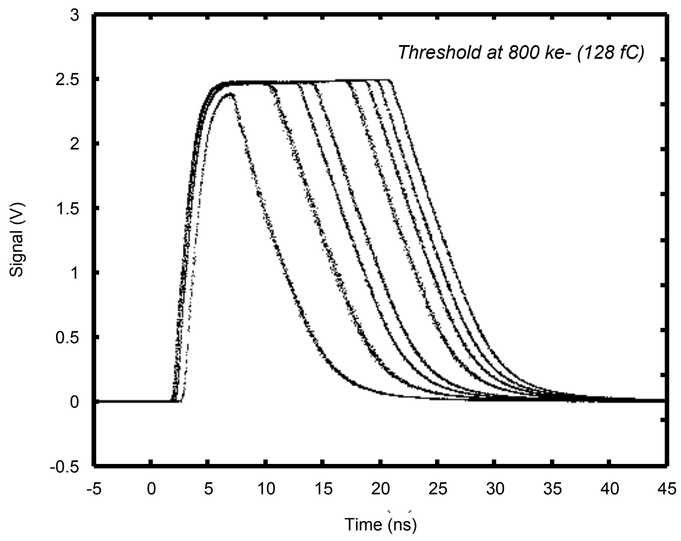


Threshold at 300 ke- (48 fC)



The width of the output pulse is proportional to the input charge, going from 5 ns to about 25 ns for signals within a factor of 10 above threshold.
The time walk can be estimated from the above curves, giving the output delay as a function of the pulse width, and is 2.5 ns in "low power" mode, and about 1.2 ns in "timing" mode, thanks to the faster pulse at the output of the CSA.

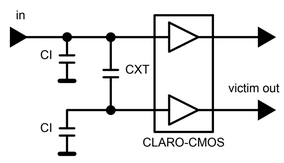
Threshold at 800 ke- (128 fC)

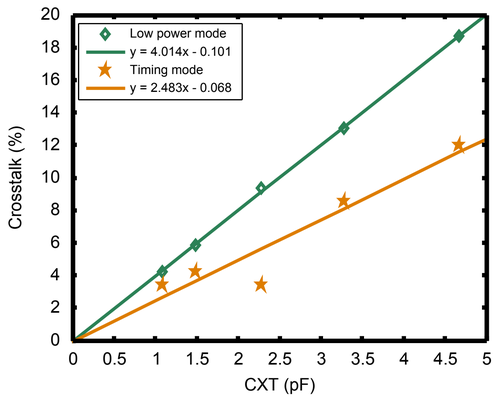


810 ke- (130 fC) to 5.6 Me- (900 fC) pulses at the comparator ouput

Crosstalk

The crosstalk was measured as a function of the capacitance CXT between two inputs, simulating the stray capacitance between the pixels of a given detector.
Here the input capacitance CI was 6.8 pF.
The crosstalk found on chip with CXT = 0, i.e. when no external crosstalk capacitance is added between the inputs, is zero.

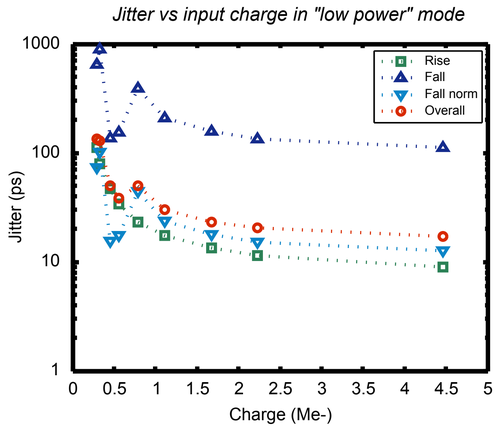




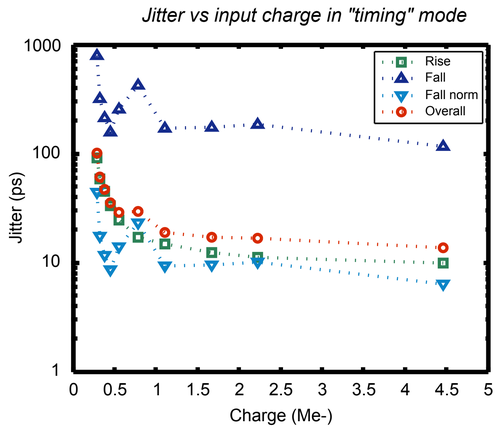
Timing and jitter

The timing error (jitter) was measured with a Agilent 81130A step generator and a Agilent DCA-X 86100D sampling scope.
The jitter contributed by the CLARO-CMOS was measured both in "low power" and in "timing" modes, with the comparator threshold set at 300 ke-.(48 fC)
Pulses from 300 ke- (48 fC) to 4.5 Me- (720 fC) were injected at the input. These charge pulses correspond to the typical single photon response of Ma-PMTs, MCPs and SiPMs.

Jitter vs input charge in "low power" mode



Jitter vs input charge in "timing" mode



The plots show the jitter on the rising and falling edges of the pulses at the output of the comparator.

In order to estimate the weight of the falling edge jitter on the accuracy of the time-over-threshold measurement to compensate time walk, the jitter on the falling edge was normalized with the slope of the time walk vs pulse width curves.
The overall jitter, including the error induced on the time walk correction, is also reported in the plots.

The overall jitter is about 10 ps RMS for signals well above threshold, both in "low power" and "timing" modes.
In "timing" mode, jitter is below 50 ps for signals larger than 380 ke- (61 fC), that is 25% above threshold.

Future steps

- A 8 channel version of the CLARO will be realized in 2013 and tested with Ma-PMTs in view of the upgrade of the LHCb RICH
- A modified version specifically tailored for SiPMs will be realized in 2013 in collaboration with groups from Ferrara, Torino and Krakow for a possible application in the SuperB IFR

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