Vertically Integrated Pattern Recognition Associative Memory for Track Finding

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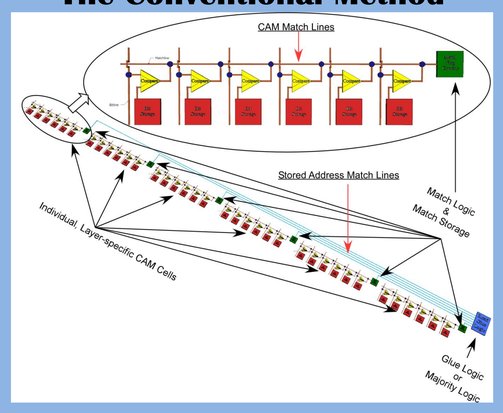
Introduction

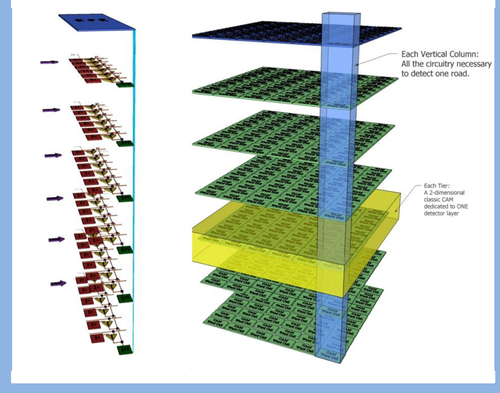
Hardware-based pattern recognition for fast triggering on particle tracks has been successfully used in high-energy physics experiments for some time[1]. The CDF Silicon Vertex Trigger (SVT) at the Fermilab Tevatron is an excellent example. The method used there, developed in the 1990's, is based on algorithms that use a massively parallel associative memory architecture to identify patterns efficiently at high speed. However, due to much higher occupancy and event rates at the LHC, and the fact that the LHC detectors have a much larger number of channels in their tracking detectors, there is an enormous challenge in implementing fast pattern recognition for a track trigger, requiring about three orders of magnitude more associative memory patterns than what was used in the original CDF SVT. Approaches to this goal in simple 2D VLSI are limited. A new concept to use emerging 3D technology to achieve this goal has been proposed [2].

The Conventional Method



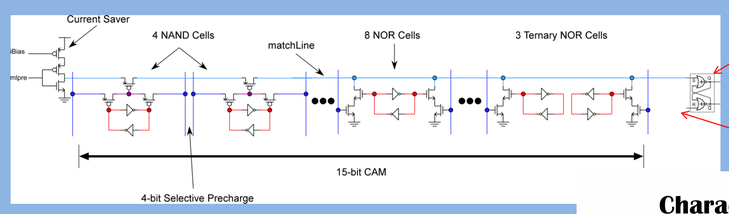
The Associative Memory approach is to use CAMs to match and Majority Logic to associate hits from different detector layers for track candidates. The essence of VIPRAM is to divide this approach up into different tiers, maximizing pattern density while minimizing critical lengths and parasitics. To demonstrate the feasibility of this approach the first goal is to develop and rigorously test the two basic 3D building blocks – the CAM Cell and the Majority Logic Cell. The VIPRAM architecture allows us to test the 3D building blocks in a simple, low-cost 2D prototype.

The VIPRAM Method



- This initial VIPRAM implementation is a division of labor that places all Control Cells (Majority Logic) in one "top" Control Tier and the CAM cells in individual Tiers corresponding to each detector layer.
- The resulting pattern "tube", shown to the left and highlighted in blue, contains all circuitry necessary to select one candidate track.
- The Stored Address Match Lines, the longest lines in the conventional method, are implemented vertically and are therefore now considerably shorter. As these lines are repeated throughout the chip, this can have a significant impact on performance.
- The vertical integration provides a flexibility in layout optimization of the building blocks, and therefore chip performance.
- The pattern density directly depends on the cross-sectional area of the tube.

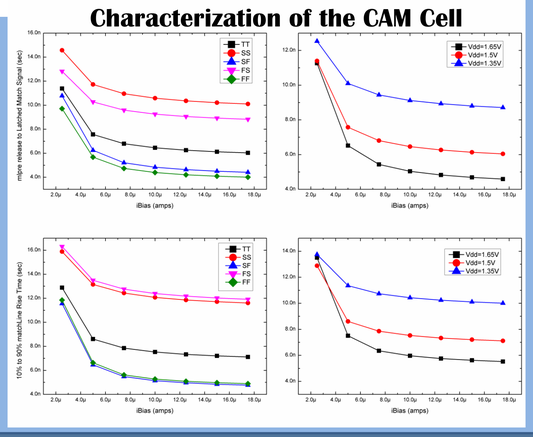
The CAM Cell



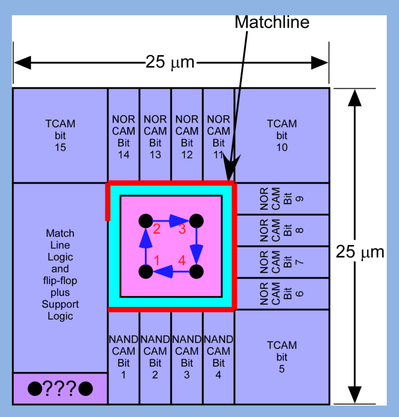
For demonstration purposes, it is useful to compare a new design to existing designs with the same core functionality[3]. Therefore, the prototype was designed as a 15-bit CAM with a 4-bit Selective Precharge, 3 Ternary CAM Cells and a Current Saver. The Selective Precharge is made with 4 NAND Cells. The 8 remaining bits are NOR Cells.

The matchLine is the single signal that connects the different bits in the CAM cell and its parasitic impedance dominates performance. The layout optimization permitted by vertical integration allows a redesign of the matchLine in the CAM cell itself. The matchLine is shortened considerably by wrapping it in a square.

Characterization of the CAM Cell

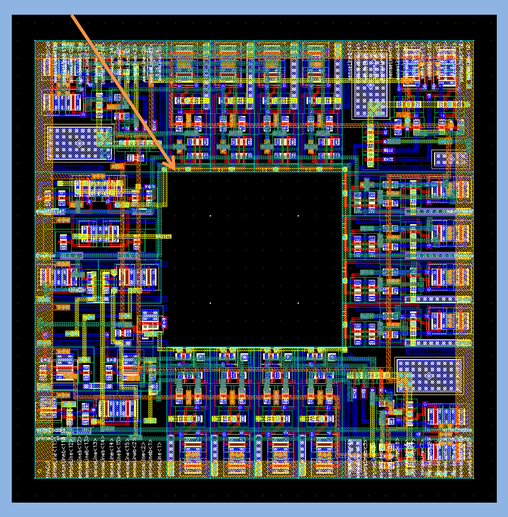


Minimizing the matchLine increases the maximum clock frequency and minimizes power consumption for a given clock frequency.



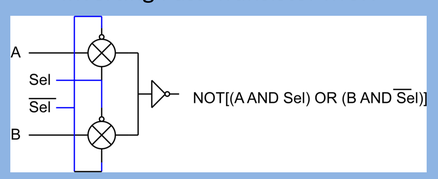
The ??? represent space reserved for extra 3D vias in the future

matchLine

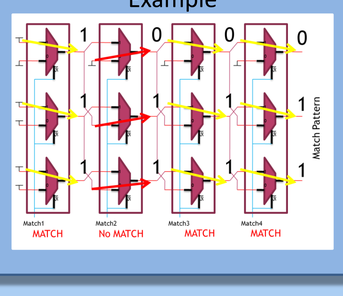


The Control Cell

Inverting Pass-Transistor MUX

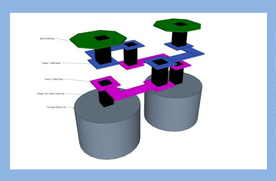


Example

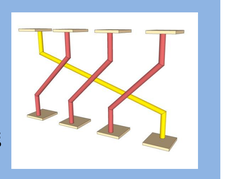


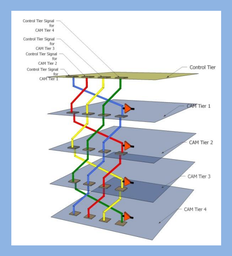
For the VIPRAM approach to work optimally, the CAM Cell and the Control Cell should be approximately the same size. This is possible because of the pass transistor logic used in the Majority Logic. The figure to the left show the 6-transistor inverting pass-transistor multiplexor. An example of the Majority Logic is also shown using non-inverting multiplexors for simplicity.

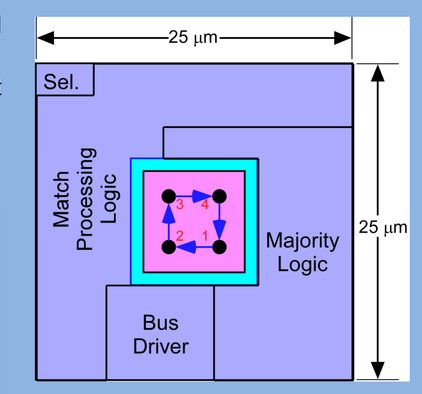
Diagonal Via

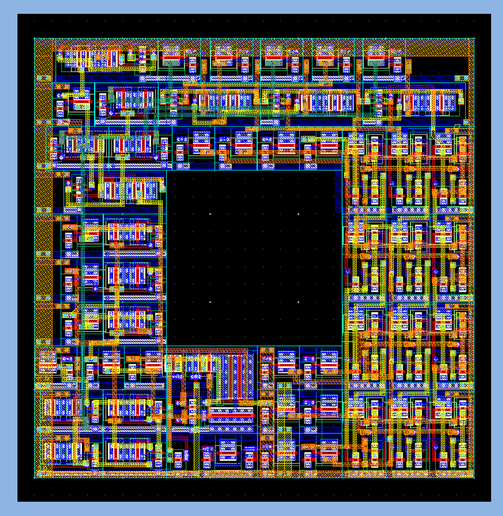


Diagonal Vias are patented VLSI structures capable of uniquely targeting one layer

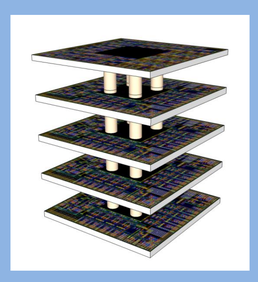


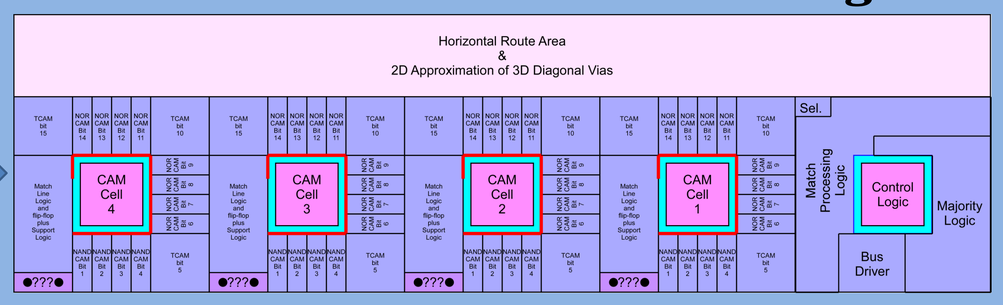


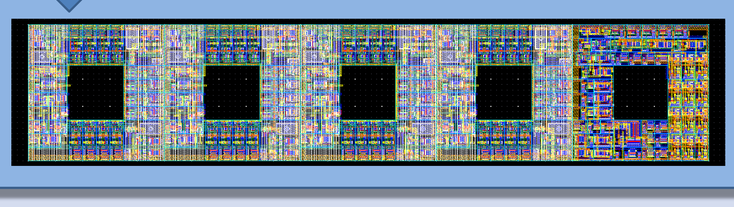




Testing Methodology of the 3D Building Blocks

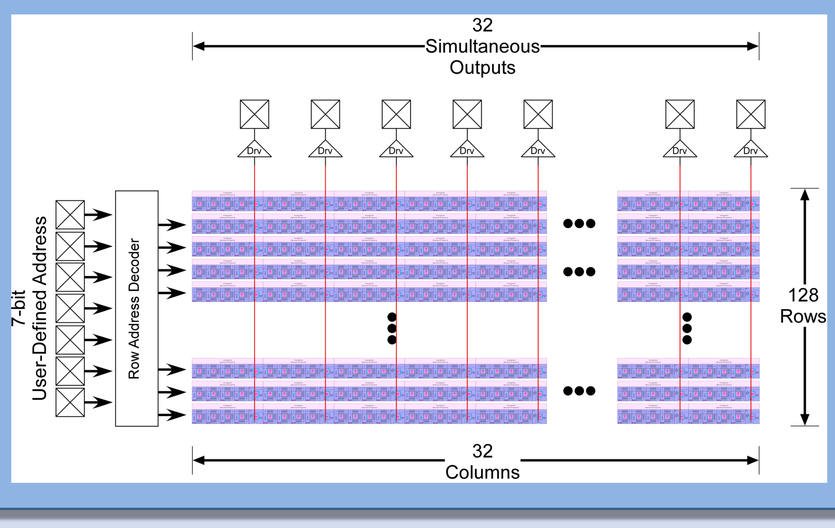




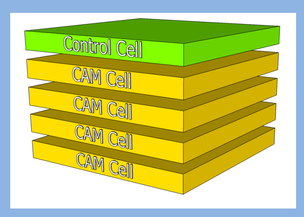


The first prototype of the new layouts will be a 2D implementation of a simple 4-CAM Layer Tube using the actual 3D building blocks. The 3D vias must be approximated in higher levels of metal and some horizontal routing space is necessary because the prototype is 2D.

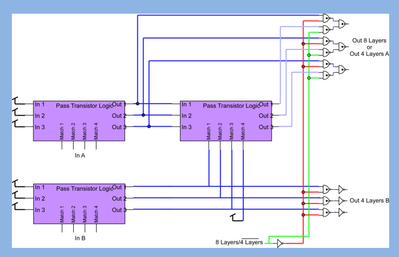
The Readout Architecture has been minimized to display the performance of the CAM and Control Cells most clearly.



Architectural Flexibility



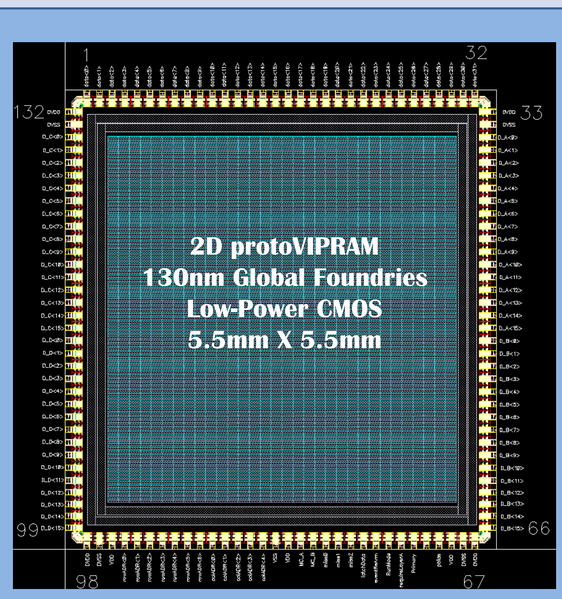
The VIPRAM architecture is intrinsically open and flexible. For example, a simple logic modification to the Majority Logic allows a combination of two "tubes" to function either as two 4-layer pattern cells or one 8-layer pattern cell.



Summary

The associative memory approach to track finding and the PRAM devices that implement it are well suited to modern 3D integration. The algorithm is easily divisible into logical partitions that are physically separable from one another due to the simplicity and consistency of the interconnects between these logical partitions. Moreover, integrating them vertically yields an immediate pattern density improvement to the associative memory approach. Diagonal Vias permit simple automatic tier self-ID which allows the VIPRAM design to be accomplished with only two mask sets regardless of the number of detector layers in the final design.

As 3D technology evolves, the spacing of Through Silicon Vias and other structures unique to 3D integration will also evolve. For the moment, it makes sense to remain at a reasonable technology node such as 130nm rather than pursue a more aggressive node such as 65nm. This will allow for relatively inexpensive prototyping. When all of the processing steps for a final VIPRAM are prototyped, then the selection of a final VLSI technology node will be clearer.



References

[1] M. Dell'Orso and L. Ristori, "VLSI Structures for Track Finding," Proceedings in Nuclear Instruments and Methods, vol. A278, pp. 436-440, 1989.
[2]T. Liu, J. Hoff, G. Deptuch, R. Yarema, "A New Concept of Vertically Integrated Pattern Recognition Associative Memory", be published in the Proceedings of the TIPP 2011 Conference, DOI number 10.1016/j.phpro.2012.02.521
[3] A. Annovi, *et al*, "Associative memory design for the fast track processor (FTK) at ATLAS, Nuclear Science Symposium and Medical Imaging Conference (NSS/MIC), 2011 IEEE Page(s): 141 – 146