Design tools and foundry access service plans for 65 nm technologies

Microelectronics User Group
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Outline

- Motivation for use of 65 nm CMOS technologies
- Technology options for 65 nm
  - Devices
  - Metal stack
  - Libraries
- Possible scheme of technology distribution for 65 nm
  - Development and integration of PDK
  - Maintenance
  - Training
  - Support
  - Foundry access
- Possible access to 130 nm technology

Motivation

- Future vertex detectors for high energy physics experiments can benefit from modern deep submicron technologies
  - Scaling is necessary to improve the performances of pixel detectors
    - Smaller pixel sizes (pitch)
    - More “intelligence” in each pixel
  - Faster serializers/deserializers
- In general, the expected advantages in porting a front-end circuit to a more advanced technology include
  - A much more compact, faster digital part (reduction in area of ~60% compared to 130nm technology)
  - Better matching than in 130nm
- Results of radiation hardness studies are very encouraging
  - See https://iopscience.iop.org/1748-0221/7/01/P01015/ , “Characterization of a commercial 65 nm CMOS technology for SLHC applications”, also presented in TWEPP 2011
  - Radiation characterization of the selected technology is nevertheless needed
- Foundry will be selected with a call for tender

Technology options

- Plenty of options… but expensive !
  - Options modulate strongly the manufacturing cost
- Low-power CMOS 65 nm
  - 1.0V or 1.2V core, 1.2V or 2.5V capable I/Os
  - Extra steps for mixed-signal/RF applications
    - MIM capacitors
      - Costly option, maybe possible to use instead Vertical Natural Capacitors (VNC, VPP, MOM, …)
    - High-Q inductors
      - Fabricated with Ultra-Thick Metal (UTM)

Technology options & costs

- Many tech. options but they all come at a cost
  - Thin metals are expensive because of their fine pitch
- 6+1 metal levels (Cu)
  - Thin metals
    - M1-M4
  - Thick metals
    - M5-M6
  - Last metal, redistribution layer (RDL)
    - used for pad (WB and bump), interconnection, laser fuses
- Devices
  - Transistors
    - Standard-, high- and low-Vt
      - Low-vt devices have high leakage
      - Standard-vt is high for typical analog applications
        - Limited dynamic range
        - ...or low-voltage architectures needed
      - Low- and high-vt are expensive options!
    - zero-vt
    - Triple well
  - Junction diodes: N+/PW, P+/NW, NW/Psub

Foundry libraries

- Wide choice of standard cell libraries from foundries
  - tapless/tap-cell (substrate/n-well contacts in each cell or not)
  - multi-Vt, multi-Vdd
  - power switches, isolation cells, level translators, …
  - several pitch sizes
    - 7-, 9-, 10-, 12-tracks, …
- IP blocks from foundries
  - SRAMs, PLLs, SerDes, specialty I/O, …
  - … but radiation tolerance must be verified

Drawbacks of 65 nm

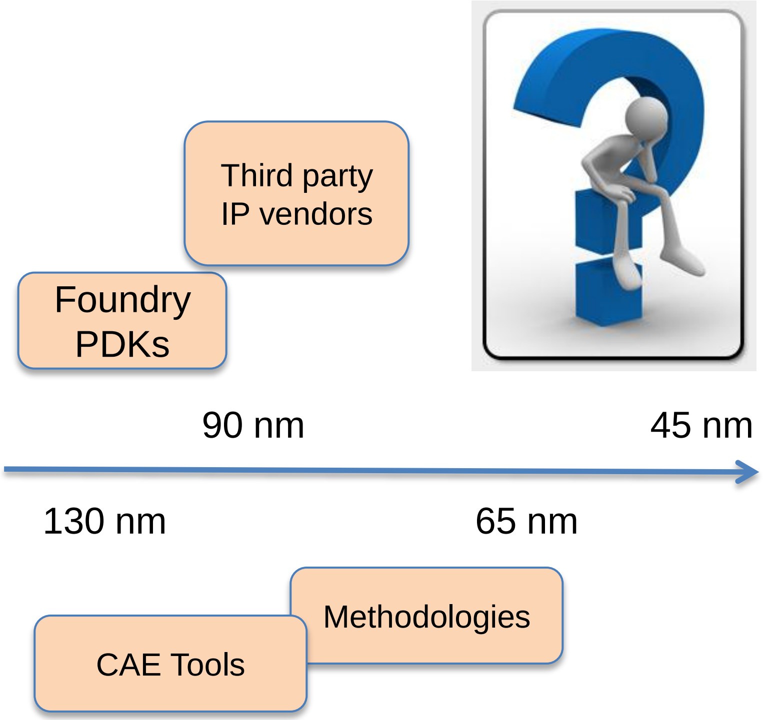
- Higher cost of tape-out compared to older technologies
  - Strong push for 1st working silicon
  - Push for more IP re-usage?
  - Must limit technology options usage
- Higher gate leakage current

	65nm technology	130nm technology
Minimum gate length	60nm	120nm
Metal layers	10	8
Power supply	1.2 V - 1.0 V	1.5 V - 1.2 V
Gate leakage	~350 pA/μm^2	20 pA/μm^2
Channel leakage (at minimum length)	~210 pA/μm	400 pA/μm
Typical transistor leakage (minL,3minW)	~85 pA	290 pA

- More stringent design rules: ELT transistors are not allowed, more difficult to achieve an optimal layout.
    - OPC rules: avoid jogs, zigzag, shapes like “L”, “U” or ring, …
- Deep submicron technologies are not optimized for analog designs
  - Smaller dynamic range due to the lower power supply reduces the possibilities to use some structures (such as cascoded stages). Multiple stages, with possible stability issues, are needed to achieve a high gain.
    - This problem is moreover aggravated by the lower output resistance of the MOSFETs which lowers the gain of the single stages.

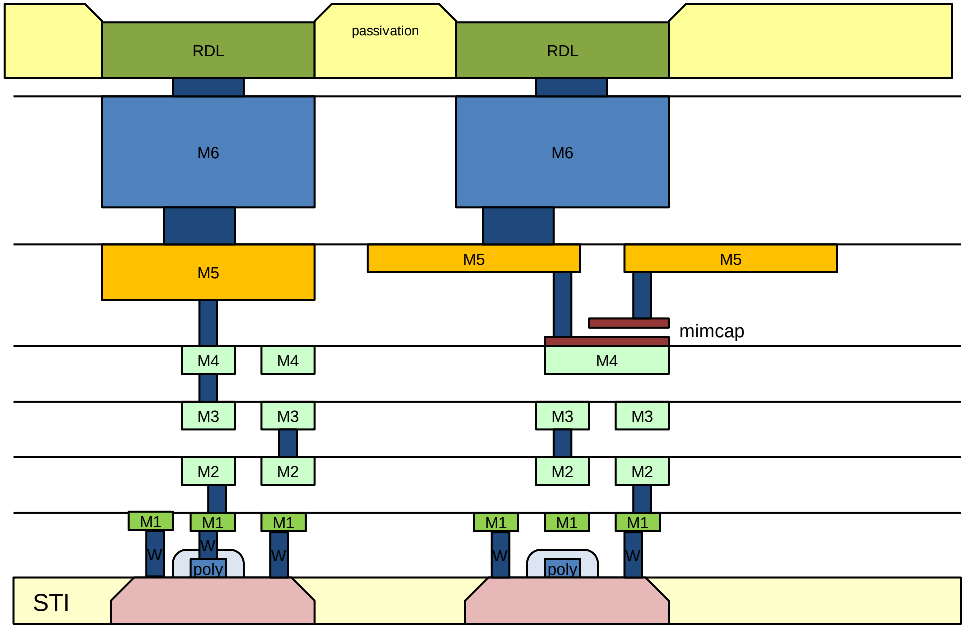
Motivation for a M/S flow

- New technologies require a stronger organization of design methodologies
  - 65 nm presents stricter design rules, more complex RC extraction, must be verified more carefully (more corners, Montecarlo), etc.
- A complex design environment
  - Projects with large, fragmented, multinational design teams.
  - Academic environment with designers having different levels of design expertise
  - Powerful and flexible CAE Tools but complicated to use.
  - Third party digital cell IP libraries primarily prepared for the back-end design flow.
  - Designs of increased complexity (SOC).
- A uniform set of tools and an uniform way of using them, for every designer is necessary
  - All design teams have to conform to a common design workflow
  - Benefits:
    - Design productivity improvements and reduced design cost
    - Successful silicon-accurate designs.
    - More manageable technical support services.



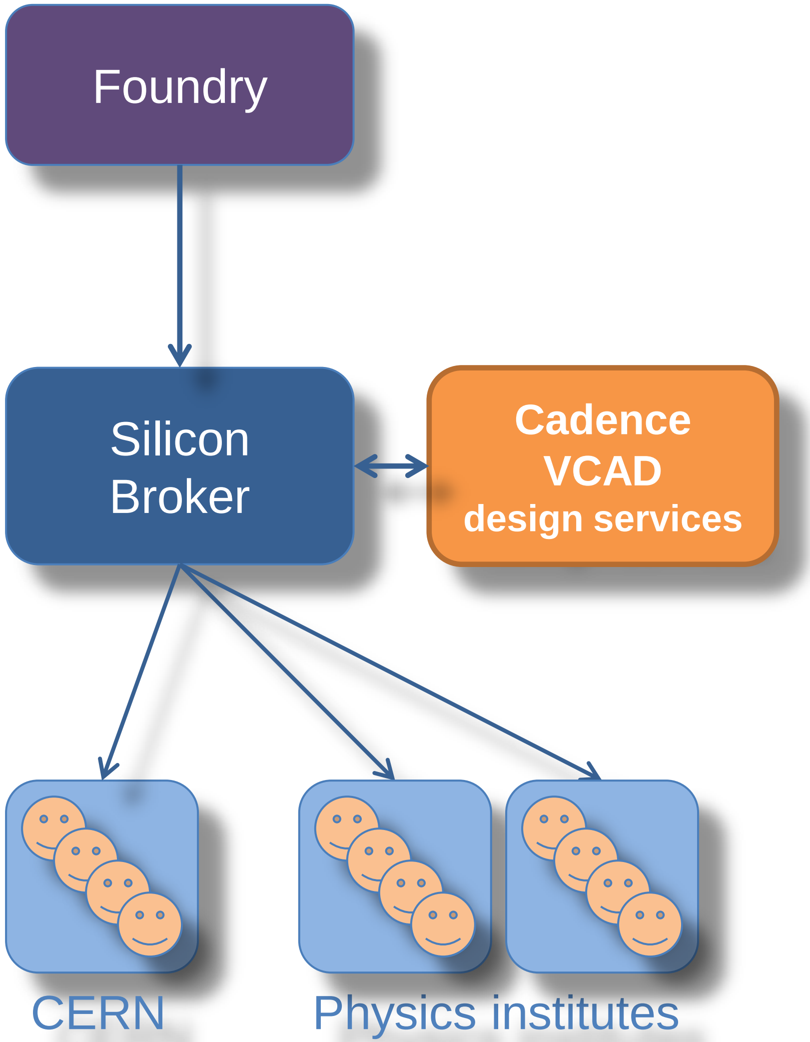
M/S flow: metal stack and libraries

- One metal stack and one library delivered at first
  - 6+1 metals
  - 4-thin, 2-thick, RDL
    - no mimcaps included by default
  - Library: 9-tracks, standard-Vt
- A second option of metal stack and library made available later (TBD)



- Many tech. options but they all come at a cost
  - Thin metals are expensive because of their fine pitch

M/S flow distribution #1

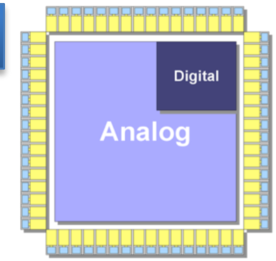


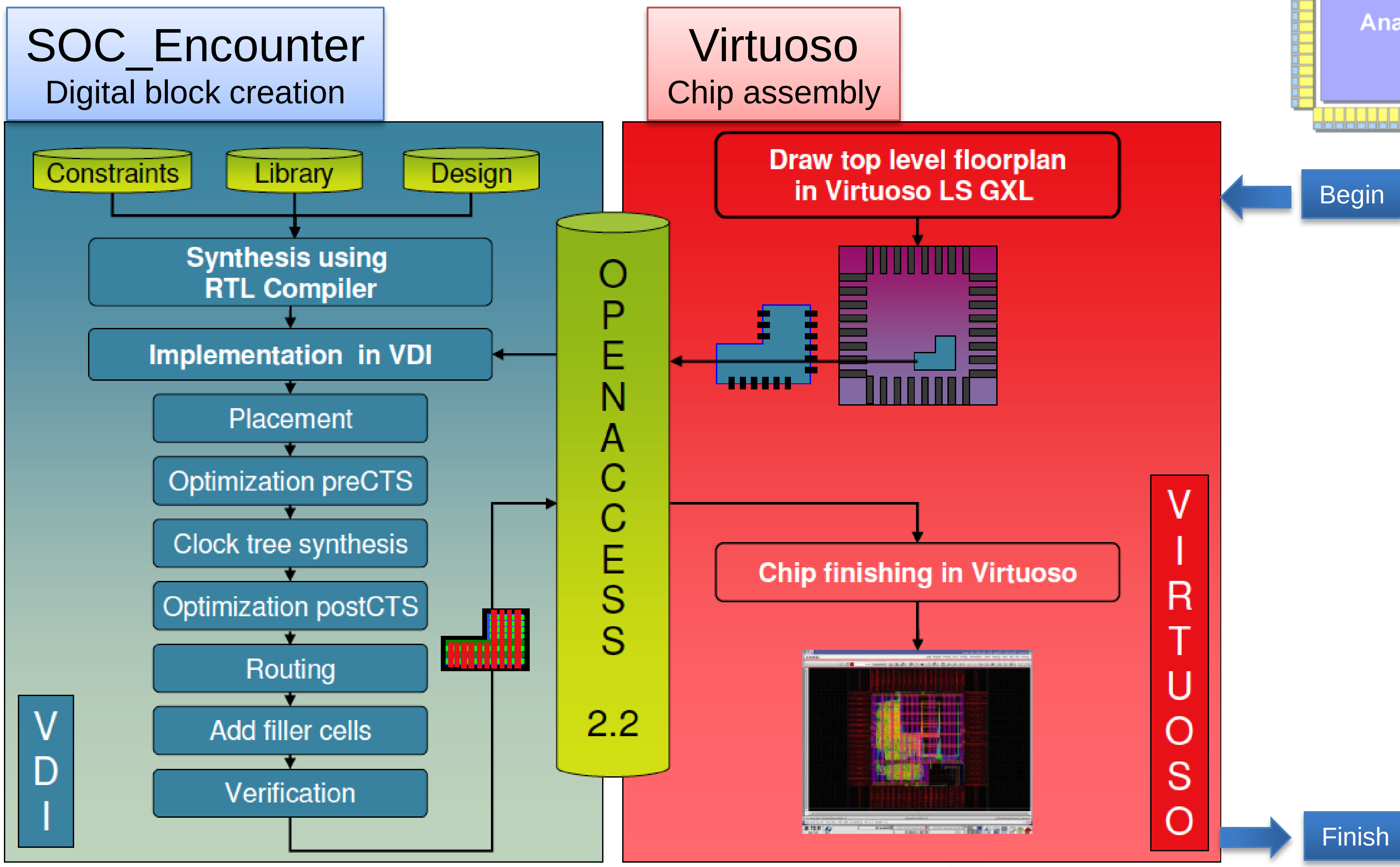
- an OA PDK+Library package will be created
  - Suitable for both analog and digital design
  - by CERN, VCAD and an intermediate Silicon Broker
- Create Mixed Signal flows
  - Analog-on-top SoC with digital blocks
  - Digital-on-top SoC with analog blocks
  - Integration done by VCAD
    - Must be validated with a reference design
- Distribution of package to institutes done by Silicon Broker
  - Layout views included in the libraries

"Analog on Top" Design Flow

Chip Finishing in Virtuoso

For big 'A' small 'D' designs.

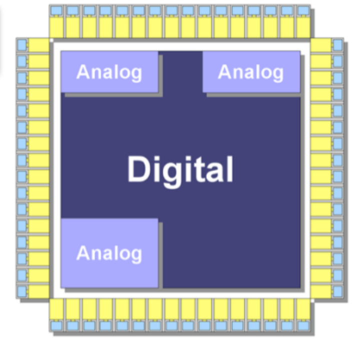




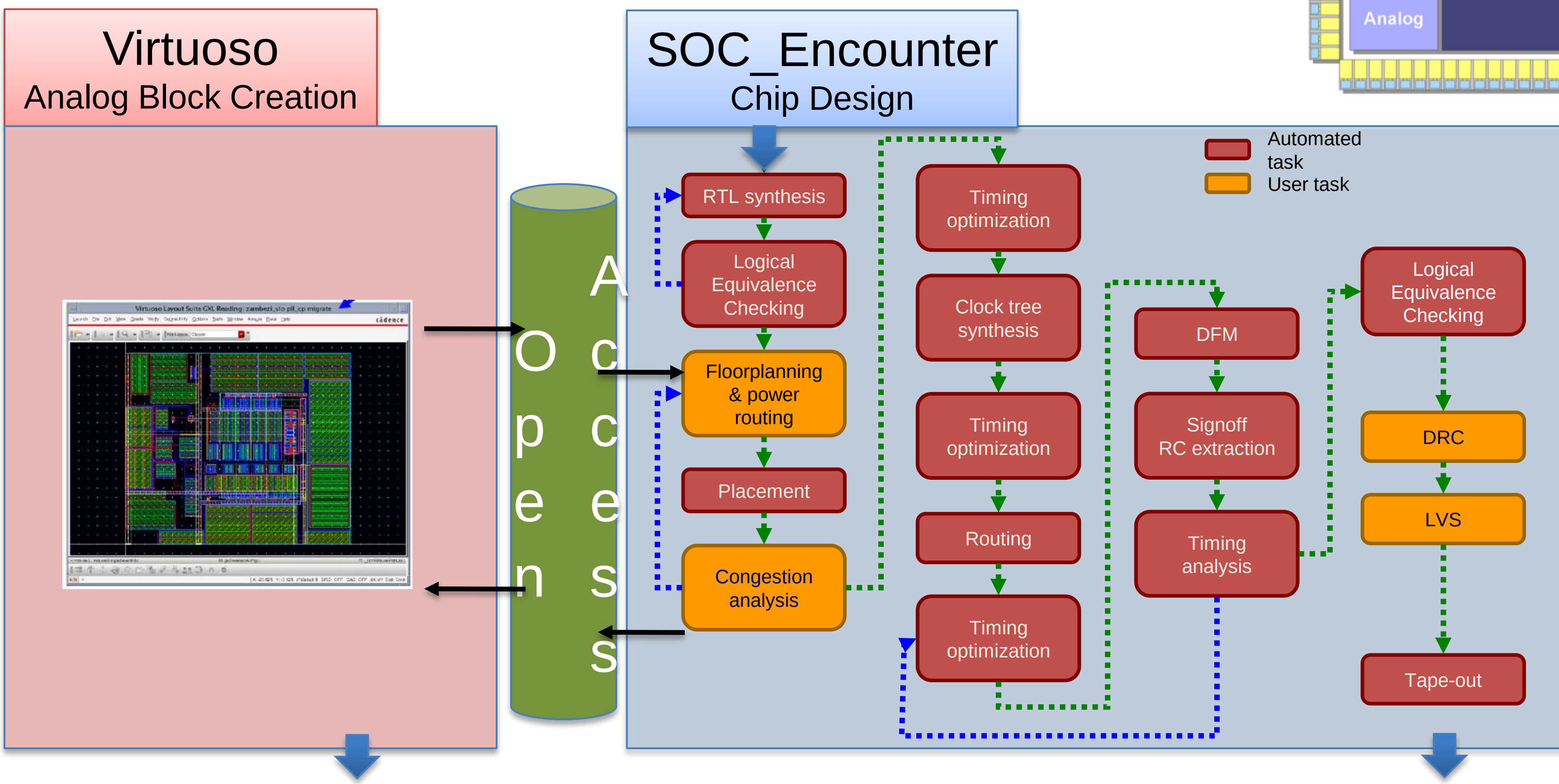
“Digital on Top” Design Flow

Chip Finishing in SOC Encounter

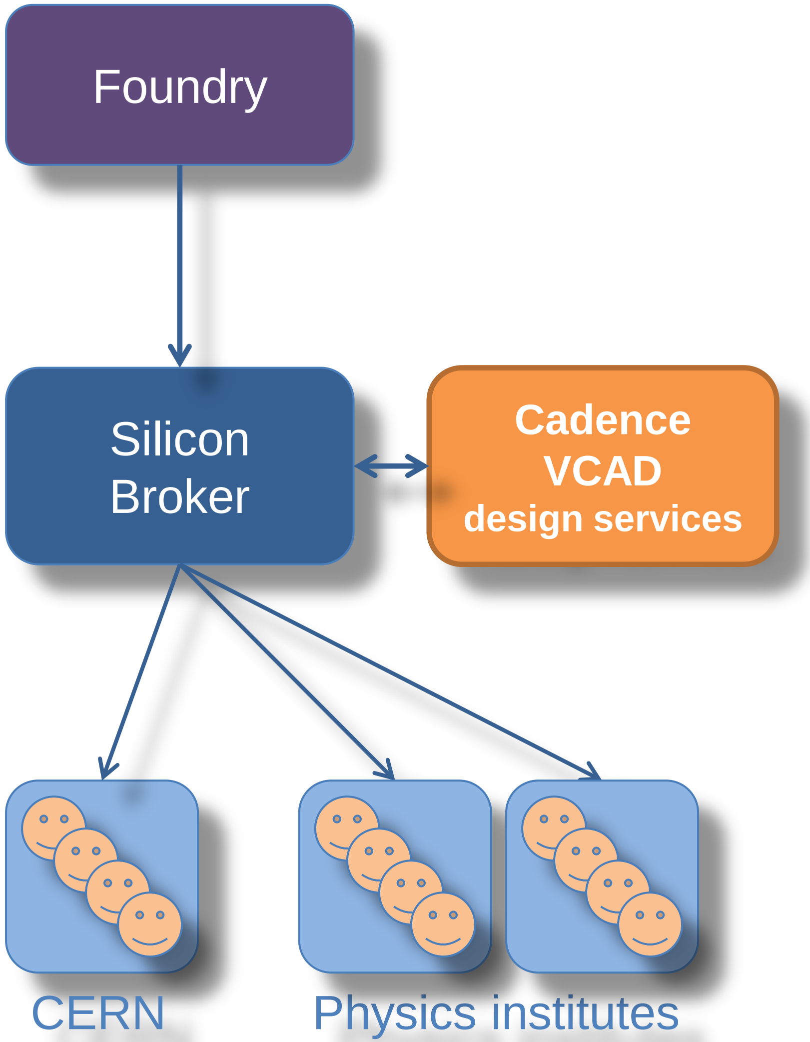
For big ‘D’ small ‘A’ designs.



Customized, fully scripted digital implementation flow.



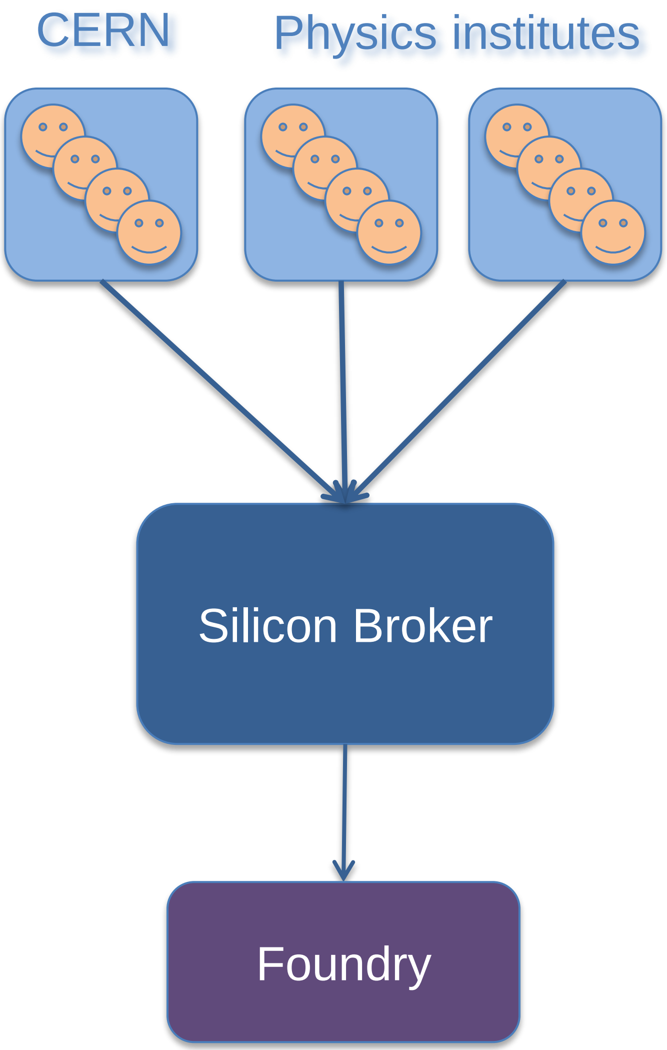
M/S flow distribution #2



- The role of the Silicon Broker will include
  - distribution of the package to HEP Institutes and give support
  - Maintenance of the PDK and libraries with updates from foundry
    - depending on frequency of updates and their complexity
  - Organization of workshop / training courses on the Mixed Signal flow
    - Reference design given as example
  - Organization of common MPW runs for users

Foundry Access Services

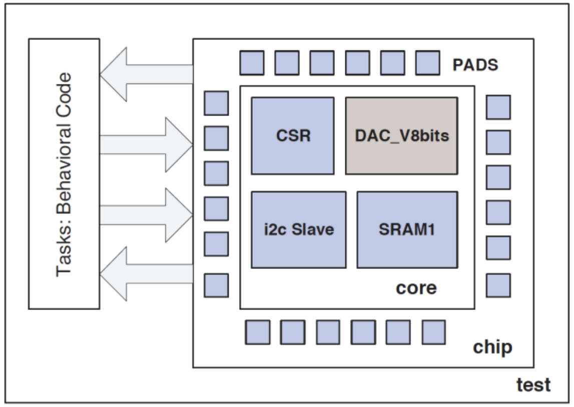
- Foundry Access
  - MPW as scheduled from Silicon Broker
    - Might have to adapt metal stack
  - Additional runs for HEP
    - Metal stack 4-thin, 2-thick,
    - Possibly every 4 months?
  - Engineering/production runs
    - Physics institutes can send the purchase order via CERN
    - GDS will be submitted directly to Broker



Training: M/S kit Workshops

- A series of Training Workshops for 65nm CMOS will be organized
  - To present the Mixed Signal Kit.
  - To present Analog, Digital and Mixed Signal design Workflows.
  - Cadence (VCAD) design services team (TBD):
    - Will prepare the training lectures and the accompanying documentation
    - Will provide engineers to lecture in the courses.
  - 5 days training with lectures and hands-on design exercises
  - Workshop modules based on a realistic Mixed Signal Design
  - Training material (scripts, design examples and documentation) made available to participants.

Example Mixed Signal ASIC:
"8-bit DAC with I^2C serial interface"



Radiation performance

- 65 nm demonstrates a better radiation hardness than previous generation technologies
  - Core transistors
    - Very small threshold voltage shifts (<60mV @200Mrad) and leakage currents
    - No ELT necessary for digital core logic
      - …but W_{PMOS}>1um helps limiting drive/speed loss
  - I/O devices still need ELT
    - PMOS loss of drive current (-transconductance & +threshold voltage)
    - …needs to be oversized!
  - SEU performance is better as sensitive areas are smaller
    - ~4x cross-section reduction with respect to 130nm
    - But beware in using more logic in chips
    - More evident MBUs
      - Observed up to 10-bit upsets in SRAM @1.2V, LET=20.4 MeVcm2/mg
      - MBU contribution in D-FF registers is ~0.5% due to 2-BU and 3-BU.

Rad-hard CMOS I/O pad library

- Standard I/O pad library from foundry may suffer from radiation effects
  - Use of 2.5V-rated transistors with >5-nm-thick gate oxide
  - NMOS leakage
  - PMOS tend to turn off + loss in transconductance
    - ~50% loss in maximum drive current within 200 Mrad
    - Speed reduction
- Radiation hardened I/O pad library
  - Rated for 1.2V or 1.0V
  - Only core devices, thin gate oxide
  - Better radiation performance
  - To be packaged together with the OA M/S design kit

Timeline

- Sep. 2012: Market survey closed.
- Oct. 2012: Call for tender.
- Dec. 2012: Contract approved by CERN Finance Committee
- Jan. 2013: PDK+Library integration work start with VCAD

Extension to 130 nm

- Market survey includes access to older technology nodes: 130 nm
- The same scheme of M/S kit development and distribution can be applied to 130 nm
  - CERN would continue to work with IBM and the new foundry in parallel
  - Libraries and metal stack To Be Defined
  - Radiation Hardness must be investigated

Conclusions

- Need an integrated OA PDK and digital library in 65 nm
  - For Mixed Signal System-On-Chip design
  - Standardized workflows
  - Roles of Silicon Broker could include:
    - Maintenance
    - Training
    - Support
    - Foundry access
  - Cadence VCAD can provide development and help when necessary

- The same concept can be applied in 130 nm

- Future plans
  - Design CMOS I/O standard pad library
  - Further investigation on radiation performance