TWEPP-12
Topical Workshop on Electronics for Particle Physics
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GLIB status update

Paschalis VICHOUDIS

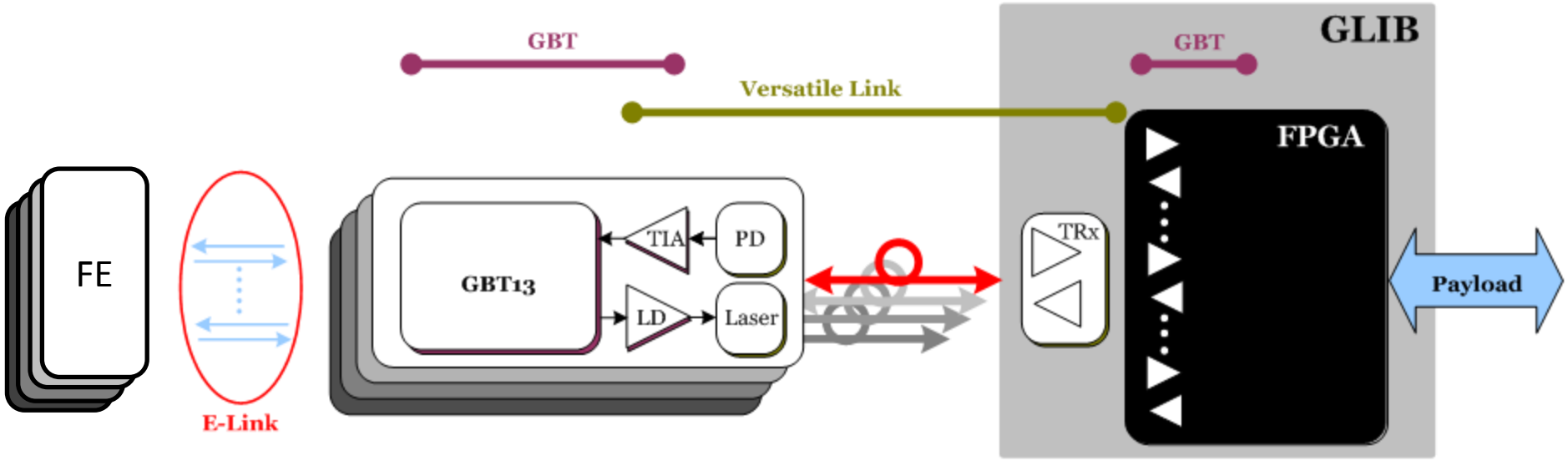
CERN
PH-ESE-BE

on behalf of
M. Barros Marin, S. Baron, V. Bobillier, S. Haas, M. Hansen, M. Joos, L. Lobato Pardavila, F. Vasey

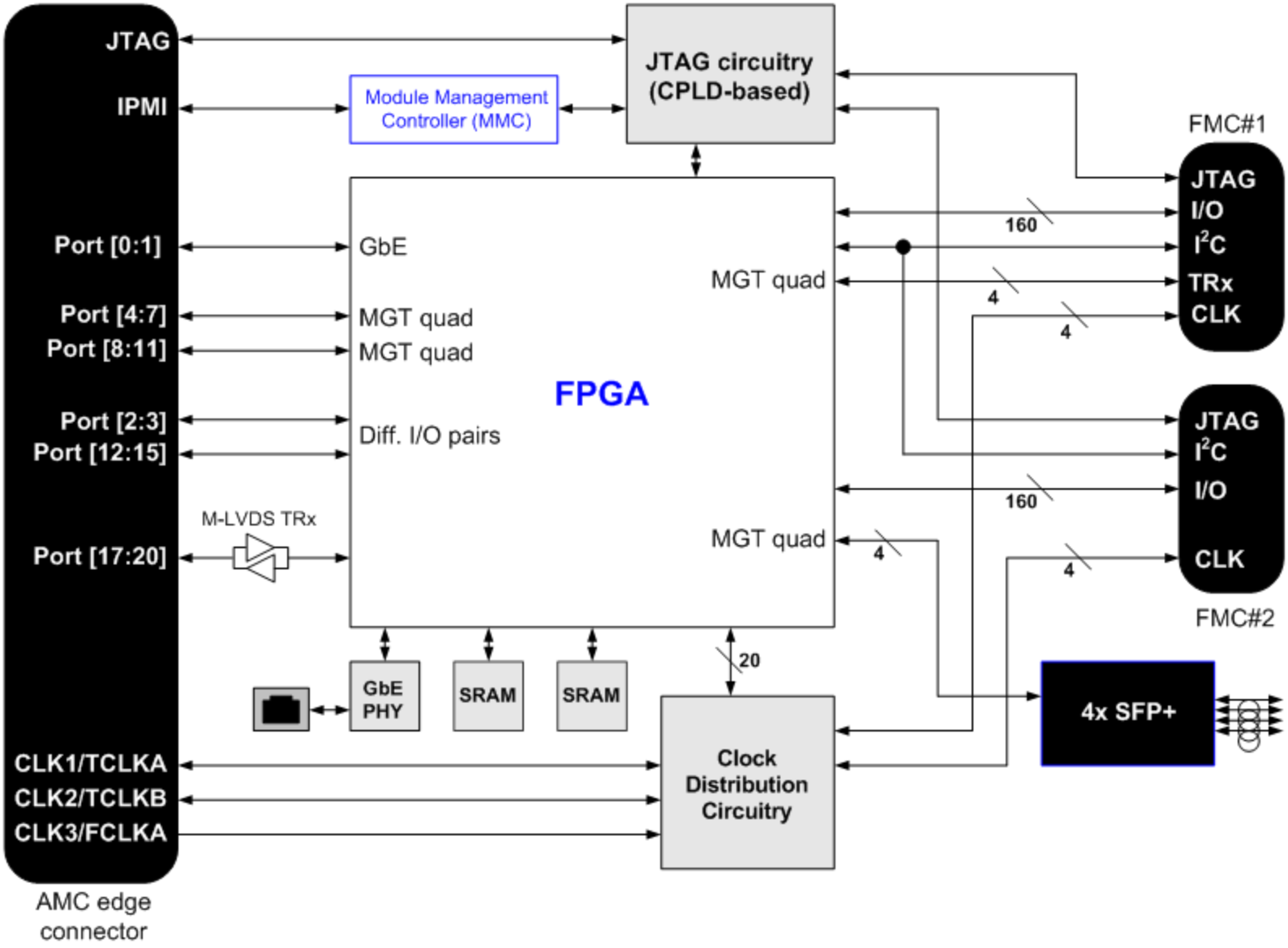
THE GLIB IS: an evaluation platform and an easy entry point for users of high speed optical links

THE GLIB IS TARGETED FOR:

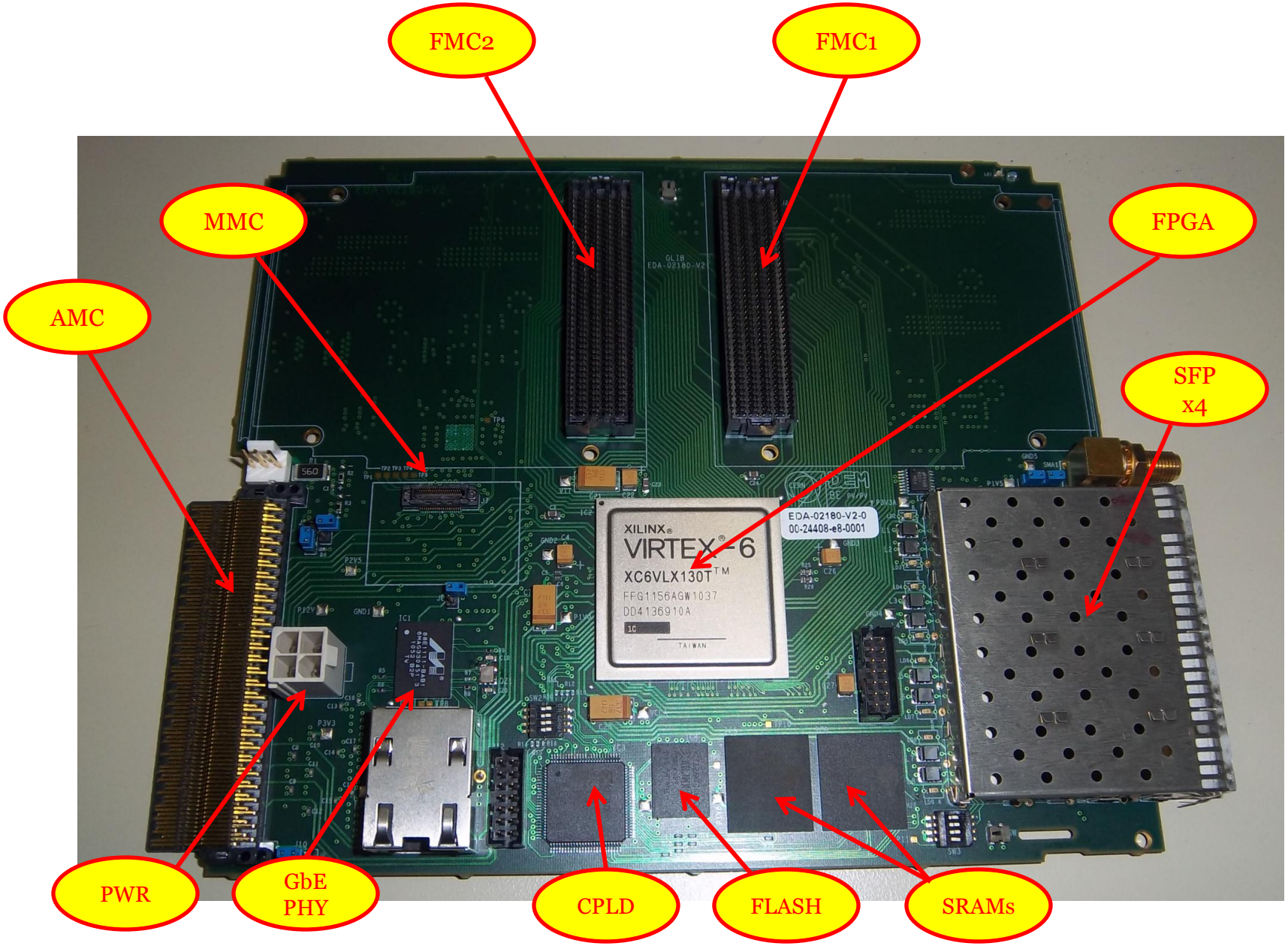
- optical link evaluation in the laboratory
- control, triggering and data acquisition from remote modules in beam or irradiation tests



ARCHITECTURE



THE BOARD


FMC2
FMC1
MMC
FPGA
AMC
SFP
x4
PWR
GbE
PHY
CPLD
FLASH
SRAMs
XILINX
VIRTEX-6
XC6VLX130T
FFG1156AGW1037
EDA-02180-V2-0
00-24408-e8-0001

HISTORY

- Mar-2010: **1st Spec draft**
- Sep-2010: **Spec Approval**
- Jan-2011: **1st prototype**
- Aug-2011: **2nd prototype (GLIB v2)**
- Nov-2011: **1st release to beta users (HW/FW/SW)**
- May-2012: **Feedback deadline for the final prototype**
  Production of GLIB v2 (10pcs) to satisfy high demand
- Jun-2012: **Final prototype design (GLIB v3)**

- Sep-2012: **Preproduction (2pcs)**
- Dec-2012: **Production (40pcs)**

ACHIEVEMENTS

- **GBT FPGA HDL core improvements**
  - Minimized the latency (20-bit MGT interface instead of 40)
  - Adapted the HDL core to Virtex-6 features for deterministic operation
- **Demonstration of GBT communication**
  - between a GLIB and the GBT evaluation board
  - between two GLIB cards with unrelated clocks
- **Successful IPMI, GbE & PCIe operation in µTCA crate**
- **Successful integration of commercial & custom FMC modules for I/O expansion**
  - GLIB ecosystem is growing
- **Firmware architecture for facilitating user development**
  - Available to all CERN users via SVN
- **Hardware delivered to users**
  - 12 GLIB v2 already, more to come
- **Big interest from the community**
  - All production boards already reserved

Projects	Users
ATLAS TileCal	S. Muschter (Stockholm)
ALICE DAQ	F. Costa (CERN) & W. Rauch (Frankfurt)
Versatile Link	C. Soos & S. Detraz (CERN)
CMS Tracker	L. Gross & L. Charles (CNRS Strasburg)
ATLAS Muon	M. Fras (Max Planck)
CMS BRM	M. Hansen (CERN)
CMS GEM	G. De Lentdecker (Brussels)
CMS HCAL	T. Grassi (Maryland) & U. Behrens (DESY)
CMS Tracker	D. Contardo (Lyon)
LHCb VELO	J. Buytaert (CERN)
Versatile Link	A. Prosser (FNAL)
ATLAS Strip Tracker	M. Warren (UCL)
ATLAS Muon Micromegas	K. Johns (Arizona) & V. Polychronakos (BNL)
CMS TTC	M. Hansen (CERN)
CMS DAQ	A. Racz (CERN)
CMS HCAL	W. Beaumont (Antwerpen) & D. Newbold (Bristol)
LHCb SciFi Tracker	H. Chanal (Clermont-Ferrand)
CLIC Acquisition & Control	B. Bielawski (CERN)
GBT Testing	T. Grassi (Maryland)

- **Signal Integrity:**
  - Improved routing of high-speed signals

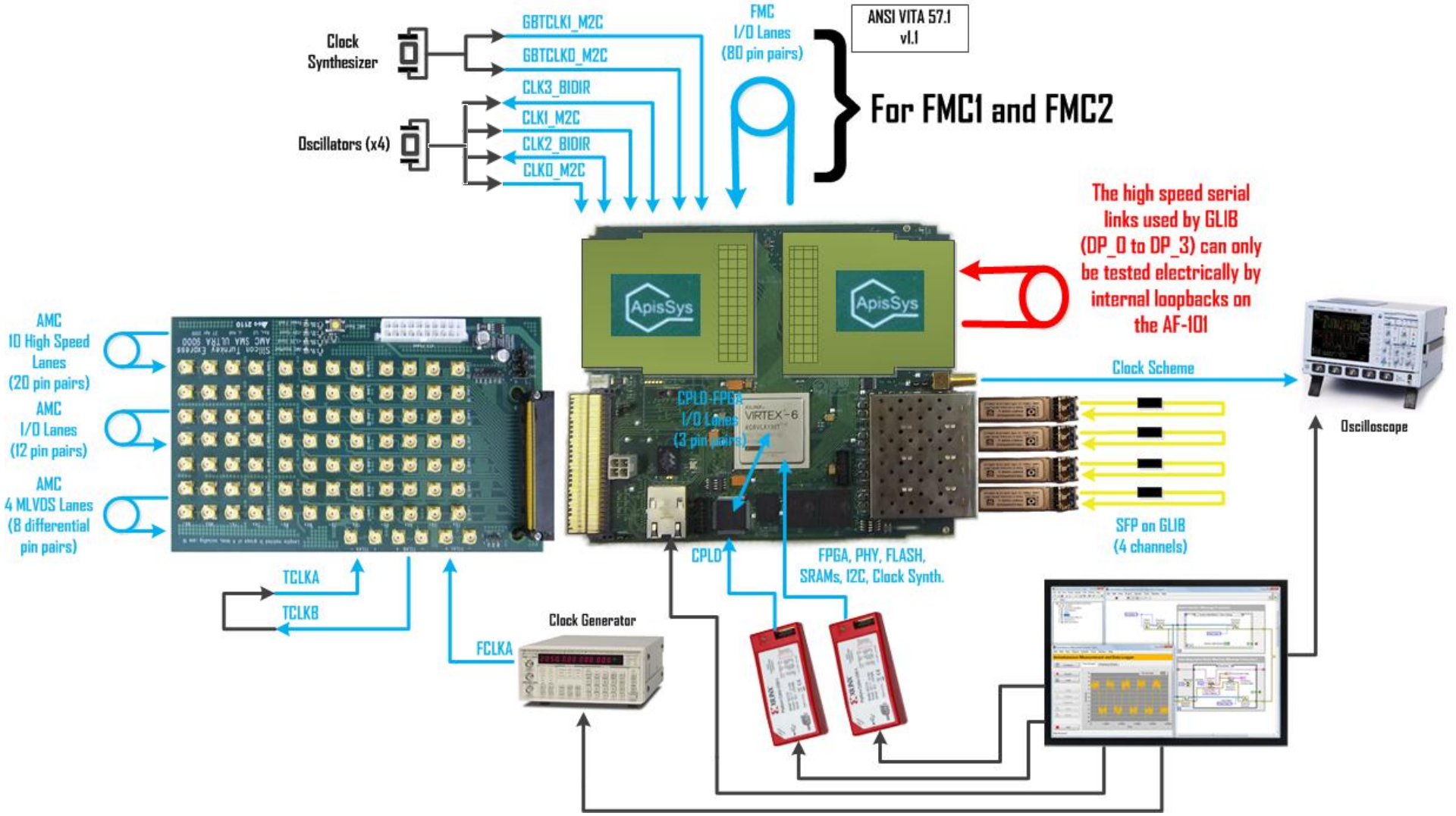
- **Clocking:**
  - Connected the GBTCLKs from FMC1
  - Unidirectional TCLKA (from MCH to GLIB)
  - Unidirectional TCLKB (from GLIB to MCH)

- **Configuration:**
  - add nets to allow the MMC to select FLASH page for FPGA conf.

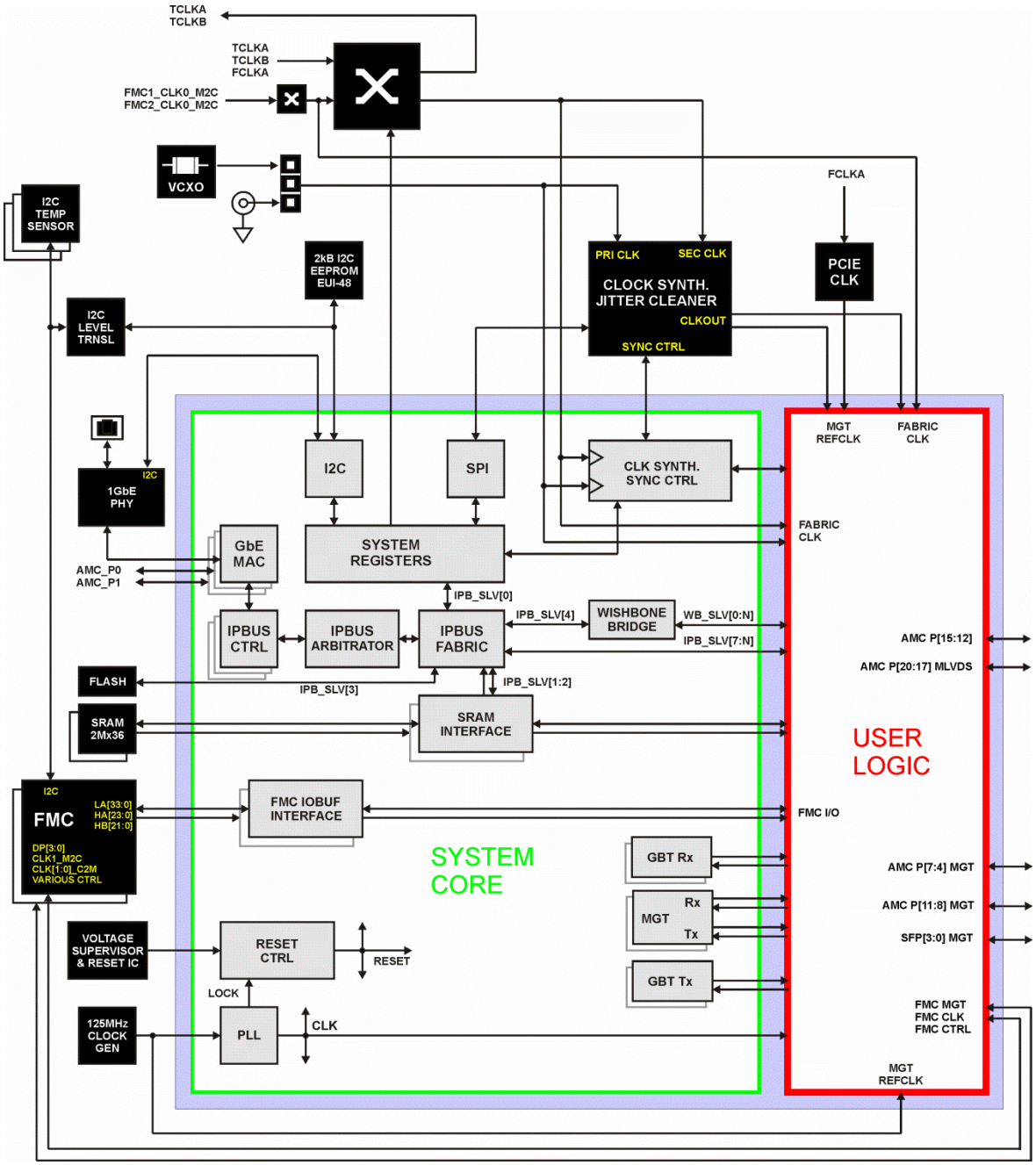
- **Mechanical:**
  - move the FMCs closer to board's edge

- **Minor:**
  - add in the front panel user LEDs connected to FPGA & CPLD
  - add missing pull-ups etc
  - enable SRAM byte-wise operation
  - GbE PHY management both with I2C & MDC/MDIO

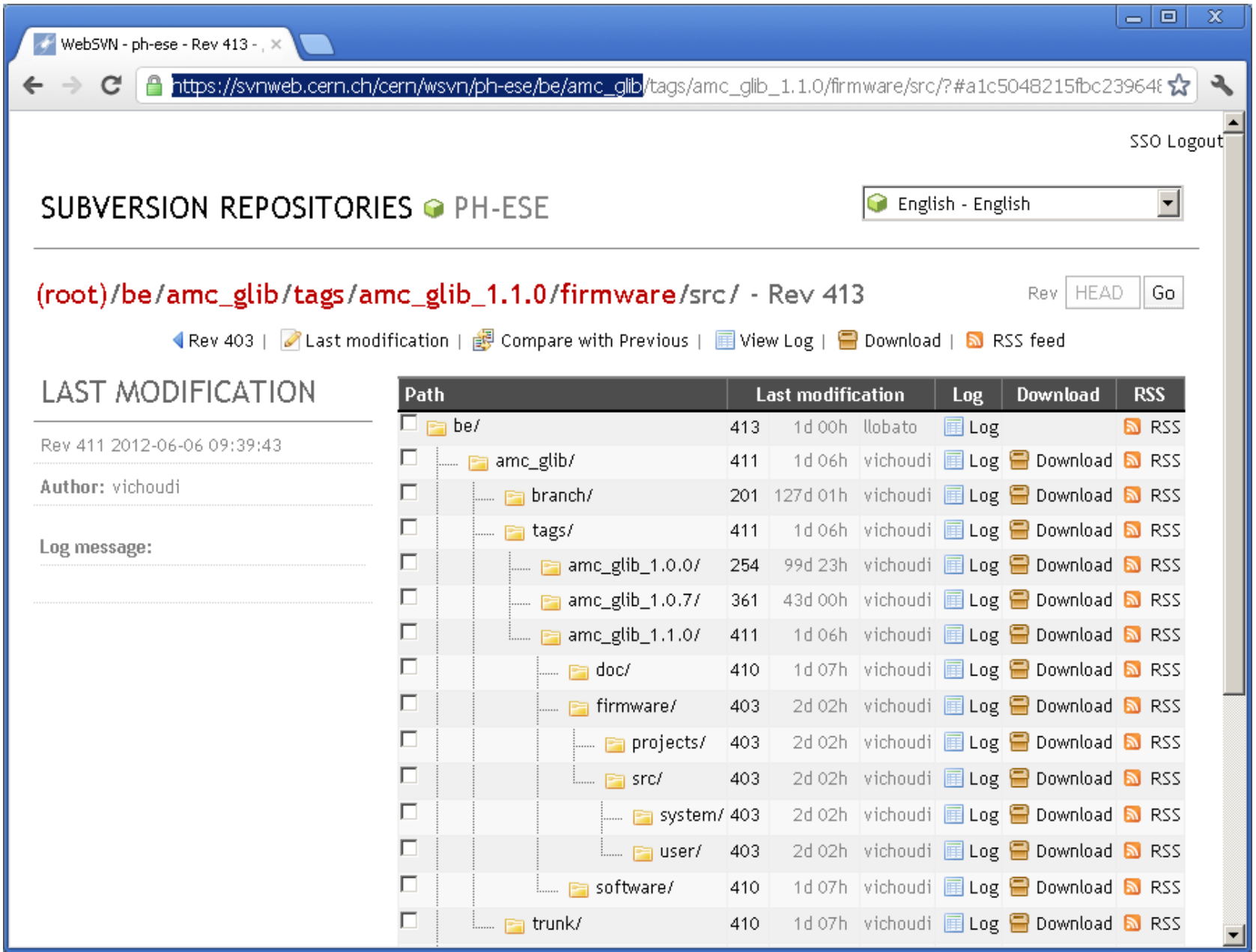
GLIB v3 TEST-BENCH



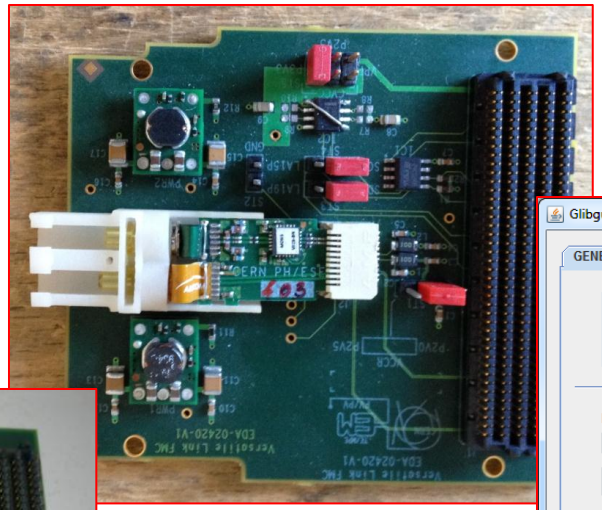
FIRMWARE

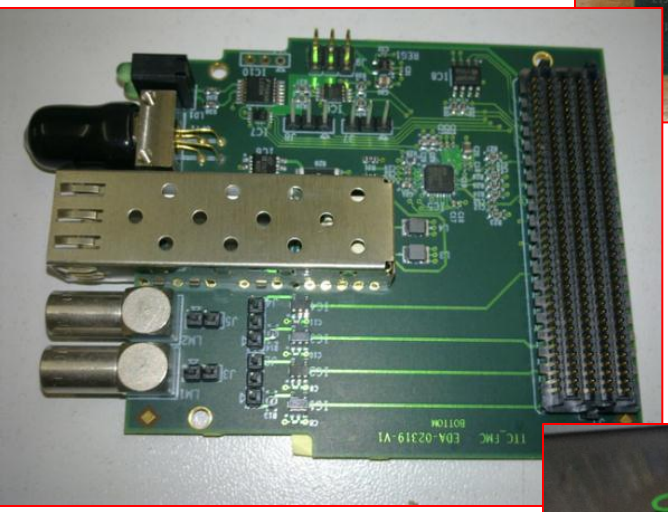

TCLKA
TCLKB
TCLKA
TCLKB
FCLKA
FMC1_CLK0_M2C
FMC2_CLK0_M2C
VCXO
FCLKA
I2C TEMP SENSOR
2kB I2C EEPROM EUI-48
PRI CLK
SEC CLK
CLOCK SYNTH. JITTER CLEANER
CLKOUT
SYNC CTRL
PCIE CLK
I2C LEVEL TRNSL
MGT REFCLK
FABRIC CLK
I2C
1GbE PHY
I2C
SPI
CLK SYNTH. SYNC CTRL
FABRIC CLK
GbE MAC
SYSTEM REGISTERS
AMC_P0
AMC_P1
IPB_SLV[0]
IPB_SLV[4]
WISHBONE BRIDGE
WB_SLV[0:N]
IPB_SLV[7:N]
IPBUS CTRL
IPBUS ARBITRATOR
IPBUS FABRIC
AMC P[15:12]
AMC P[20:17] MLVDS
FLASH
IPB_SLV[3]
IPB_SLV[1:2]
SRAM 2Mx36
SRAM INTERFACE
USER LOGIC
I2C
FMC
LA[33:0]
HA[23:0]
HB[21:0]
DP[3:0]
CLK1_M2C
CLK[1:0]_C2M
VARIOUS CTRL
FMC IOBUF INTERFACE
FMC I/O
SYSTEM CORE
GBT Rx
AMC P[7:4] MGT
MGT
Rx
Tx
AMC P[11:8] MGT
SFP[3:0] MGT
VOLTAGE SUPERVISOR & RESET IC
RESET CTRL
RESET
GBT Tx
LOCK
125MHz CLOCK GEN
PLL
CLK
FMC MGT
FMC CLK
FMC CTRL
MGT REFCLK

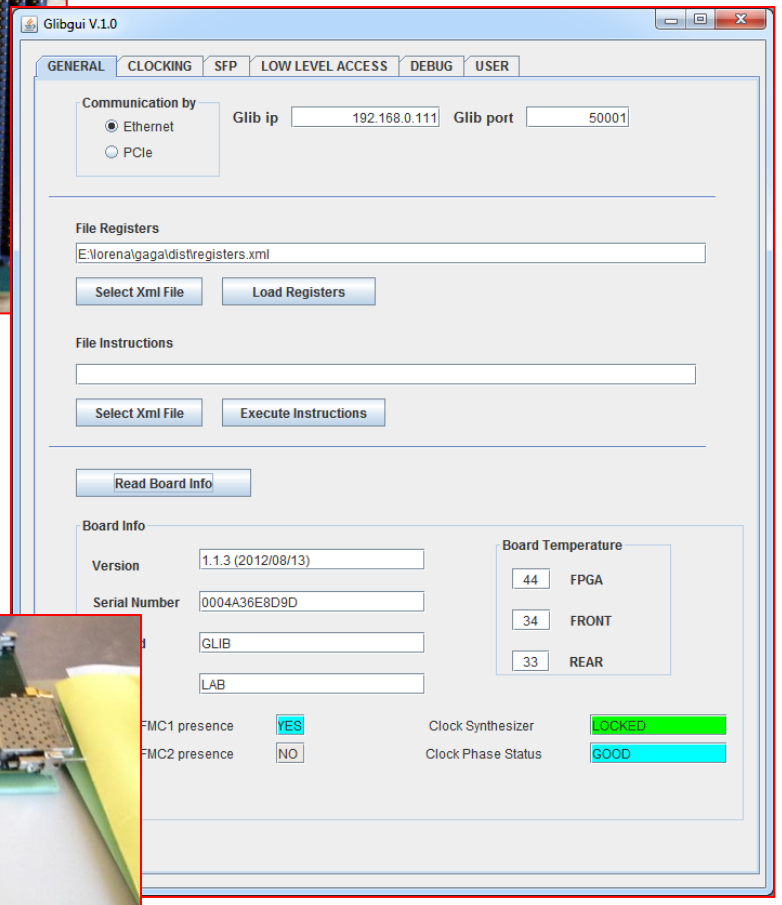
FIRMWARE SVN



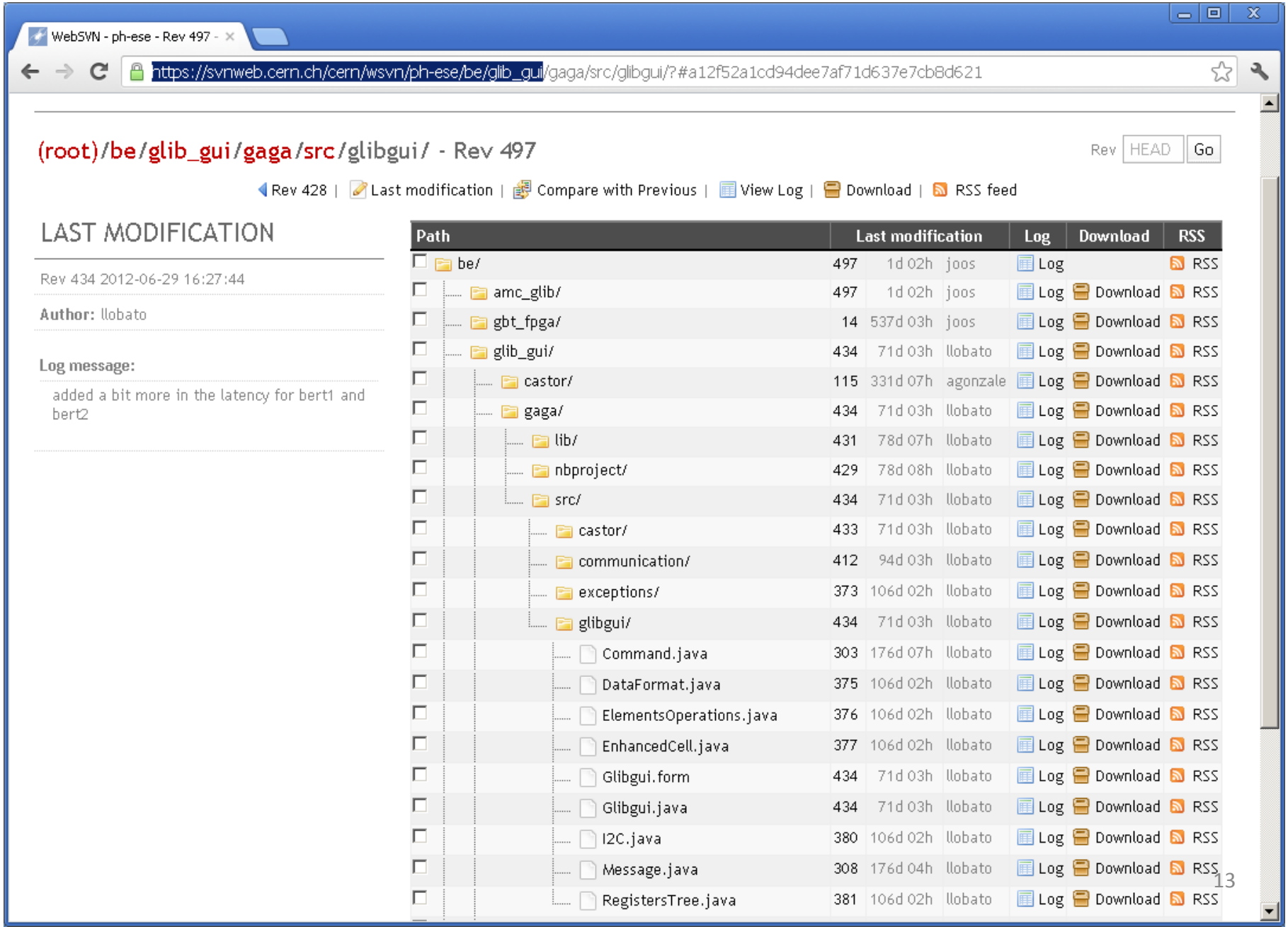
THE ECOSYSTEM







GUI SVN


WebSVN - ph-ese - Rev 497 -
https://svnweb.cern.ch/cern/wsvn/ph-ese/be/glib_gui/gaga/src/glibgui/?#a12f52a1cd94dee7af71d637e7cb8d621
(root)/be/glib_gui/gaga/src/glibgui/ - Rev 497
Rev HEAD Go
Rev 428 | Last modification | Compare with Previous | View Log | Download | RSS feed
LAST MODIFICATION
Rev 434 2012-06-29 16:27:44
Author: llobato
Log message:
added a bit more in the latency for bert1 and bert2
Path | Last modification | Log | Download | RSS
be/ 497 1d 02h joos Log RSS
amc_glib/ 497 1d 02h joos Log Download RSS
gbt_fpga/ 14 537d 03h joos Log Download RSS
glib_gui/ 434 71d 03h llobato Log Download RSS
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exceptions/ 373 106d 02h llobato Log Download RSS
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Command.java 303 176d 07h llobato Log Download RSS
DataFormat.java 375 106d 02h llobato Log Download RSS
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EnhancedCell.java 377 106d 02h llobato Log Download RSS
Glibgui.form 434 71d 03h llobato Log Download RSS
Glibgui.java 434 71d 03h llobato Log Download RSS
I2C.java 380 106d 02h llobato Log Download RSS
Message.java 308 176d 04h llobato Log Download RSS
RegistersTree.java 381 106d 02h llobato Log Download RSS

SUMMARY

Although only 2,5 year old project, GLIB it is in a very advanced stage

Boards are already delivered to users:

CMS, ATLAS, ALICE, LHCb

Big interest from the community:

requests for boards from various institutes

expect to see GLIB used in several projects in 2013

In Production phase: 40pcs will be produced by end 2012

Additional batches on request (10pcs minimum)

Important spin-offs: TTC FMC, significant improvements of GBT-FPGA HDL core