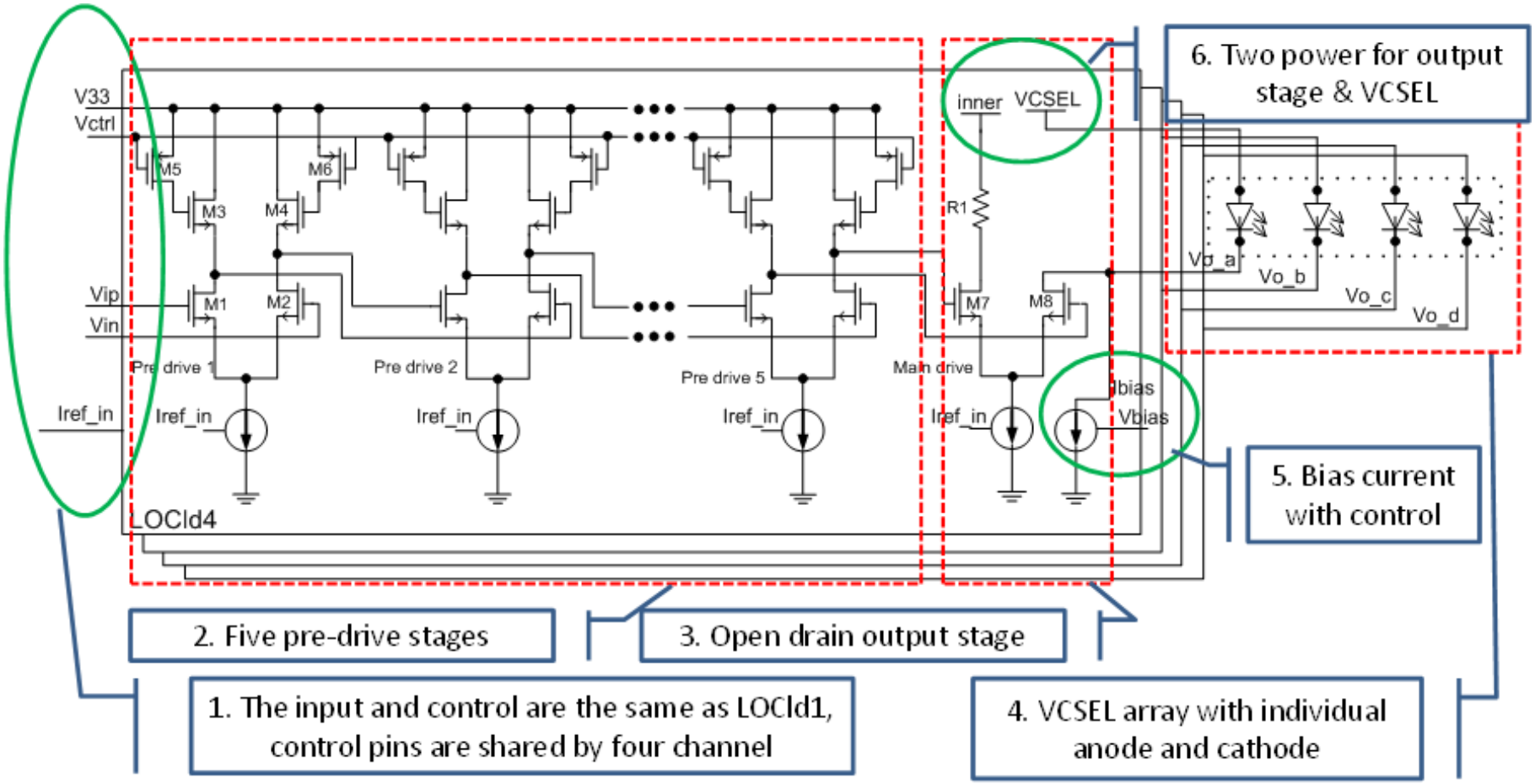
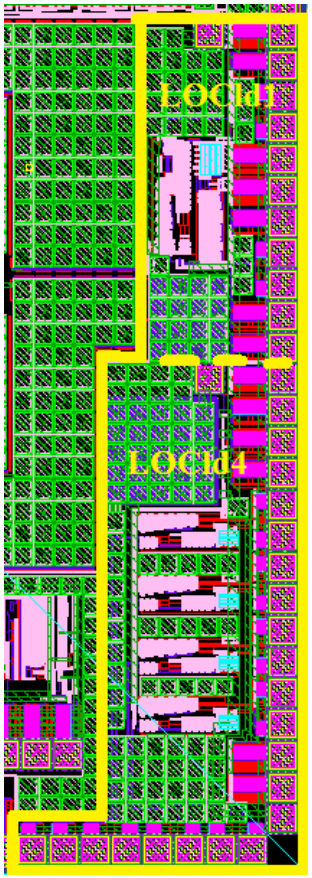
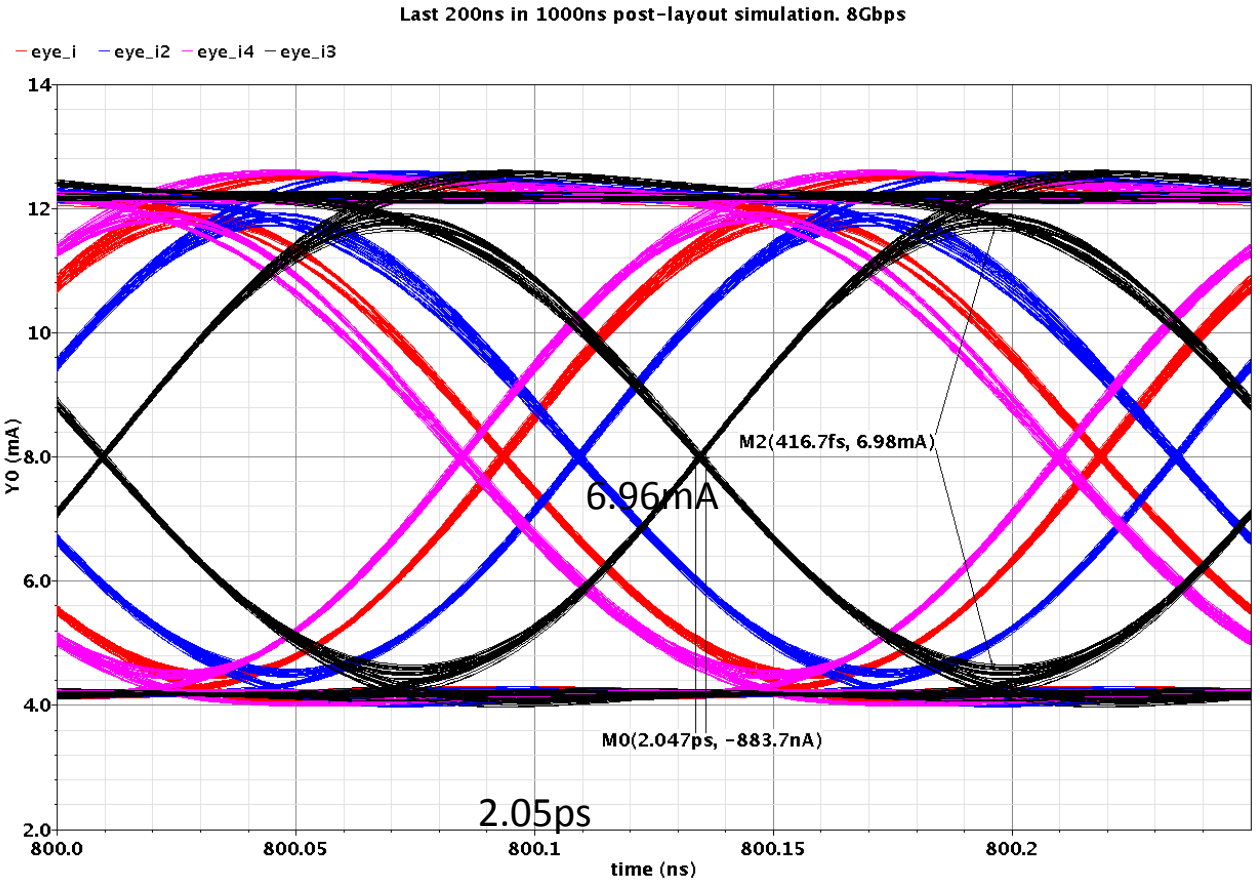
VCSEL array driver



Block diagram of LOCld4

VCSEL array driver





Post layout simulation at 8 Gbps, typ. conditions

- Fabricated in a 0.25-um silicon-on-sapphire (SoS) CMOS process
- To be delivered next week